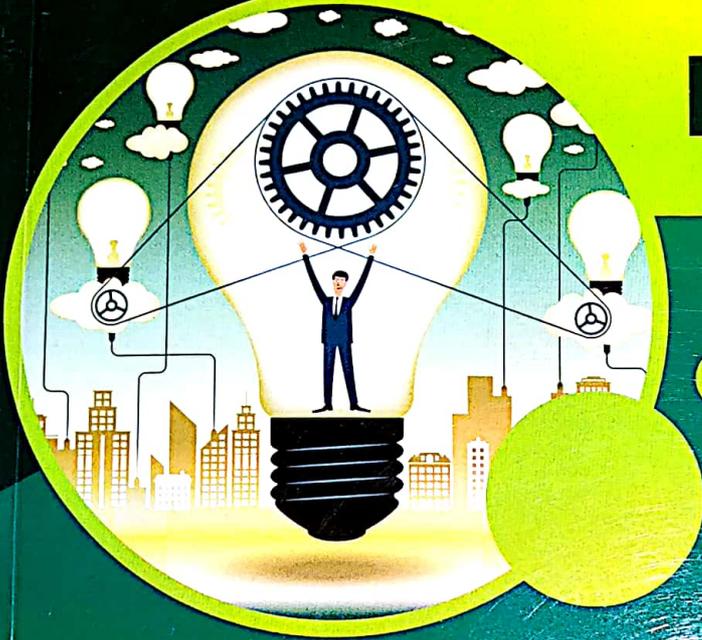


Digital Fundamentals



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● AS PER NEW SYLLABUS OF
GUJARAT TECHNOLOGICAL UNIVERSITY

● SEMESTER III (CE/IT)

● SIMPLIFIED APPROACH

● CHAPTERWISE SOLVED GTU QUESTIONS
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● ORAL QUESTIONS & ANSWERS

MODEL PAPER

AS PER NEW QUESTION PAPER PATTERN



**TECHNICAL
PUBLICATIONS**

An Up-Thrust for Knowledge

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**Solved Model Question Paper
[As per New Question Paper Pattern]**

(S - 1) to (S - 2)

1

Fundamentals of Digital Systems and Logic Families

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1.1 Digital Signals

Analog versus Digital

Analog systems process information that varies continuously i.e. they process time varying signals that can take on any value across a continuous range of voltage, current or any physical parameter. On the other hand, the digital systems use discrete quantities to represent information. Discrete means distinct or separated as opposed to continuous and connected. The Fig. 1.1.1 shows the difference between two signals : continuous and discrete.

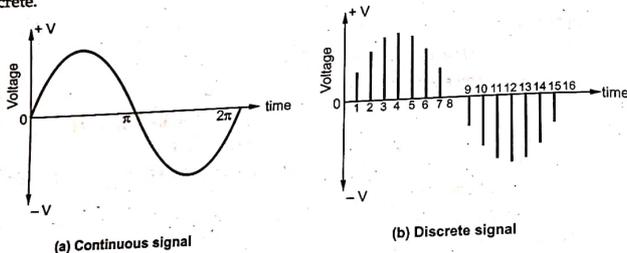


Fig. 1.1.1

Digital / discrete signal : A digital/discrete signal is a signal that can have one of a finite set of possible values at any time.

Analog / continuous signal : An analog/continuous signal is a signal that can have one of an infinite number of possible values.

Binary signal : In digital systems, the most common digital signal is the signal that has one of two possible values, like on or off (often represented as 1 or 0). Such signal is known as binary signal. In digital systems number formed by binary values are used to represent the levels of discrete signal.

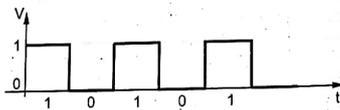


Fig. 1.1.2 Binary signal

The reasons for widespread use of digital systems are :

1. They are easy to design.
2. They are more flexible in design.
3. They provide higher accuracy.

4. They are less affected by component aging and noise.
5. They are also less affected by variations in power-supply voltage and temperature.
6. They can have memory and hence they are highly suitable for computers, calculators, watches, etc.
7. It is easy to provide added functionality in digital systems than analog systems.
8. They always produce exactly same results with same set of inputs and circuit components.
9. In digital systems, display of information is very convenient, accurate and elegant.
10. They are cost effective.
11. HDL (Hardware Description Languages) are available; they make digital system design simple.
12. Communication between digital systems is much more easier.

Advantage of Binary

- The base for all digital system operations is the binary number system. Though many systems use octal, decimal and hexadecimal number system, when the data is provided to a digital system it is in the form of binary numbers. Thus, all computers represent numbers and alphabetic characters in the binary form.
- In binary number system there are only two logic values viz. logic 0 and logic 1. These two logic values are also known as low level logic/OFF and high level logic/ON. Thus, binary number system is easy, highly reliable and accurate.
- The binary number system can produce two different states easily. For example, a flip-flop has output either '1' or '0'. This make the use of binary system a very reasonable choice, in case of various electronic circuits.
- Though multilevel circuits having more than two output levels have been studied since long time, binary circuits are universal in computer systems.

Review Questions

1. Define digital signal and analog signal.
2. Compare digital signal with analog signal.
3. What is binary signal ?
4. State the advantages of digital systems/digital circuits.
5. Give the advantages of binary number system.

1.2 Number Systems

- Number system is a basis for counting various items.

- The decimal number system has 10 digits : 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.
- Modern computers communicate and operate with binary numbers which use only the digits 0 and 1.
- When decimal quantities are represented in the binary form, they take more digits.
- For large decimal numbers people have to deal with very large binary strings and therefore, they do not like working with binary numbers. This fact gave rise to three new number systems : Octal, Hexadecimal and Binary Coded Decimal (BCD).

Review Questions

1. Explain various number systems.
2. Name the number system used in computers.

1.3 Representation of Numbers of Different Radix

1.3.1 Decimal Number System

- In decimal number system we can express any decimal number in units, tens, hundreds, thousands and so on.
- When we write a decimal number say, 5678.9, we know it can be represented as $5000 + 600 + 70 + 8 + 0.9 = 5678.9$
- The decimal number 5678.9 can also be written as 5678.9_{10} , where the 10 subscript indicates the radix or base.
- The position of a digit with reference to the decimal point determines its value/weight. The sum of all the digits multiplied by their weights gives the total number being represented.
- The leftmost digit, which has the greatest weight is called the **most significant digit** and the rightmost digit, which has the least weight, is called the **least significant digit**.
- Fig. 1.3.1 shows decimal digit and its weights expressed as a power of 10.

	10^3	10^2	10^1	10^0		10^{-1}
	5	6	7	8	.	9
In power of 10	5×10^3	6×10^2	7×10^1	8×10^0	.	9×10^{-1}
	MSD					LSD

Fig. 1.3.1 Representation of a decimal number

1.3.2 Binary Number System

- Binary system with its two digits is a **base-two system**.
- The two binary digits (bits) are 1 and 0.
- In binary system, weight is expressed as a power of 2.
- The Fig. 1.3.2 (a) shows representation of binary number 1101.101 in power of 2.
- By adding each digit of a binary number in a power of 2 we can find the decimal equivalent of the given binary number.

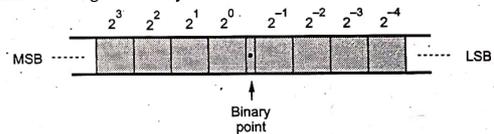


Fig. 1.3.2 Binary position values as a power of 2

	2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}
N =	1	1	0	1	.	1	0	1
	1×2^3	1×2^2	0×2^1	1×2^0	.	1×2^{-1}	0×2^{-2}	1×2^{-3}

$$N = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} = (13.625)_{10}$$

Fig. 1.3.2 (a)

1.3.3 Octal Number System

- The octal number system uses first eight digits of decimal number system : 0, 1, 2, 3, 4, 5, 6 and 7. As it uses 8 digits, its base is 8.
- For example, the octal number 5632.471 can be represented in power of 8 as shown in Fig. 1.3.2 (b).

	8^3	8^2	8^1	8^0		8^{-1}	8^{-2}	8^{-3}
N =	5	6	3	2	.	4	7	1
	5×8^3	6×8^2	3×8^1	2×8^0	.	4×8^{-1}	7×8^{-2}	1×8^{-3}

$$N = 5 \times 8^3 + 6 \times 8^2 + 3 \times 8^1 + 2 \times 8^0 + 4 \times 8^{-1} + 7 \times 8^{-2} + 1 \times 8^{-3} = (2970.611328)_{10}$$

Fig. 1.3.2 (b)

- By adding each digit of an octal number in a power of 8 we can find the decimal equivalent of the given octal number.

1.3.4 Hexadecimal Number System

- The hexadecimal number system has a base of 16 having 16 characters : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F.
- Table 1.3.1 shows the relationship between decimal, binary, octal and hexadecimal.

Decimal	Binary	Octal	Hexadecimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

Table 1.3.1 Relation between decimal, binary, octal and hexadecimal numbers

- For example, 3FD.84 can be represented in power of 16 as shown below.
- By adding each digit of a hexadecimal number in a power of 16 we can find decimal equivalent of the given hexadecimal number.

$$N = \begin{matrix} & 16^2 & 16^1 & 16^0 & & 16^{-1} & 16^{-2} \\ \begin{matrix} 3 & F & D & & 8 & 4 \end{matrix} \\ \begin{matrix} 3 \times 16^2 & F \times 16^1 & D \times 16^0 & & 8 \times 16^{-1} & 4 \times 16^{-2} \end{matrix} \end{matrix}$$

$$N = 3 \times 16^2 + F \times 16^1 + D \times 16^0 + 8 \times 16^{-1} + 4 \times 16^{-2}$$

$$= 3 \times 16^2 + 15 \times 16^1 + 13 \times 16^0 + 8 \times 16^{-1} + 4 \times 16^{-2} = (1021.515625)_{10}$$

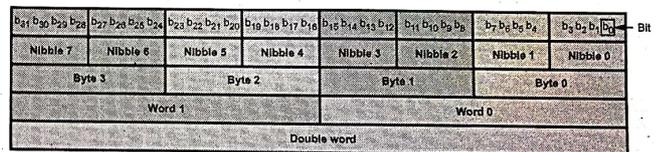
1.3.5 Usefulness of Octal and Hexadecimal System

- When dealing with a large quantity of binary numbers of many bits, it is convenient to use octal and hexadecimal numbers as a "shorthand" means of expressing large binary numbers.

- But it is necessary to keep in mind that the digital circuits and systems work strictly in binary; we are using octal and hexadecimal only as a convenience for the operators of the system.

1.3.6 Format of a Binary Number

- A single digit in the binary number is called bit.



- The following figure shows the format of binary number. Four binary digits form a nibble, eight binary digits form a byte, sixteen binary digits form a word and thirty-two binary digits form a double-word.

Nibble : 4-bits can represent $2^4 = 16$ distinct values

Byte : 8-bits can represent $2^8 = 256$ distinct values

Word : 16-bits can represent $2^{16} = 65536$ distinct values

Double word : 32-bits can represent $2^{32} = 4294967296$ distinct values

1.3.7 Counting in Radix (Base)-r

- Each number system has r set of characters. For example, in decimal number system r equals to 10 has 10 characters from 0 to 9, in binary number system r equals to 2 has 2 characters 0 and 1 and so on.
- In general we can say that, a number represented in radix r, has r characters in its set and r can be any value. This is illustrated in Table 1.3.2.

Radix (Base) r	Characters in set
2 (Binary)	0, 1
3	0, 1, 2
4	0, 1, 2, 3
5	0, 1, 2, 3, 4
6	0, 1, 2, 3, 4, 5
7	0, 1, 2, 3, 4, 5, 6
8 (Octal)	0, 1, 2, 3, 4, 5, 6, 7
9	0, 1, 2, 3, 4, 5, 6, 7, 8
10 (Decimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9
16 (Hexadecimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Table 1.3.2 Radix and character set

Example 1.3.1 Find the decimal equivalent of $(231.23)_4$.

Solution :
$$N = 2 \times 4^2 + 3 \times 4^1 + 1 \times 4^0 + 2 \times 4^{-1} + 3 \times 4^{-2}$$

$$= 32 + 12 + 1 + 0.5 + 0.1875$$

$$= 45.6875_{10}$$

Example 1.3.2 Count from 0 to 9 in radix 5.

Solution : The Table 1.2.2 indicates that radix 5 has 5 characters. A count sequence from 0 decimal to 9 decimal is

00, 01, 02, 03, 04, 10, 11, 12, 13, 14

Example 1.3.3 What is the largest binary number that can be expressed with 12-bits? What is the equivalent decimal and hexadecimal?

Solution : $(1111\ 1111\ 1111)_2$, $(4095)_{10}$, $(FFF)_H$.

1.4 Conversion of Numbers from One Radix to Another Radix

GTU : Dec.-12, 13, May-12, 13, 14, Winter-15, 16, 17, Summer-16, 17, 18

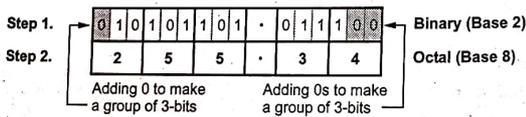
1.4.1 Binary to Octal Conversion

- The base for octal number is 8 and the base for binary number is 2.
- The base for octal number is the third power of the base for binary numbers. Therefore, by grouping 3 digits of binary numbers and then converting each group digit to its octal equivalent we can convert binary number to its octal equivalent.

Example 1.4.1 Convert 10101101.0111 to octal equivalent.

Solution :

Step 1 : Make group of 3-bits starting from LSB for integer part and MSB for fractional part, by adding 0s at the end, if required.



Step 2 : Write equivalent octal number for each group of 3-bits.

$$\therefore (10101101.0111)_2 = (255.34)_8$$

1.4.2 Octal to Binary Conversion

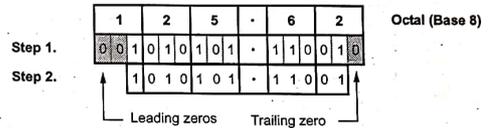
- Conversion from octal to binary is a reversal of the process explained in the previous section. Each digit of the octal number is individually converted to its binary equivalent to get octal to binary conversion of the number.

Example 1.4.2 Convert $(125.62)_8$ to binary.

Solution :

Step 1 : Write equivalent 3-bit binary number for each octal digit.

Step 2 : Remove any leading or trailing zeros.



$$\therefore (125.62)_8 = (1010101.11001)_2$$

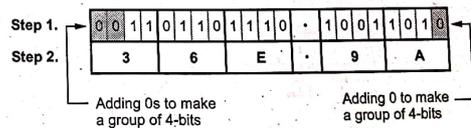
1.4.3 Binary to Hexadecimal Conversion

- The base for hexadecimal numbers is 16 and the base for binary numbers is 2.
- The base for hexadecimal number is the fourth power of the base for binary numbers. Therefore, by grouping 4 digits of binary numbers and then converting each group digit to its hexadecimal equivalent we can convert binary number to its hexadecimal equivalent.

Example 1.4.3 Convert 1101101110.1001101 to hexadecimal equivalent.

Solution :

Step 1 : Make group of 4-bits starting from LSB for integer part and MSB for fractional part, by adding 0s at the end, if required.



Step 2 : Write equivalent hexadecimal number for each group of 4-bits.

$$\therefore (1101101110.1001101)_2 = (36E.9A)_{16}$$

1.4.4 Hexadecimal to Binary Conversion

- Conversion from hexadecimal to binary is a reversal of the process explained in the previous section. Each digit of the hexadecimal number is individually converted to its binary equivalent to get hexadecimal to binary conversion of the number.

Example 1.4.4 Convert $(8A9.B4)_{16}$ to binary.

Solution :

- Step 1 :** Write equivalent 4-bit binary number of each hexadecimal digit.
- Step 2 :** Remove any leading or trailing zeros.

	8	A	9	.	B	4
Step 1.	1000	1010	1001	.	1011	0100
Step 2.	1000	1010	1001	.	1011	01

Trailing zeros

$\therefore (8A9.B4)_{16} = (1000\ 1010\ 1001.101101)_2$

1.4.5 Octal to Hexadecimal Conversion

- The easiest way to convert octal number to hexadecimal number is given below.
- 1. Convert octal number to its binary equivalent.
- 2. Convert binary number to its hexadecimal equivalent.

Example 1.4.5 Convert $(615.25)_8$ to its hexadecimal equivalent.

Solution :

- Step 1 :** Write equivalent 3-bit binary number for each octal digit.
- Step 2 :** Make group of 4-bits starting from LSB for integer part and MSB for fractional part by adding 0s at the end, if required.
- Step 3 :** Write equivalent octal number for each group to 4-bits.

	6	1	5	.	2	5
Step 1.	110	001	101	.	010	101
Step 2.	0011	0011	0011	.	0101	0100
Step 3.	1	8	D	.	5	4

Adding 0s to make a group of 4-bits

Adding 0s to make a group of 4-bits

1.4.6 Hexadecimal to Octal Conversion

- The easiest way to convert hexadecimal number to octal number is given below.
- 1. Convert hexadecimal number to its binary equivalent.
- 2. Convert binary number to its octal equivalent.

Example 1.4.6 Convert $(BC66.AF)_{16}$ to its octal equivalent.

Solution :

- Step 1 :** Write equivalent 4-bit binary number for each hexadecimal digit.
- Step 2 :** Make group of 3-bits starting from LSB for integer part and MSB for fractional part by adding 0s at the end, if required.
- Step 3 :** Write equivalent octal number for each group of 3-bits.

	B	C	6	6	.	A	F
Step 1.	1011	1100	0110	0110	.	1010	1111
Step 2.	0010	1101	1100	0110	.	1010	1111
Step 3.	1	3	6	1	.	5	3

Adding 0s to make a group of 3-bits

Adding 0 to make a group of 3-bits

1.4.7 Converting any Radix to Decimal

- In general, numbers can be represented as
- $$N = A_{n-1}r^{n-1} + A_{n-2}r^{n-2} + \dots + A_1r^1 + A_0r^0 + A_{-1}r^{-1} + A_{-2}r^{-2} + \dots + C_{-m}r^{-m}$$
- where N = Number in decimal
 A = Digit
 r = Radix or base of a number system
 n = The number of digits in the integer portion of number
 m = The number of digits in the fractional portion of number

- From this general equation we can convert number with any radix into its decimal equivalent. This is illustrated using following example.

Example 1.4.7 Convert $(3102.12)_4$ to its decimal equivalent.

Solution : $N = 3 \times 4^3 + 1 \times 4^2 + 0 \times 4^1 + 2 \times 4^0 + 1 \times 4^{-1} + 2 \times 4^{-2}$
 $= 192 + 16 + 0 + 2 + 0.25 + 0.125 = 210.375_{10}$

Example 1.4.8 Determine the value of base x, if $(193)_x = (623)_8$

Solution : $(193)_x = (623)_8$

Converting octal into decimal : $6 \times 8^2 + 2 \times 8 + 3 = (403)_{10} = (623)_8$

$\therefore (193)_x = 1 \times x^2 + 9 \times x + 3 \times x^0 = (403)_{10}$

$\therefore x^2 + 9x + 3 = 403 \quad \therefore x = 16 \text{ or } x = -25$

Negative is not applicable

$\therefore x = 16$

$\therefore (193)_{16} = (623)_8$

1.4.8 Conversion of Decimal Number to Any Radix Number

Step 1 : Convert integer part.

Step 2 : Convert fractional part.

- The conversion of integer part is accomplished by successive division method and the conversion of fractional part is accomplished by successive multiplication method.

Steps in Successive Division Method

- Divide the integer part of decimal number by desired base number, store quotient (Q) and remainder (R).
- Consider quotient as a new decimal number and repeat step 1 until quotient becomes 0.
- List the remainders in the reverse order.

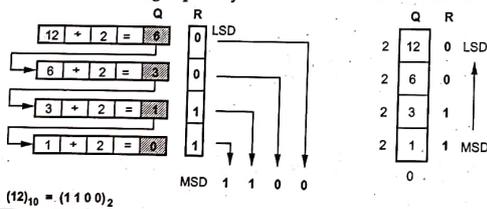
Steps in Successive Multiplication Method

- Multiply the fractional part of decimal number by desired base number.
- Record the integer part of product as carry and fractional part as new fractional part.
- Repeat steps 1 and 2 until fractional part of product becomes 0 or until you have many digits as necessary for your application.
- Read carries downwards to get desired base number.

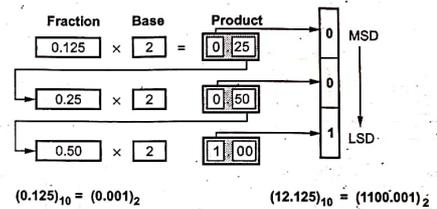
Example 1.4.9 Convert 12.125 decimal into binary.

Solution :

Integer part : Conversion of integer part by successive division method.



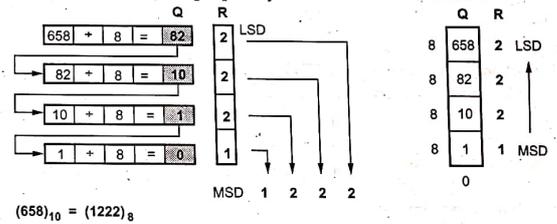
Fractional part : Conversion of fractional part by successive multiplication method.



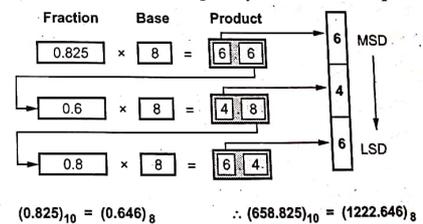
Example 1.4.10 Convert 658.825 decimal into octal.

Solution :

Integer part : Conversion of integer part by successive division method.



Fractional part : Conversion of fractional part by successive multiplication method.

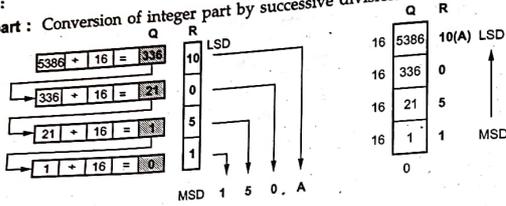


In this example, we have restricted fractional part up to 3 digits. This answer is an approximate answer. To get more accurate answer we have to continue multiplying by 8 until we have as many digits as necessary for our application.

Example 1.4.11 Convert 5386.345 decimal into hexadecimal.

Solution :

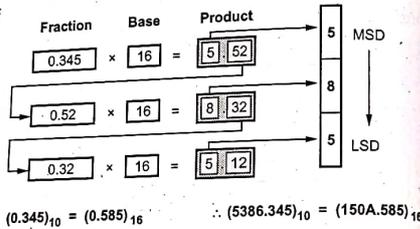
Integer part : Conversion of integer part by successive division method.



$(5386)_{10} = (150A)_{16}$

Fractional part : Conversion of fractional part by successive multiplication method.

In this example, we have restricted fractional part up to 3 digits. This answer is an approximate answer. To get more accurate answer we have to continue multiplying by 16 until we have as many digits as necessary for our application.



$(0.345)_{10} = (0.585)_{16}$ $\therefore (5386.345)_{10} = (150A.585)_{16}$

Example 1.4.12 The solution to the quadratic equation " $x^2 - 11x + 22 = 0$ " are $x = 3$ and $x = 6$. What is the base of the number system used?

Solution : Let us assume that the base is b. We have,

$(x - 3)(x - 6) = x^2 - 11x + 22$

But 3 and 6 are same in any base, whose value is more than 6.

i.e. $(3)_b = (3)_{10}$ and $(6)_b = (6)_{10}$

$\therefore (x^2 - 9x + 18)_{10} = (x^2 - 11x + 22)_b$

Comparing coefficients of x we have

$(9)_{10} = (11)_b$

$\therefore 9 = b^1 + b^0 = b^1 + 1$

$\therefore b = 8$

Comparing coefficients of x^0 we have

$(18)_{10} = (22)_b$

$\therefore 18 = 2 \times b^1 + 2 \times b^0 = 2 \times b^1 + 2$

$\therefore 16 = 2b$

$\therefore b = 8$

Example 1.4.13 Convert the base - 5 number $(4433214)_5$ directly to base - 12.

Solution : $(4433214)_5 = 4 \times 5^6 + 4 \times 5^5 + 3 \times 5^4 + 3 \times 5^3 + 2 \times 5^2 + 1 \times 5^1 + 4 \times 5^0$
 $= 4 \times 15625 + 4 \times 3125 + 3 \times 625 + 3 \times 125 + 2 \times 25 + 1 \times 5 + 4 \times 1$
 $= 62500 + 12500 + 1875 + 375 + 50 + 5 + 4$
 $= 77309$

12	77309	5
12	6442	10 → A
12	536	8
12	44	8
12	3	3
	0	

$\therefore (4433214)_5 = (388A5)_{12}$

Example 1.4.14 Convert the base - 7 number $(35614)_7$ to base - 12.

Solution : $(35614)_7 = 3 \times 7^4 + 5 \times 7^3 + 6 \times 7^2 + 1 \times 7^1 + 4 \times 7^0$
 $= 7203 + 1715 + 294 + 7 + 4$
 $= 9223$

12	9223	7
12	768	0
12	64	4
12	5	5
	0	

$\therefore (35614)_7 = (5407)_{12}$

Example 1.4.15 Convert the decimal number 250.5 to base 3, base 4, base 7 and base 16.

GTU : Dec.-12, May-12, 13, Marks 4

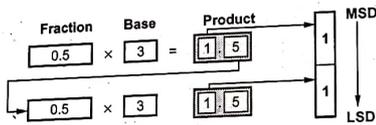
Solution : i) $(250.5)_{10} = ()_3$

Integer part :

Q	R	LSD
3	250	1
3	83	2
3	27	0
3	9	0
3	3	1
3	1	1
	0	

$\therefore (250)_{10} = (110021)_3$

Fractional part :



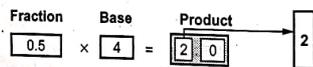
$\therefore (0.5)_{10} = (0.11)_3$
 $\therefore (250.5)_{10} = (110021.11)_3$
 ii) $(250.5)_{10} = ()_4$

Integer part :

Q	R	LSD
4	250	2
4	62	2
4	15	3
4	3	3
	0	

$\therefore (250)_{10} = (3322)_2$

Fractional part :



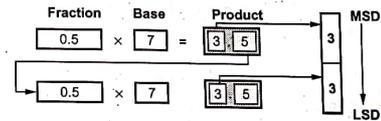
$\therefore (0.5)_{10} = (0.2)_4$
 $\therefore (250.5)_{10} = (3322.2)_4$
 iii) $(250.5)_{10} = ()_7$

Integer part :

Q	R	LSD
7	250	5
7	35	0
7	5	5
	0	

$\therefore (250)_{10} = (505)_7$

Fractional part :



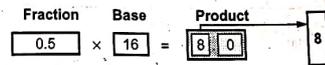
$\therefore (0.5)_{10} = (0.33)_7$
 $\therefore (250.5)_{10} = (505.33)_7$
 iv) $(250.5)_{10} = ()_{16}$

Integer part :

Q	R	LSD
16	250	10 → A
16	15	15 → F
	0	

$\therefore (250)_{10} = (FA)_{16}$

Fractional part :



$\therefore (0.5)_{10} = (0.8)_{16}$
 $\therefore (250.5)_{10} = (FA.8)_{16}$

Example 1.4.16 Convert the following numbers as directed :

- 1) $(130)_{10} = ()_2$ 2) $(1011011)_2 = ()_{10}$ **GTU : Dec.-13, Marks 7**
 3) $(1011101111)_2 = ()_8$ 4) $(110111011101110111)_2 = ()_{16}$

Solution : 1) $(130)_{10} = ()_2$

2	130	0	LSD
2	65	1	↑
2	32	0	
2	16	0	
2	8	0	
2	4	0	
2	2	0	
2	1	1	
2	0	0	

$(130)_{10} = (10000010)_2$

2) $(1011011)_2 = ()_{10}$

$N = 1 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$
 $= (91)_{10}$

$\therefore (1011011)_2 = (91)_{10}$

3) $(1011101111)_2 = ()_8$

0	0	1	0	1	1	1	0	1	1	1	1
1	3	5	7								

Binary number
Octal number

Adding 0 to make a group of 3-bits

$\therefore (1011101111)_2 = (1357)_8$

4) $(110111011101110111)_2 = ()_{16}$

0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1
3	7	7	7	B											

Adding 0 to make a group of 4-bits

$\therefore (110111011101110111)_2 = (3777B)_{16}$

Example 1.4.17 Convert the decimal number 250.5 to base 8. **GTU : Dec.-12, Marks 3**

Solution : Integer part :

	Q	R		
8	250	2	LSD	
8	31	7	↑	
8	3	3		MSD
0				

$\therefore (250)_{10} = (372)_8$

Fractional part :

Fraction	Base	Product	
0.5	8	4.0	4

$\therefore (0.5)_{10} = (0.4)_8$

$\therefore (250.5) = (372.4)_8$

Example 1.4.18 Convert following :

- 1) $(4E7.2)_{16} = ()_8$ 2) $(521.3)_8 = ()_2$ **GTU : May-14, Marks 6**

Solution : 1) $(4E7.2)_{16} = ()_8$

Step 1 : Hexadecimal to binary conversion

4	E	7	.	2	Hexadecimal number												
0	1	0	0	1	1	1	0	0	1	1	1	.	0	0	1	0	Binary number

$\therefore (4E7.2)_{16} = (010011100111.0010)_2$

Step 2 : Binary to octal conversion

0	1	0	0	1	1	1	0	0	1	1	1	.	0	0	1	0	Binary number
2	3	4	7	.	1	Octal number.											

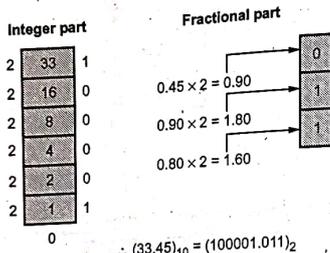
$\therefore (4E7.2)_{16} = (2347.1)_8$

2) $(521.3)_8 = ()_2$

5	2	.	1	.	3	Octal number						
1	0	1	0	1	0	0	1	.	0	1	1	Binary number

$\therefore (521.3)_8 = (101010001.011)_2$

Example 1.4.19 Convert $(33.45)_{10}$ to binary. Result should be accurate to within 0.01_{10} .
GTU : Summer-18, Marks 4



$\therefore (33.45)_{10} = (100001.011)_2$

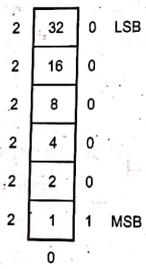
Solution : $\therefore (33.45)_{10} = (100001.011)_2$

Example 1.4.20 $(56)_{16} = (?)_{10}$ **GTU : Winter-16, Mark 1**

Solution : $(56)_{16} = 5 \times 16^1 + 6 \times 16^0 = 80 + 6 = (86)_{10}$

Example 1.4.21 $(32)_{10} = (?)_2$ **GTU : Winter-16, Mark 1**

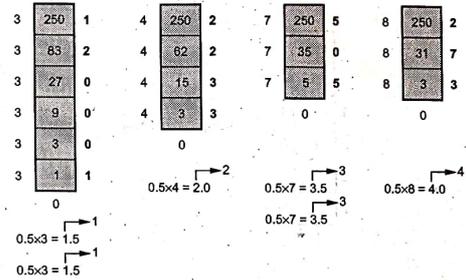
Solution :



$\therefore (32)_{10} = (100000)_2$

Example 1.4.22 Convert the decimal number 250.5 to base 3, base 4, base 7 and base 8.
GTU : Summer-17, Marks 4

Solution :



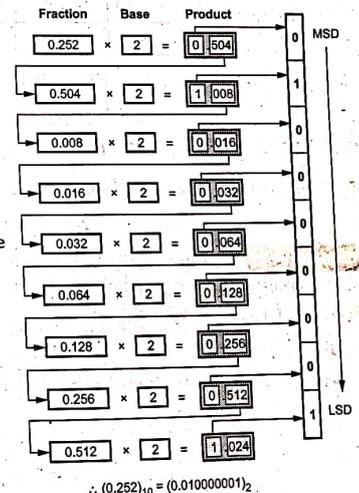
$\therefore (250.5) = (100021.11)_3 = (3322.2)_4 = (505.33)_7 = (372.4)_8$

Example 1.4.23 Convert decimal number $(0.252)_{10}$ to binary with an error less than 1%.
GTU : Winter-15, Marks 3

Solution : Error allowable is 0.01×0.252

$= 0.00252$
 $2^{-n} < 0.00252$ or $2^n > 397$
 $n = \frac{\log 397}{\log 2} = 8.63$
 $\therefore n = 8.63 = 9$
 (nearest integer)

Number of digits after decimal are nine.



$\therefore (0.252)_{10} = (0.010000001)_2$

Example 1.4.24 Convert the following numbers.

- i) $(52)_{10} = ()_2$ ii) $(436)_8 = ()_{16}$ iii) $(5C7)_{16} = ()_{10}$ iv) $(11011.101)_2 = ()_{10}$

GTU - Winter-17, Marks 4

Solution : i)

2	52	0
2	26	0
2	13	1
2	6	0
2	3	1
2	1	1
0		

$\therefore (52)_{10} = (110100)_2$

ii)

	4	3	6	Octal number								
0	0	0	1	0	0	0	1	1	1	1	0	Binary number
	1	1	E	Hex number								

$\therefore (436)_8 = (11E)_{16}$

iii) $(5C7)_{16} = 5 \times 16^2 + 12 \times 16^1 + 7 \times 16^0 = 1280 + 192 + 7 = (1479)_{10}$

iv) $(11011.101)_2 = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3}$
 $= 16 + 8 + 0 + 2 + 1 + 0.5 + 0.125 = 27.625$

Example 1.4.25 Do as directed : I. Given that $(16)_{10} = (100)_x$, find the value of x.

II. $(4433)_5 = ()_{10} = ()_2$

GTU - Summer-16, Marks 2

Solution : I. $(16)_{10} = 1 \times x^2 + 0 \times x + 0 = x^2 \therefore x = 4.$

II)

$(4433)_5 = 4 \times 5^3 + 4 \times 5^2 + 3 \times 5^1 + 3 \times 5^0 = 500 + 100 + 15 + 3 = (618)_{10}$

2	618	0	LSD
2	309	1	
2	154	0	
2	77	1	
2	38	0	
2	19	1	
2	9	1	
2	4	0	
2	2	0	
2	1	1	MSD
0			

$\therefore (618)_{10} = (1001101010)_2$

Example 1.4.26 Do as directed : $(1011011101101110)_2 = ()_{16}$ GTU - Summer-16, Mark 1

Solution : $\frac{1011}{B} \frac{0111}{7} \frac{0110}{6} \frac{1110}{E}$

$\therefore (1011011101101110)_2 = (B76E)_{16}$

1.5 Complement of Numbers

- In this section, we see the complement numbers used in different number systems. These complement numbers are used in case of subtraction of two numbers in corresponding number systems.

1.5.1 1's Complement Representation

- The 1's complement of a binary number is the number that results when we change all 1's to zeros and the zeros to ones.

Example 1.5.1 Find 1's complement of $(11010100)_2$.

Solution :

1	1	0	1	0	1	0	0	Number
↓	↓	↓	↓	↓	↓	↓	↓	NOT operation
0	0	1	0	1	0	1	1	1's complement of number

1.5.2 2's Complement Representation

- The 2's complement is the binary number that results when we add 1 to the 1's complement. It is given as,

2's complement = 1's complement + 1

- The 2's complement form is used to represent negative numbers.

Example 1.5.2 Find 2's complement of $(11000100)_2$.

Solution :

1	1	0	0	0	1	0	0	Number
					1	1		Carry
0	0	1	1	1	0	1	1	1's complement of number
							1	Add 1
0	0	1	1	1	1	0	0	2's complement of number

Example 1.5.3 Represent the decimal number -200 and 200 using 2's complement binary form.

Solution : To represent 200 and -200 we need 9-bit number system.

+200	=	0	1	1	0	0	1	0	0	0	
-200	=	1	0	0	1	1	0	1	1	1	1's complement
										1	Add 1
		1	0	0	1	1	0	0	0	0	2's complement

Fig. 1.5.1

1.6 Signed Binary Numbers

- In practice, we use plus sign to represent positive number and minus sign to represent negative number.
- However, because of hardware limitations, in computers, both positive and negative numbers are represented with only binary digits.
- The leftmost bit (sign bit) in the number represents sign of the number.
- The sign bit is 0 for positive numbers and it is 1 for negative numbers.
- Fig. 1.6.1 shows the sign magnitude format for 8-bit signed number.
- Here are some examples of sign-magnitude numbers.

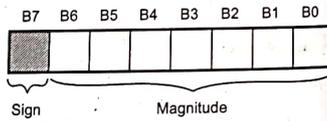


Fig. 1.6.1

- + 6 = 0000 0110
- 14 = 1000 1110
- + 24 = 0001 1000
- 64 = 1100 0000

Maximum positive number : $0\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 = +127$
 Maximum negative number : $1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 = -127$

- Let us see how -6 is represented in these three formats. Consider the number 6 represented in binary with eight bits.

Signed-magnitude representation :	1	0	0	0	1	1	0
Signed-1's complement representation :	1	1	1	1	0	0	1
Signed-2's complement representation :	1	1	1	1	0	1	0

- In signed-magnitude, -6 is obtained from +6 by changing the sign bit in the leftmost position from 0 to 1. In signed-1's complement, -6 is obtained by complementing all the bits of +6, including the sign bit. The signed-2's complement representation of -6 is obtained by taking 2's complement of positive number, including the sign bit.

Decimal	Signed-2's complement	Signed-1's complement	Signed magnitude
+7	0111	0111	0111
+6	0110	0110	0110
+5	0101	0101	0101
+4	0100	0100	0100
+3	0011	0011	0011
+2	0010	0010	0010
+1	0001	0001	0001
+0	0000	0000	0000
-0	-	1111	1000
-1	1111	1110	1001
-2	1110	1101	1010
-3	1101	1100	1011
-4	1100	1011	1100
-5	1011	1010	1101
-6	1010	1001	1110
-7	1001	1000	1111
-8	1000	-	-

Table 1.6.1

- The Table 1.6.1 lists all possible 4-bit signed binary numbers in the three representations. Looking at the Table 1.6.1 we understand following points :
 - Positive numbers in all three representations are identical and have 0 in the leftmost position.
 - All negative numbers have a 1 in the leftmost bit position.
 - The signed-2's complement system has only one representation for 0, which is always positive.
 - The signed-magnitude and 1's complement systems have either a positive 0 or a negative 0.
- With four bits, we can represent 16 binary numbers.
- The sign-magnitude representation requires separate handling for sign and magnitude during arithmetic operations and hence it is suitable in computer arithmetic. Therefore, the signed complement numbers are normally used in computer arithmetic. The 1's complement imposes some difficulties and is seldom used for arithmetic operations. It is used as a logical operation since the change of 1 to 0 or 0 to 1 is equivalent to a logical complement operation. The signed-2's complement system is commonly used in computer arithmetic.

Example 1.6.1 Represent numbers +9 and -9 signed-magnitude, signed 1's complement and signed 2's complement 8-bit form.

Solution : Signed magnitude representation of a number :

In this representation most significant bit is used to code sign of a number (1 = negative, 0 = +ve) and remaining bits are used to represent magnitude with 'n' bit representation, number represented will be from $+2^{n-1}$ to -2^{n-1} .

Number	Signed magnitude representation	1's complement representation	2's complement representation
+9	0000 1001	0000 1001	0000 1001
-9	1000 1001	1111 0110	1111 0111

Example 1.6.2 Represent decimal number "-13" in all three methods of negative binary number representation using eight bits.

Solution :

1 0 0 0 0 1 1 0 1 1 -13 in sign magnitude representation

1 1 1 1 1 0 0 1 0 1 0 -13 in 1's complement representation

1 1 1 1 1 0 0 1 1 1 -13 in 2's complement representation

Example for Practice

Example 1.6.3 : Write the sign-magnitude, 1's complement and 2's complement forms of -36 in a 8-bit number system [Ans. : Sign-magnitude: 10100100
1's complement: 11011011, 2's complement: 11011100]

Review Questions

1. What are 1's complement and 2's complement numbers ?
2. State advantages of 2's complement number representation.
3. State the different ways for representing the signed binary numbers.

1.7 Binary Arithmetic

GTU : May-13, Summer-15, Winter-17

1.7.1 Binary Addition

- The addition consists of four possible elementary operations, as shown in Table 1.7.1.

- The first three operations produce a sum whose length is one digit, but when the last operation is performed sum is two digits.
- The higher significant bit of this result is called a carry and lower significant bit is called sum.
- Such an operation is known as half addition.
- The operation which performs addition of three bits (two significant bits and a previous carry) is called a full addition.
- The Table 1.7.2 shows the truth table for full addition.

Sr. No.	Operations
0.	0 + 0 = 0
1.	0 + 1 = 1
2.	1 + 0 = 1
3.	1 + 1 = 10 ₂

Table 1.7.1 Addition operations

Addition Method

1. Add bits column-wise starting from LSB with carry if any.
2. Put the sum at the bottom of the same column.
3. Put the carry, if any, on the top of next column.

Inputs			Outputs	
A	B	C _{in}	C _{out}	Sum (S)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1.7.2 Truth table for full-adder

Example 1.7.1 Perform addition of (11001100)₂ and (11011010)₂.

Solution : In the above example, we have seen the addition of two unsigned binary numbers. In case of the signed numbers, we have to consider the sign of the number and we may require sign extension to avoid possible overflow.

1	1	1	1	0	0	1	1	0	0	Carry
1	1	0	0	1	1	0	1	0	0	Number 1
1	1	0	1	1	0	1	0	1	0	Number 2
1	1	0	1	0	0	1	1	0		Result (S)

Example 1.7.2 Add (28)₁₀ and (15)₁₀ by converting them into binary.

Solution : Using decimal to binary conversion technique discussed in section 1.4.8 we have,

Sign Extension	+	0	0	1	1	1	0	0	0	Carry	(28) ₁₀
Sign	+	0	0	0	1	1	1	1		Binary equivalent of (28) ₁₀	+ (15) ₁₀
		0	1	0	1	0	1	1		Binary equivalent of (15) ₁₀	(43) ₁₀
		0	1	0	1	0	1	1		Result : Binary equivalent of (43) ₁₀	

(28)₁₀ = (011100)₂ and (15)₁₀ = (01111)₂

- If carry is generated then the result is positive and in the true form. In this case, carry is ignored.
- If carry is not generated then the result is negative and in the 2's complement form.

Example 1.7.6 Perform $(28)_{10} - (15)_{10}$ using 6-bit 2's complement representation.

Solution : $(28)_{10} = (011100)_2$

$(15)_{10} = (001111)_2$

	0	0	1	1	1	1	
	0	0	1	1	1	1	
+	1	1	0	0	0	0	1
	1	1	0	0	0	0	1
							1

	1	1					
	0	1	1	1	0	0	
+	1	1	0	0	0	0	1
	1	1	0	0	0	0	1
							1

Example 1.7.7 Perform $(15)_{10} - (28)_{10}$ using 6-bit 2's complement representation.

Solution : $(15)_{10} = (001111)_2$

$(28)_{10} = (011100)_2$

	0	1	1	1	0	0	
	0	1	1	1	0	0	
+	1	0	0	0	1	1	1
	1	0	0	1	0	0	
							1

	0	1	1				
	0	0	1	1	1	1	
+	1	0	0	1	0	0	
	1	1	0	0	1	1	
							1

	0	0	1	1	0	0	
	0	0	1	1	0	0	
+	0	0	1	1	0	0	1
	0	0	1	1	0	0	1
							1

Example 1.7.8 Perform the following subtraction using 2's complement method:
 i) $01000 - 01001$
 ii) $00111001 - 00011110$

Solution : i) $01000 - 01001$

	0	1	0	0	1	
	1	0	1	1	0	
+	1	0	1	1	1	1
	1	0	1	1	1	1
						1

	0	1	0	0	0	
	1	0	1	1	1	
+	1	1	1	1	1	1
	1	1	1	1	1	1
						1

ii) $00111001 - 00011110$

	0	0	0	1	1	0	0	1
	1	1	1	0	0	0	0	1
+	1	1	1	0	0	0	0	1
	1	1	1	0	0	0	0	1
								1

	1	1	1				
	0	0	1	1	1	0	0
+	1	1	1	0	0	0	1
	0	0	0	1	1	0	1
							1

Example 1.7.9 Perform following arithmetic operation in binary using signed 2's complement representation : $(-42) - (-13)$

Solution : $-42 - (-13) = -42 + 13$

$(+13)_{10} = (0001101)_2$
 $(+42)_{10} = (0101010)_2$

	0	1	0	1	0	1	0
	1	0	1	0	1	0	1
+	1	0	1	0	1	0	1
	1	0	1	0	1	0	1
							1

	0	0	0	1	1	0	1
	1	0	1	0	1	1	0
+	1	1	0	0	0	1	1
	1	1	0	0	0	1	1
							1

Example 1.7.10 Perform the subtraction with the following decimal numbers using 1's complement and 2's complements.

GTU : May-13, Marks 7

a) 11010 - 1101 b) 10010 - 10011. Solution : It is assumed that given numbers are signed numbers.

a) 11010 - 1101

Subtraction using 1's complement

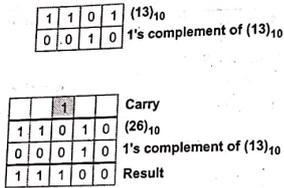


Fig. 1.7.1

There is no end around carry. Therefore, the answer is, - (1's complement of 11100) = - (00011)

Subtraction using 2's complement

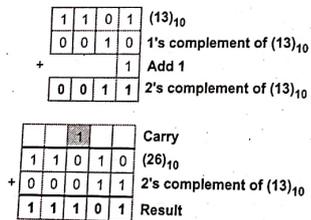


Fig. 1.7.2

There is no end carry. Therefore, the answer is, - (2's complement of 11101) = - (00011)

b) 10010 - 10011

Subtraction using 1's complement

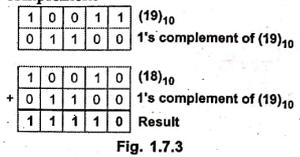


Fig. 1.7.3

There is no end carry. Therefore, the answer is, - (1's complement of 11110) = - (00001)

Subtraction using 2's complement

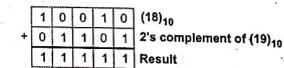
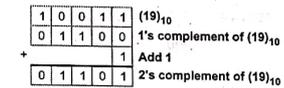


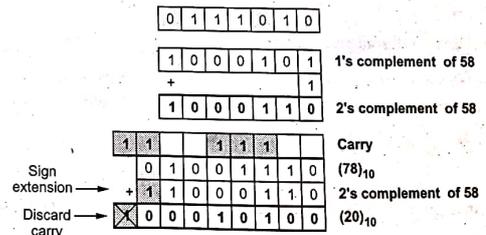
Fig. 1.7.4

There is no end carry. Therefore, the answer is, - (2's complement of 11111) = - (00001)

Example 1.7.11 Perform subtraction of (78)₁₀ - (58)₁₀ using 2's complement method.

GTU : Summer-15, Marks 3

Solution : (78)₁₀ = (01001110)₂
(58)₁₀ = (0111010)₂



Example 1.7.12 Perform following subtraction using 2's complement method.

GTU : Winter-17, Marks 3

$(11010)_2 - (10000)_2$

Solution :

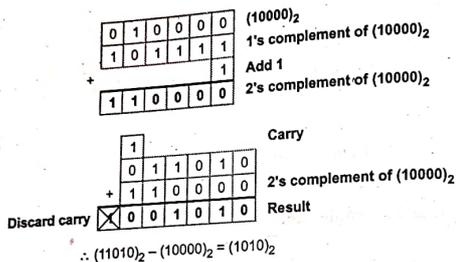


Fig. 1.7.5

1.8 Octal Arithmetic

GTU : Summer-16

1.8.1 Octal Addition

- The sum of two octal digits is the same as their decimal sum, provided the decimal sum is less than 8. If the decimal sum is 8 or greater, subtract 8 to obtain the octal digit.
- A carry of 1 is produced when the decimal sum is corrected this way, as illustrated in the following examples.

Example 1.8.1 a) $4_8 + 2_8$ b) $6_8 + 7_8$ c) $1_8 + 7_8$

Solution : a) $4_8 + 2_8 = (6)_8$

b) $6_8 + 7_8 = (13 - 8)_8$ carry 1

c) $1_8 + 7_8 = (8 - 8)_8$ carry 1

Note Subscript 8 denotes it is an octal number.

- To obtain the sum of multi-digit octal numbers, the procedure just described is applied to each column of digits as illustrated in the following example.

Example 1.8.2 Add $(167)_8$ and $(325)_8$.

Solution :

- If the decimal sum of several octal digits is 16 or greater, subtract 16 and set carry equal to 2.

- In general, we can express any decimal sum in octal by repeatedly subtracting 8 until the result is one of the octal digits through 0 to 7.
- Each time 8 is subtracted, the amount of the carry is increased by 1. This procedure is illustrated in the following example.

1	1	
1	6	7
3	2	5
5	(9-8)	(12-8)
5	1	4

Carry
Number 1
Number 2
When sum is > 8,
Sum = Sum - 8, Carry = 1
Result

Example 1.8.3 Add the octal numbers $(341)_8$, $(125)_8$, $(472)_8$ and $(577)_8$

Solution :

1	2	1	
	3	4	1
	1	2	5
	4	7	2
	5	7	7
1	(15-8)	(21-16)	(15-8)
1	7	5	7

Carry
 $(341)_8$
 $(125)_8$
 $(472)_8$
 $(577)_8$
Result

$\therefore (341)_8 + (125)_8 + (472)_8 + (577)_8 = (1757)_8$

1.8.2 Octal Subtraction using 8's Complement

- We have seen how binary subtraction is performed using 2's complement method. Similarly, octal subtraction is performed using 8's complement method.
- The 8's complement of an octal number is found by adding a 1 to the least significant bit of the 7's complement of an octal number, as illustrated in the Example 1.8.2.

Example 1.8.4 Find the 8's complement of $(346)_8$.

Solution :

- Step 1 :** Subtract each digit of a number from 7 to get the 7's complement of the number.

	7	7	7
-	3	4	6
	4	3	1
+		1	
	4	3	2

$(346)_8$
7's complement of $(346)_8$
Add 1
8's complement of $(346)_8$

Step 2 : Add 1 to it to get the 8's complement of the number.
The steps for octal subtraction using 8's complement method are as given below :

Step 1 : Find 8's complement of subtrahend.

Step 2 : Add two octal numbers (first number and 8's complement of the second number).

Step 3 : If carry is produced in the addition it is ignored; otherwise find 8's complement of the sum as a result with negative sign.

Example 1.8.5 Use 8's complement method of subtraction to compute $(516)_8 - (413)_8$.

Solution :

Step 1:

7	7	7
4	1	3
3	6	4
		1
3	6	5

(413)₈
7's complement of (413)₈
Add 1
8's complement of (413)₈

Step 2:

1	1	1
	5	1
	3	6
1	(9-8)	(8-8)
1	0	3
	1	0

Carry (516)₈
8's complement of (413)₈
Ignore carry →
Result

Step 3:

	1	0	3
--	---	---	---

$\therefore (516)_8 - (413)_8 = (103)_8$

Example 1.8.6 Use the 8's complement method of subtraction to compute $316_8 - 451_8$.

Solution :

Step 1:

7	7	7
4	5	1
3	2	6
		1
3	2	7

(451)₈
7's complement of (451)₈
Add 1
8's complement of (451)₈

Step 2:

	1	
3	1	6
3	2	7
6	4	(13-8)
6	4	5

Carry (316)₈
8's complement of (451)₈
Result

Step 3 : No carry, hence take 8's complement

7	7	7
6	4	5
1	3	2
		1
1	3	3

7's complement of result
Add 1
8's complement of (645)₈

$\therefore (316)_8 - (451)_8 \rightarrow (-133)_8$

Example 1.8.7 1. Subtract $(45)_8$ from $(66)_8$.

GTU : Summer-16, Mark 1

Solution : Let us perform octal subtraction using 8' complement

8's complement of 45 = $77 - 45 + 1 = 33$

$\therefore (66)_8 - (45)_8 = (21)_8$

1	1	
	6	6
+	3	3
	(10-8)	(9-8)
Ignore carry	2	1

Carry
8's complement of 45
Result
 $\therefore (66)_8 - (45)_8 = (21)_8$

Fig. 1.8.1

1.9 Hexadecimal Arithmetic

GTU : Summer-16

1.9.1 Hexadecimal Addition

- The sum of two hexadecimal digits is the same as their equivalent decimal sum (with any sum from 10 through 16 is expressed a letter from A through F), provided the decimal equivalent is less than 16.
- If the decimal sum is 16 or greater, subtract 16 to obtain the hexadecimal digit.
- A carry of 1 is produced when the decimal sum is corrected this way, as illustrated in the following examples.

Example 1.9.1 a) $3_{16} + 9_{16}$ b) $9_{16} + 7_{16}$ c) $A_{16} + 8_{16}$.

Solution : a) $3_{16} + 9_{16} = C_{16}$

b) $9_{16} + 7_{16} = (16 - 16) \quad 0_{16} \text{ carry } 1 = (10)_{16}$

c) $A_{16} + 8_{16} = (18 - 16) \quad 2_{16} \text{ carry } 1 = (12)_{16}$

Note Sometimes instead of subscript 16, subscript H is used to denote the hexadecimal number.

- To obtain the sum of multi-digit hexadecimal numbers, the procedure just described is applied to each column of digits as illustrated in the following example.

Example 1.9.2 Add $3F8_{16}$ and $5B3_{16}$

Solution :

- If the decimal sum of several hex digits is 32 or greater, subtract 32 and set carry equal to 2.

1			
3	F	8	
5	B	3	
9	(26-16)	B	
9	A	B	

Carry
(3F8)₁₆
(5B3)₁₆

When Sum > 16, Sum = Sum - 16, Carry = 1

- In general, we can express any decimal sum in hexadecimal form by repeatedly subtracting 16 until the result is one of the hex digits through 0 to F.
- Each time 16 is subtracted the amount of the carry is increased by 1.

Example 1.9.3 Add the hexadecimal numbers $(892)_{16}$, $(58F)_{16}$, $(178)_{16}$ and $(48E)_{16}$.

Solution :

1	2	2	
8	9	2	
5	8	F	
1	7	8	
4	8	E	
1	(20-16)	(34-32)	(39-32)
1	4	2	7

Carry
(892)₁₆
(58F)₁₆
(178)₁₆
(48E)₁₆
Result

$\therefore (892)_{16} + (58F)_{16} + (178)_{16} + (48E)_{16} = (1427)_{16}$

Example 1.9.4 Do as directed : Add $(6E)_{16}$ and $(C5)_{16}$

GTU - Summer-16, Marks 4

Solution :

1	1	
6	E	
+	C	5
	(19-16)	(19-16)
1	3	3

Carry

$\therefore (6E)_{16} + (C5)_{16} = (133)_{16}$

Fig. 1.9.1

1.9.2 Hexadecimal Subtraction using 16's Complement

- Hexadecimal subtraction is best accomplished using the 16's complement method like 2's complement for binary subtraction.
- The 16's complement of a hexadecimal number is found by adding a 1 to the least significant bit of the 15's complement of a hexadecimal number, as illustrated in the example 1.8.4.

Example 1.9.5 Find the 16's complement of $(ABC)_{16}$.

Solution :

Step 1 : Subtract each digit of a number from 15 to get the 15's complement of the number.

Step 2 : Add 1 to it to get the 16's complement of the number.

15	15	15
A	8	C
5	7	3
		1
5	7	4

(ABC)₁₆

15's complement of (ABC)₁₆

Add 1

16's complement of (ABC)₁₆

- The steps for hexadecimal subtraction using 16's complement method are as given follows.

Step 1 : Find 16's complement of subtrahend.

Step 2 : Add two hexadecimal numbers (first number and 16's complement of the second number).

Step 3 : If carry is produced in the addition it is discarded; otherwise find 16's complement of the sum as a result with negative sign.

Example 1.9.6 Use the 16's complement method of subtraction to compute $CB2_{16} - 972_{16}$.

Solution :

Step 1 :

15	15	15
9	7	2
6	8	D
		1
6	8	E

(972)₁₆

15's complement of (972)₁₆

Add 1

16's complement of (972)₁₆

Step 2 :

1	1	1	
	C	B	2
+	6	8	E
	(19-16)	(20-16)	(16-16)
	3	4	0

Carry

(CB2)₁₆

16's complement of (972)₁₆

Ignore carry

Step 3 :

Result

$\therefore (CB2)_{16} - (972)_{16} \rightarrow (340)_{16}$

Example 1.9.7 Use the 16's complement method of subtraction to compute $3B7_{16} - 854_{16}$.

Solution :

Step 1:

15	15	15
8	5	4
7	A	B
7	A	C

15's complement of $(854)_{16}$
Add 1
16's complement of $(854)_{16}$

Step 2:

1	1	Carry
3	B	7
7	A	C
B	6	3

$(3B7)_{16}$
16's complement of $(854)_{16}$
Result

Step 3: No carry, hence take 16's complement

15	15	15
B	6	3
4	9	C
4	9	D

15's complement of result
Add 1
16's complement of result

$\therefore (3B7)_{16} - (854)_{16} \rightarrow (-49D)_{16}$

Examples for Practice

- Example 1.9.8:** Perform addition of $(FA6)_{16}$ and $(BC4)_{16}$ [Ans. : $(1B6A)_{16}$]
- Example 1.9.9:** Perform $(E8D)_{16} - (1F8)_{16}$ [Ans. : $(C95)_{16}$]
- Example 1.9.10:** Perform addition of $(1A6)_{16}$ and $(474)_8$ [Ans. : $(2E2)_{16}$]
- Example 1.9.11:** Perform $(E8D)_{16} - (10101010)_2$ [Ans. : $(DE3)_{16}$]
- Example 1.9.12:** Add the following numbers : $(ABC)_{16} + (CDE)_{16}$ [Ans. : $(179A)_{16}$]

1.10 Binary Codes

GTU : May-14, Summer-15, 16, 18, Winter-16

- When numbers, alphabets or words are represented by a specific group of symbols, we can say that they are encoded.
- The group of symbols used to encode them are called codes. The digital data is represented, stored and transmitted as groups of binary digits (bits).
- The group of bits, also known as binary code, represent both numbers and letters of the alphabets as well as many special characters and control functions. They are classified as numeric or alphanumeric.
- Numeric codes are used to represent numbers.
- Alphanumeric codes are used to represent characters : alphabetic letters and numerals.

1.10.1 Classification of Binary Codes

- The Fig. 1.10.1 shows the classification of codes.

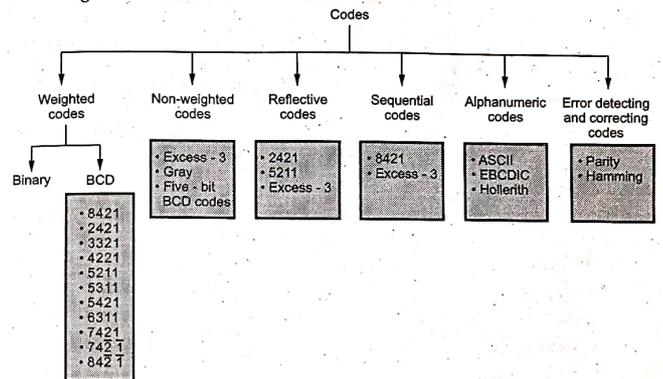


Fig. 1.10.1 Classification of codes

- The codes are broadly classified as
 1. Weighted codes
 2. Non-weighted codes
 3. Reflective codes
 4. Sequential codes
 5. Alphanumeric codes
 6. Error detecting and correcting codes.

Weighted codes

- In weighted codes, each digit position of the number represents a specific weight.
- For example, in decimal code, if number is 567 then weight of 5 is 100, weight of 6 is 10 and weight of 7 is 1.
- In weighted binary code each bit has a weight 8, 4, 2 or 1 and each decimal digit is represented by a group of four bits, as shown in the Fig. 1.10.2 (a).

Non-weighted codes

- Non-weighted codes are not assigned with any weight to each digit position, i.e., each digit position within the number is not assigned fixed value.
- Excess-3 and gray codes are the non-weighted codes.

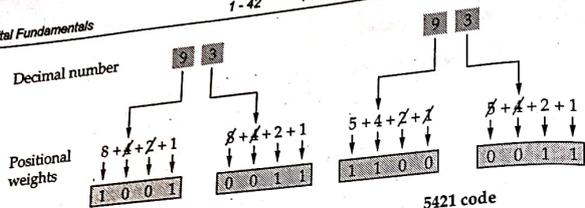


Fig. 1.10.2 (a) Weighted codes

Reflective codes

- A code is said to be reflective when the code for 9 is the complement for 0, the code for 8 is complement for 1, 7 for 2, 6 for 3 and 5 for 4. This is illustrated in Fig. 1.10.2 (b).

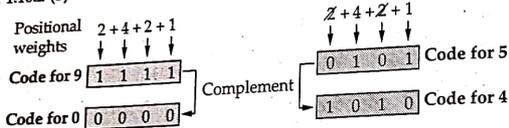


Fig. 1.10.2 (b) Reflective codes

- Like 2421, codes 5211 and excess-3 are also reflective. The 8421 code is not reflective.
- Reflectivity is desirable in a code when the nine's complement must be found, such as in nine's complement subtraction.

Sequential codes

- In sequential codes each succeeding code is one binary number greater than its preceding code.
- This greatly aids mathematical manipulation of data.
- The 8421 and excess-3 are sequential, whereas the 2421 and 5211 codes are not.

Alphanumeric codes

- The codes which consists of both numbers and alphabetic characters are called alphanumeric codes.
- Most of these codes, however, also represent symbols and various instructions necessary for conveying intelligible information.
- The most commonly used alphanumeric codes are : ASCII (American Standard Code for Information Interchange), EBCDIC (Extended Binary Coded Decimal Interchange Code) and Hollerith code.

Error detecting and correcting codes

- When the digital information in the binary form is transmitted from one circuit or system to another circuit or system an error may occur. This means a signal corresponding to 0 may change to 1 or vice versa due to presence of noise.
- To maintain the data integrity between transmitter and receiver, extra bit or more than one bit are added in the data.
- These extra bits allow the detection and sometimes correction of error in the data.
- The data along with the extra bit/bits forms the code. Codes which allow only error detection are called error detecting codes and codes which allow error detection and correction are called error detecting and correcting codes.

1.10.2 BCD (Binary Coded Decimal) Codes

- BCD is an abbreviation for binary coded decimal.
- BCD is a numeric code in which each digit of a decimal number is represented by a separate group of 4-bits. The most common BCD code is 8-4-2-1 BCD.
- It is called 8-4-2-1 BCD because the weights associated with 4 bits are 8-4-2-1 from left to right. This means that, bit-3 has weight 8, bit-2 has weight 4 bit-1 has weight 2 and bit-0 has weight 1.
- The Table 1.10.1 shows the 4-bit 8-4-2-1 BCD code used to represent a single decimal digit.

Decimal	BCD code			
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table 1.10.1 8-4-2-1 BCD code

In multidigit coding, each decimal digit is individually coded with 8-4-2-1 BCD code, as shown in the Fig. 1.10.3. Total 8-bits are required to encode 58₁₀ in 8-4-2-1 BCD.

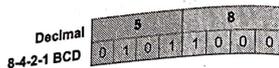


Fig. 1.10.3

Advantage

- 1. Easy to convert between it and decimal.

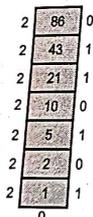
Disadvantages

- 1. Since it requires more binary digits to represent multi-digit number than binary number system. It is less efficient. For example, to represent the same number (58) in binary: 111010₂, we require only 6 digits.
- 2. Arithmetic operations are more complex.

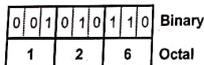
Example 1.10.1 Convert 10000 0110 (BCD) to decimal, binary and octal.

GTU : Summer-18, Marks 3

Solution : (1000 0110)_{BCD} = (86)₁₀



$\therefore (86)_{10} = (1010110)_2$



$\therefore (86)_{10} = (1010110)_2 = (126)_8$

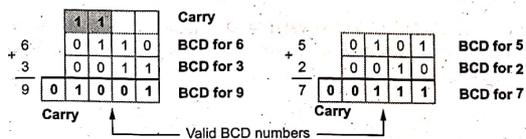
Fig. 1.10.4

1.10.2.1 BCD Addition

The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added.

Case 1 : Sum equals 9 or less with carry 0

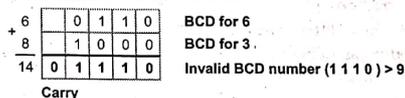
Let us consider additions of 3 and 6 in BCD.



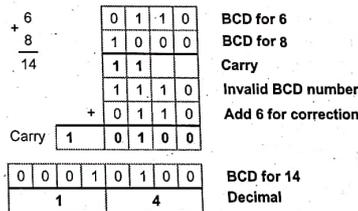
- The addition is carried out as in normal binary addition and the sums are 1 0 0 1 and 0 1 1 1 which are valid BCD codes.

Case 2 : Sum greater than 9 with carry 0

- Let us consider addition of 6 and 8 in BCD.



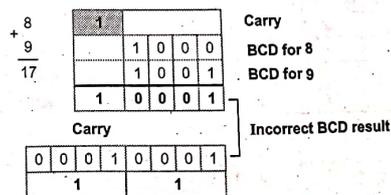
- The sum 1 1 1 0 is an invalid BCD number. This has occurred because the sum of the two digits exceeds 9. Whenever this occurs the sum has to be corrected by the addition of six (0110) in the invalid BCD number, as shown follows.



- After addition of 6 carry is produced into the second decimal position.

Case 3 : Sum equals 9 or less with carry 1

- Let us consider addition of 8 and 9 in BCD.



Solution :

983 =	1	0	0	1	1	0	0	0	0	1	1	BCD for 983
748 =	0	1	1	1	0	1	0	0	1	0	0	BCD for 748
-748 =	0	0	1	0	0	1	0	1	0	0	0	9's complement of 748

983	1	0	0	1	1	0	0	0	0	1	1	BCD for 983
+ 748	0	0	1	0	0	1	0	1	0	0	0	9's complement of 748
235	1	0	1	1	1	1	0	1	0	1	0	Add 660
	0	1	1	0	0	1	1	0	0	0	0	Add end around carry
	1	0	0	1	0	0	0	1	1	0	1	BCD for 235

Example 1.10.11 Perform the following arithmetic operations in BCD numbers :
893 - 647.

Solution :

893 =	1	0	0	0	1	0	0	1	0	0	1	1	BCD for 893
-647 =	0	1	1	0	0	1	0	0	0	1	1	1	BCD for 647
246	0	0	1	1	0	1	0	1	0	0	1	0	9's complement of 647

893	1	0	0	0	1	0	0	1	0	0	1	1	BCD for 893
+ 647	0	0	1	1	0	1	0	1	0	0	1	0	9's complement of 647
					1		1						Add 660
	1	0	1	1	1	1	1	0	0	1	0	1	Add end around carry
	0	1	1	0	0	1	1	0	0	0	0	0	BCD for 246

1.10.23 BCD Subtraction using 10's Complement Method

- Subtraction of BCD numbers can also be performed by representing negative numbers in the 10's complement form.
- The 10's complement of a decimal number is equal to the 9's complement plus 1.

Example 1.10.12 Find the 10's complement of (3497)_{BCD}.

Solution :

Steps for subtraction of BCD numbers using 10's complement method

9	9	9	9	(3497) _{BCD}
3	4	9	7	9's complement of (3497) _{BCD}
6	5	0	2	Add 1
6	5	0	3	10's complement of (3497) _{BCD}

- Step 1 : Find the 10's complement of a negative number.
- Step 2 : Add two numbers using BCD addition (Minuend + 10's complement of subtrahend).
- Step 3 : If carry is not generated result is negative and find the 10's complement of the result, otherwise result is positive and discard carry.

Example 1.10.13 Find the 10's complement of the following :

- 1) (935)₁₁
- 2) (6106)₁₀

GTU : Winter-16. Marks 4

Solution : 1) $(935)_{11} = 9 \times 11^2 + 3 \times 11^1 + 5 \times 11^0 = 1089 + 33 + 5 = (1127)_{10}$
 $9999 - 1127 + 1 = 8873$... 10's complement of (935)₁₁
 2) $9999 - 6106 + 1 = 3894$... 10's complement of (6106)₁₀

Example 1.10.14 Perform $(46)_{10} - (22)_{10}$ in BCD using 10's complement.

Solution :

- Step 1 : Find 10's complement of 22.
 $10's \text{ complement of } 22 = 9's \text{ complement of } 22 + 1$
 $= (99 - 22) + 1 = 78$

Step 2 : Add 46 and 10's complement of 22.

	+	46	+	0	1	0	0	0	1	1	0	Carry
		-22	+	0	1	1	1	1	0	0	0	(46) _{BCD}
		24		1	0	1	1	1	1	1	0	(78) 10's complement of (22) _{BCD}
				1	1	1	1	1	1	1		Carry
				1	0	1	1	1	1	1	0	Invalid BCD numbers
				0	1	1	0	0	1	1	0	Add 6 in each digit
Discard carry	⊗			0	0	1	0	0	1	0	0	Result

Example 1.10.18 Represent $(7)_{10}$ using all the weighted 4-bit BCD codes listed in the Table 1.10.5.

Solution :

1. 3321 code

$$(7)_{10} = \begin{matrix} 3 & + & 3 & + & 2 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 1 & 0 & 1 & & & \\ \hline & & 1 & 1 & 0 & 1 & \end{matrix} = (1101)_{3321 \text{ BCD}}$$

2. 4221 code

$$(7)_{10} = \begin{matrix} 4 & + & 2 & + & 2 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 0 & 1 & 1 & & & \\ \hline & & 1 & 0 & 1 & 1 & \end{matrix} = (1011)_{4221 \text{ BCD}}$$

3. 5211 code

$$(7)_{10} = \begin{matrix} 5 & + & 2 & + & 1 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 1 & 0 & 0 & & & \\ \hline & & 1 & 1 & 0 & 0 & \end{matrix} = (1100)_{5211 \text{ BCD}}$$

4. 5311 code

$$(7)_{10} = \begin{matrix} 5 & + & 3 & + & 1 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 0 & 1 & 1 & & & \\ \hline & & 1 & 0 & 1 & 1 & \end{matrix} = (1011)_{5311 \text{ BCD}}$$

5. 5421 code

$$(7)_{10} = \begin{matrix} 5 & + & 4 & + & 2 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 0 & 1 & 0 & & & \\ \hline & & 1 & 0 & 1 & 0 & \end{matrix} = (1010)_{5421 \text{ BCD}}$$

6. 6311 code

$$(7)_{10} = \begin{matrix} 6 & + & 3 & + & 1 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 0 & 0 & 1 & & & \\ \hline & & 1 & 0 & 0 & 1 & \end{matrix} = (1001)_{6311 \text{ BCD}}$$

7. 7421 code

$$(7)_{10} = \begin{matrix} 7 & + & 4 & + & 2 & + & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 0 & 0 & 0 & & & \\ \hline & & 1 & 0 & 0 & 0 & \end{matrix} = (1000)_{7421 \text{ BCD}}$$

8. 7 4 2 1 code

$$(7)_{10} = \begin{matrix} 7 & + & 4 & - & 2 & - & 1 \\ \downarrow & & \downarrow & & \downarrow & & \downarrow \\ 1 & 0 & 0 & 0 & & & \\ \hline & & 1 & 0 & 0 & 0 & \end{matrix} = (1000)_{7421 \text{ BCD}}$$

Example for Practice

Example 1.10.19 : Represent the decimal number 6 in $842\bar{1}$ and 2421 codes.

[Ans. : 1010, 1100]

1.10.4 Excess-3 Code

- The excess-3 code can be derived from the natural BCD code by adding 3 to each coded number.
- For example, decimal 12 can be represented in BCD as 0001 0010. Now adding 3 to each digit we get Excess-3 code as 0100 0101 (12 in decimal). It is a non-weighted code.

- Table 1.10.6 shows excess-3 codes to represent single decimal digit. It is sequential code because we get any code word by adding binary 1 to its previous code word as shown in the Table 1.10.6.

Decimal digit	Excess-3 code
0	0 0 1 1
1	0 1 0 0
2	0 1 0 1
3	0 1 1 0
4	0 1 1 1
5	1 0 0 0
6	1 0 0 1
7	1 0 1 0
8	1 0 1 1
9	1 1 0 0

Table 1.10.6 Excess-3 code

- In excess-3 code we get 9's complement of a number by just complementing each bit. Due to this excess-3 code is called self-complementing code or reflective code.

Example 1.10.20 Find the XS-3 code of 37.

GTU : Summer-16, Mark 1

Solution :

3	7	
0 0 1 1	0 1 1 1	BCD
0 1 1 0	1 0 1 0	BCD + 3 = XS-3 code

$$\therefore (37)_{10} = (0110 1010)_{XS-3}$$

Fig. 1.10.5

Example 1.10.21 Find the excess-3 code and its 9's complement for following decimal numbers. a) 592 b) 403

Solution :

a) By referring Table 1.10.6.

$$592_{10} = \begin{matrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ \hline 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 \end{matrix}$$

Complement of each other

9's complement of 592₁₀ =

b) By referring Table 1.10.6.

$$403_{10} = \begin{array}{|c|c|c|c|c|c|c|c|c|c|} \hline 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\ \hline \end{array} \leftarrow \text{Complement of each other}$$

$$9\text{'s complement of } 403_{10} = \begin{array}{|c|c|c|c|c|c|c|c|c|c|} \hline 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ \hline \end{array}$$

1.10.4.1 Excess-3 Addition

To perform excess-3 addition we have to

- Add two excess-3 numbers using binary addition.
- If carry = 1 → add 3 (0 0 1 1)₂ to the sum of two digits.
- If carry = 0 → subtract 3 (0 0 1 1)₂ from the sum.

Example 1.10.22 Perform the excess-3 addition of a) 8, 6 b) 1, 2.

Solution :

a) 8 + 6

1	1	1	1				
	1	0	1	1			
	1	0	0	1			
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	1
1							4

Carry
Excess-3 for 8
Excess-3 for 6
Carry = 1, hence
Add 3
Excess-3 for 14
Result in decimal

b) 1 + 2

1							
0	1	0	0				
0	1	0	1				
0	1	0	0	1			
0	0	1	1				
0	1	1	0				3

Carry
Excess-3 for 1
Excess-3 for 2
Carry = 0, hence
Sub 3
Excess-3 for 3
Result in decimal

1.10.4.2 Excess-3 Subtraction

- To perform excess-3 subtraction we have to
 - Complement the subtrahend.
 - Add complemented subtrahend to minuend.
 - If carry = 1 Result is positive. Add 3 (0 0 1 1)₂ and end-around carry.
 - If carry = 0 Result is negative. Subtract 3 (0 0 1 1)₂.

Example 1.10.23 Perform the excess-3 subtraction of a) 8 - 5, b) 5 - 8.

Solution : a) 8 - 5

1	1	1	1				
	1	0	1	1			
	0	1	1	1			
Carry	1	0	0	1	0		
	0	0	1	1			
	0	1	0	1			
							1
	0	1	1	0			

Excess-3 for 8
Complement of 5 in excess-3
Add 3
Add end-around carry
Excess-3 for 3

Note In excess-3, 9's complement and complement of any number is same. So this excess-3 subtraction method is also known as excess-3 subtraction using 9's complement.

b) 5 - 8

	1	0	0	0			
	0	1	0	0			
Carry	0	1	1	0	0		
	0	0	1	1			
	1	0	0	1			

Excess-3 for 5
Complement of 8 in excess-3
Subtract 3
Excess-3 for -3

Example 1.10.24 Perform each of the following operations in excess-3 code.

a) $\begin{array}{r} 16 \\ + 29 \\ \hline \end{array}$ b) $\begin{array}{r} 21 \\ - 12 \\ \hline \end{array}$

Solution :

a) 16 + 29

1							
	0	1	0	0			
	0	1	0	1			
Carry	0	1	0	0	1		
	0	1	0	0	1		
							1
	0	1	0	1	0		
	1	0	1	0			
	0	0	1	1			
	0	1	1	1			
							4

Carry
Excess-3 for 16
Excess-3 for 29
Propagate carry
Carry
Add 3 to correct 0 1 0 1
Subtract 3 to correct 1 0 1 0
Excess-3 for 45
Result

b) 21 - 12

1	1	1	1				
	0	1	0	1			
	1	0	1	1			
Carry	1	0	0	0	0		
	0	0	1	1			
	0	0	1	1			
							1
	0	0	1	1			
							9

Carry
Excess-3 for 21
Complement of 12 in excess-3
Add 3 and subtract 3
Add end-around carry
Excess-3 for 9

Examples for Practice

Example 1.10.25 : Represent decimal number 327 in Excess-3 code. [Ans. : 0110 0101 1010]

Example 1.10.26 : What is Excess-3 code of binary numbers : 0010 B, 0110 B and 0111 B ? [Ans. : 0101, 1001, 1010]

Example 1.10.27 : Represent the decimal number 6 in Excess-3 code. [Ans. : 1001]

1.10.5 Gray Code

- Gray code is a non-weighted code and is a special case of unit-distance code.
- In unit-distance code, bit patterns for two consecutive numbers differ in only one bit position. These codes are also called cyclic codes.
- The Table 1.10.7 shows the bit patterns assigned for gray code from decimal 0 to decimal 15.
- As shown in the Table 1.10.7 for gray code any two adjacent code groups differ only in one bit position.
- **Reflective Property :** The gray code is also called reflected code. Notice that the two least significant bits for 4_{10} through 7_{10} are the mirror images of those for 0_{10} through 3_{10} . Similarly, the three least significant bits for 8_{10} through 15_{10} are the mirror images of those for 0_{10} through 7_{10} .
- In general, the n least significant bits for 2^n through $2^{n+1} - 1$ are the mirror images of those for 0 through $2^n - 1$.

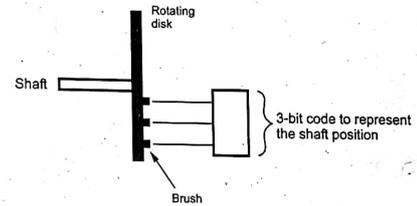
Decimal code	Gray code
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111
11	1110
12	1010
13	1011
14	1001
15	1000

Table 1.10.7 Gray code

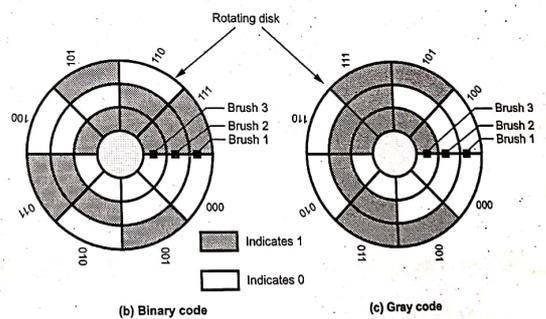
1.10.5.1 Application of Gray Code

- Let us consider an application where 3-bit binary code is provided to indicate position of the rotating disk with the help of brushes.
- When brushes are on the black portion, they output a 1. When on the white portion, they output a 0.
- Now consider what happens when the brushes are on the 111 sector and almost ready to enter the 000 sector.

- If one brush is slightly ahead of the other, say the 3rd brush, then the position is indicated by a 011 instead of a 111 or 000. This results, a 180° error in the disk position.
- Since it is physically impossible to have all the brushes precisely aligned, some error will always be present at the edges of the sectors.
- If we use gray code to represent disk position then error due to improper brush alignment can be reduced. This is because the gray code assures that only one bit will change each time the decimal number is incremented.



(a) Shaft position encoder



(b) Binary code

(c) Gray code

Fig. 1.10.6 Position indication using binary and gray codes

- So in 3-bit code, error may occur due to one bit position. Other two bits positions of two adjacent sectors are always same and hence there is no possibility of error.
- Therefore in 3-bit code probability of error is reduced up to 66%. In case of 4-bit code it is reduced up to 75%. This is an important advantage of gray code.

1.10.5.2 Gray to Binary Conversion

Steps for gray to binary code conversion

1. The Most Significant Bit (MSB) of the binary number is the same as the Most Significant Bit (MSB) of the gray code number. So write down MSB as it is.
2. To obtain the next binary digit, perform an exclusive-OR-operation between the bit just written down and the next gray code bit. Write down the result.
3. Repeat step 2 until all gray code bits have been exclusive-ORed with binary digits.

A	B	$A \oplus B$ Exclusive OR operation
0	0	0
0	1	1
1	0	1
1	1	0

Table 1.10.8 Exclusive OR operation

Example 1.10.28 Convert gray code 101011 into its binary equivalent.

Solution :

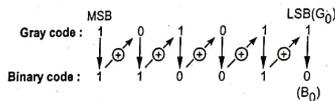


Fig. 1.10.7

$(101011)_{\text{gray}} = (110010)_2$

In general we can perform gray code to binary code conversion as shown below :

$$\begin{aligned}
 B_n \text{ (MSB)} &= G_n \text{ (MSB)} & B_2 &= B_3 \oplus G_2 \\
 B_{n-1} &= B_n \oplus G_{n-1} & \dots & & B_1 &= B_2 \oplus G_1 \\
 B_{n-2} &= B_{n-1} \oplus G_{n-2} & & & B_0 &= B_1 \oplus G_0
 \end{aligned}$$

Example 1.10.29 Convert the gray code 1101 to binary

GTU : Summer-16, Mark 1

Solution :

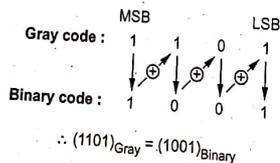


Fig. 1.10.8

1.10.5.3 Binary to Gray Code Conversion

Steps for binary to gray code conversion

1. The MSB of the gray code is the same as the MSB of the binary number. So write down MSB as it is.
2. To obtain the next gray digit, perform an exclusive-OR-operation between previous and current binary bit. Write down the result.
3. Repeat step 2 until all binary bits have been exclusive-ORed with their previous ones.

Example 1.10.30 Convert 10111011 in binary into its equivalent gray code.

Solution :

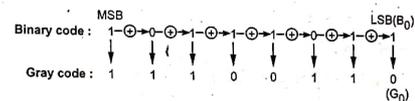


Fig. 1.10.9

$(10111011)_2 = (11100110)_{\text{gray}}$

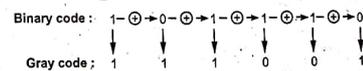
In general we can perform binary code to gray code conversion as shown below :

$$\begin{aligned}
 G_n \text{ (MSB)} &= B_n \text{ (MSB)} & G_2 &= B_3 \oplus B_2 \\
 G_{n-1} &= B_n \oplus B_{n-1} & \dots & & G_1 &= B_2 \oplus B_1 \\
 G_{n-2} &= B_{n-1} \oplus B_{n-2} & & & G_0 &= B_1 \oplus B_0
 \end{aligned}$$

Example 1.10.31 Encode the decimal number 46 to Gray code.

Solution :

$(46)_{10} = (101110)_2$

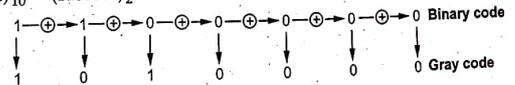


$(46)_{10} = (111001)_{\text{Gray}}$

Example 1.10.32 Convert $(96)_{10}$ to its equivalent gray code and EX-3 code.

GTU : Summer-15, Marks 4

Solution : $(96)_{10} = (1100000)_2$



$(96)_{10} = (1010000)_{\text{Gray}} = (11001001)_{\text{EX-3}}$

Example for Practice

[Ans. : 0101]

Example 1.10.33 : Represent the decimal number 6 in Gray code.

1.10.6 Alphanumeric Codes

- The codes which consists of both numbers and alphabetic characters are called alphanumeric codes.
- The most commonly used alphanumeric codes are : ASCII (American Standard Code for Information Interchange) and EBCDIC (Extended Binary Coded Decimal Interchange Code).
- These codes consists of symbols to represent -
 - 26 alphabets with capital and small letters.
 - Numbers from 0 to 9.
 - Punctuation marks and other symbols.

1.10.6.1 ASCII

- ASCII code is a seven-bit code in which the decimal digits are represented by the BCD code preceded by 011.
- Since it is a 7-bit code, it represent $2^7 = 128$ symbols.
- The letter of the alphabet and other symbols and instructions are represented by other code combination as shown in Table 1.10.9. For example, ASCII code for N = $(4E)_H = (10011110)_2$.

LSBs	MSBs							
	000 (0)	001 (1)	010 (2)	011 (3)	100 (4)	101 (5)	110 (6)	111 (7)
0000 (0)	NUL	DLE	SP	0	@	P	.	p
0001 (1)	SOH	DC ₁	!	1	A	Q	a	q
0010 (2)	STX	DC ₂	"	2	B	R	b	r
0011 (3)	ETX	DC ₃	#	3	C	S	c	s
0100 (4)	EOT	DC ₄	\$	4	D	T	d	t
0101 (5)	ENQ	NAK	%	5	E	U	e	u
0110 (6)	ACK	SYN	&	6	F	V	f	v
0111 (7)	BEL	ETB	'	7	G	W	g	w
1000 (8)	BS	CAN	(8	H	X	h	x

1001 (9)	HT	EM)	9	I	Y	i	y
1010 (A)	LF	SUB	*	:	J	Z	j	z
1011 (B)	VI	ESC	+	;	K	[k	{
1100 (C)	FF	FS	,	<	L	\	l	
1101 (D)	CR	GS	-	=	M]	m	}
1110 (E)	SO	RS	.	>	N	↑	n	~
1111 (F)	SI	US	/	?	O	←	o	DEL

Table 1.10.9 American standard code for information interchange

Definition of control abbreviations :

ACK	Acknowledge	FS	Form separator
BEL	Bell	GS	Group separator
BS	Backspace	HT	Horizontal tab
CAN	Cancel	LF	Line feed
CR	Carriage return	NAK	Negative acknowledge
DC ₁ -DC ₄	Direct control	NUL	Null
DEL	Delete idle	RS	Record separator
DLE	Data link escape	SI	Shift in
EM	End of medium	SO	Shift out
ENQ	Enquiry	SOH	Start of heading
EOT	End of transmission	STX	Start text
ESC	Escape	SUB	Substitute
ETB	End of transmission block	SYN	Synchronous idle
ETX	End text	US	Unit separator
FF	Form feed	VT	Vertical tab

Note The hexadecimal digit representing each bit pattern is shown in parentheses.

Example 1.10.34 Write the ASCII code for 'ELECTRONICS'.

Solution :

45, 4C, 45, 43, 54, 52, 4F, 4E, 49, 43, 53 i.e.,
 1000101 1001100 1000101 1000011 1010100 1010010
 1001111 1001110 1001001 1000011 1010011

Example 1.10.35 Encode the word 'BINARY' in ASCII form.

Solution : 42, 49, 4E, 41, 52, 59 i.e.,

1000010 1001001 1001110 1000001 1010010 1011001

Example 1.10.36 A line printer is capable of printing 132 characters in a single-line and each character is represented by ASCII code. How many bits are required to print each line ?

Solution : ASCII code is a 7-bit code. Therefore, to print one line we require $132 \times 7 = 924$ bits.

Example 1.10.37 How many bits of memory are required for storing 100 names of a group of people assuming that no name occupies more than 20 characters (including space) ? Assume 7-bit ASCII code with parity bit.

Solution : Space reserved for one name = $20 \times (7 + 1) = 160$ bits. Bits required for storing 100 names = $160 \times 100 = 16000$ bits.

Examples for Practice

Example 1.10.38 : Find gray codes for the following binary numbers :
 i) 11001100 ii) 01011110 [Ans. : i) 10101010 ii) 01110001]

Example 1.10.39 : What will be the gray code of binary number 1100 B, 0111 B and 1101 B ?
 [Ans. : 1010, 0100, 1011]

Review Questions

1. Give classification of codes.
2. Define code. List various codes.
3. What is meant by weighted and non-weighted coding ?
4. Define reflective and sequential codes ?
5. Write a note on BCD code.
6. What are the rules for BCD addition ? Illustrate with the help of example.
7. Explain the steps for BCD subtraction using 9's complement method.
8. Explain the steps for BCD subtraction using 10's complement method.
9. What is gray code ? What is the advantage of gray codes over the binary number sequence ?
10. Show that the excess-3 code is self-complementing.
11. Write a note on excess-3 code.
12. Write a brief note on gray codes. Also discuss methods for conversion from gray to binary code and vice versa. **GTU : May-14, Marks 7**
13. State the application of gray code.
14. Explain ASCII code with the help of example.
15. What is self complementing code? Represent $(472)_{10}$ in 2421 self complementing code. **GTU : Summer-15, Marks 2**

1.11 Error Detecting and Correcting Codes

- When the digital information in the binary form is transmitted from one circuit or system to another circuit or system an error may occur. This means a signal corresponding to 0 may change to 1 or vice-versa due to presence of noise. To maintain the data integrity between transmitter and receiver, extra bit or more than one bit are added in the data. These extra bits allow the detection and some times correction of error in the data. The data along with the extra bit/bits forms the code. Codes which allow only error detection are called **error detecting codes** and codes which allow error detection and correction are called **error detecting and correcting codes**.

1.11.1 Parity Bit

- A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1s either odd or even. The message, including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a **parity generator** and the circuit that checks the parity in the receiver is called a **parity checker**.
- In even parity the added parity bit will make the total number of 1s an even amount. In odd parity the added parity bit will make the total number of 1s an odd amount.
- Table 1.11.1 shows the 3-bit message with even parity and odd parity.

3-bit Message			Message with Odd Parity		Message with Even Parity	
A	B	C	Message	Parity	Message	Parity
0	0	0	000	1	000	0
0	0	1	001	0	001	1
0	1	0	010	0	010	1
0	1	1	011	1	011	0
1	0	0	100	0	100	1
1	0	1	101	1	101	0
1	1	0	110	1	110	0
1	1	1	111	0	111	1

Table 1.11.1 Message with even and odd parity

Example 1.11.1 Write a ASCII code for the decimal digit 9 with an even parity. Place parity bit in the most significant position.

Solution : The 7-bit ASCII code for the decimal digit 9 is 0111001. This requires the addition of a 0 in the most significant place to give even parity as shown.

Added parity bit → 00111001

Example 1.11.2 Write a ASCII code for the alphabet 'A' with an odd parity. Place parity bit in the most significant position.

Solution : The 7-bit ASCII code for the alphabet 'A' is 1000001. This requires the addition of a 1 in the most significant place to give odd parity, as shown.

Added parity bit → 11000001

At the receiving end, message with parity bit is received. Every time it is checked for parity. When parity error is detected, receiver requests for transmitter to re-transmit the message.

Example 1.11.3 The received code is 1000 0001. Check whether code is correctly received or not if odd parity is used.

Solution : The received code has even parity hence the code is not received correctly.

More about parity error detection

As a general rule in a digital system where the transmission system is relatively short, it may be assumed that the probability of a single-bit error is small and that of a double-bit error and higher order errors is extremely small. The parity error detection system just described detects any odd number of errors. However, it cannot detect an even number of error because such errors will not destroy the parity of the transmitted group of bits.

1.11.2 Hamming Code

- Hamming code not only provides the detection of a bit error, but also identifies which bit is in error so that it can be corrected. Thus Hamming code is called error detecting and correcting code. The code uses a number of parity bits (dependent on the number of information bits) located at certain positions in the code group. Follows sections describe how Hamming code can be constructed for single error correction.

Number of Parity Bits

- As mentioned earlier, number of parity bits depend on the number of information bits. If the number of information bits is designed x, then the number of parity bits, P is determined by the following relationship :

$$2^P \geq x + P + 1 \quad \dots (1.11.1)$$

For example, if we have four information bit, i.e. x = 4, then P is found by trial and error using equation 1. Let P = 2. Then

$$2^P = 2^2 = 4$$

and $x + P + 1 = 4 + 2 + 1 = 7$

- Since 2^P must be equal to or greater than $x + P + 1$, the relationship in equation (1.9.1) is not satisfied. Hence we have to try with next value of P. Let P = 3.

Then $2^P = 2^3 = 8$

and $x + P + 1 = 4 + 3 + 1 = 8$

- This value of P satisfies the relationship given is equation (1.9.1), and therefore we can say that three parity bits are required to provide single error correction for four information bits.

Locations of the Parity Bits in the Code

- Now we know that how to calculate the number of parity bits required to provide single error correction for given number of information bits. In our example we have four information bits and three parity bits. Therefore, the code is of seven bits. The right-most bit is designated bit 1, the next bit is bit 2, and so on, as shown below :

Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1

- The parity bits are located in the positions that are numbered corresponding to ascending powers of two (1, 2, 4, 8 ...). Therefore, for 7 - bit code, locations for parity bits and information bit are as shown below :

$D_7, D_6, D_5, P_4, D_3, P_2, P_1$

where symbol P_n designates a particular parity bit, D_n designates a particular information bit, and n is the location number.

Assigning Values to Parity Bits

- Now we know the format of the code. Let us see how to determine 1 or 0 value to each parity bit. In Hamming code, each parity bit provides a check on certain other bits in the total code, therefore, we must know the value of these others in order to assign the parity bit value. To do this, we must write the binary number for each decimal location number as shown in the third row of Table 1.9.2.

Bit designation	D_7	D_6	D_5	P_4	D_3	P_2	P_1
Bit location	7	6	5	4	3	2	1
Binary location number	111	110	101	100	011	010	001

Information bits (D_n)						
Parity bits (P_n)						

Table 1.11.2 Bit position table for a seven bit error correcting code

Assignment of P_1 :

- Looking at the Table 1.11.2 we can see that the binary location number of parity bit P_1 has a 1 for its right-most digit. This parity bit checks all bit locations, including itself, that have 1s in the same location in the binary location numbers. Therefore, parity bit P_1 checks bit locations 1, 3, 5 and 7, and assigns P_1 such that bit locations 1, 3, 5, and 7 will have even parity.

Assignment of P_2 :

- Looking at the Table 1.11.2 we can see that the binary location number of parity bit P_2 has a 1 for its middle bit. This parity bit checks all bit locations, including itself, that have 1s in the middle bit. Therefore, parity bit P_2 checks bit locations 2, 3, 6 and 7 and assigns P_2 according to even or odd parity.

Assignment of P_4 :

- Looking at the Table 1.11.2 we can see that the binary location number of parity bit P_4 has a 1 for its left-most digit. This parity bit checks all bit locations, including itself, that have 1s in the left-most bit. Therefore, parity bit P_4 checks bit locations 4, 5, 6 and 7 and assigns P_4 according to even and odd parity.

Example 1.11.4 Encode the binary word 1011 into seven bit even parity Hamming code.

Solution :

Step 1 : Find the number of parity bits required. Let $P = 3$, then

$$2^P = 2^3 = 8$$

$$x + P + 1 = 4 + 3 + 1 = 8$$

Three parity bits are sufficient.

$$\therefore \text{Total code bits} = 4 + 3 = 7$$

Step 2 : Construct a bit location table

Bit designation	D_7	D_6	D_5	P_4	D_3	P_2	P_1
Bit location	7	6	5	4	3	2	1
Binary location number	111	110	101	100	011	010	001

Information bits	1	0	1	1		
Parity bits			0		0	1

Step 3 : Determine the parity bits

For P_1 : Bit locations 3, 5 and 7 have three 1s and therefore to have an even parity P_1 must be 1.

For P_2 : Bit locations 3, 6 and 7 have two 1s and therefore to have an even parity P_2 must be 0.

For P_4 : Bit locations 5, 6 and 7 two 1s and therefore to have an even parity P_4 must be 0.

Step 4 : Enter the parity bits into the table to form a seven bit Hamming code=1010101.

Example 1.11.5 Determine the single error-correcting code for the information code 1 0 1 1 1 for odd parity.

Solution :

Step 1 : Find the number of parity bits required. Let $P = 3$.

$$\text{Then } 2^P = 2^3 = 8$$

$$\therefore x + P + 1 = 5 + 3 + 1 = 9$$

This will not work. Try $P = 4$. Then

$$2^P = 2^4 = 16$$

$$x + P + 1 = 5 + 4 + 1 = 10$$

Equation (1.9.1) is satisfied and hence four bits are sufficient.

$$\therefore \text{Total code bit} = 5 + 4 = 9$$

Step 2 : Construct a bit location table

Bit designation	D_9	P_8	D_7	D_6	D_5	P_4	D_3	P_2	P_1
Bit location	9	8	7	6	5	4	3	2	1
Binary location number	1001	1000	0111	0110	0101	0100	0011	0010	0001
Information bits	1		0	1	1		1		
Parity bits		0				1		1	0

Step 3 : Determine the Parity Bits

For P_1 : Bit locations 3, 5, 7 and 9 have three 1s and therefore to have odd parity P_1 must be 0.

For P_2 : Bit locations 3, 6, 7 have two 1s and therefore to have an odd parity P_2 must be 1.

For P_4 : Bit locations 5, 6 and 7 have two 1s and therefore to have an odd parity P_4 must be 1.

For P_8 : Bit P_8 checks bit locations 8 and 9 and must be 0 to have an odd parity.

Step 4 : Enter the parity bits into the table to form a nine bit Hamming code = 100111110.

1.11.3 Detecting and Correcting an Error

In the last section we have seen how to construct Hamming code for given number of information bits. Now we will see how to use it to locate and correct an error. To do this, each parity bit, along with its corresponding group of bits must be checked for proper parity. The correct result of individual parity check is marked by 0 whereas wrong result is marked by 1. After all parity checks, binary word is formed taking resulting bit for P_1 as LSB. This word gives bit location where error has occurred. If word has all bits 0 then there is no error in the Hamming code.

Example 1.11.6 Assume that the even parity Hamming code in example (0 1 1 0 0 1 1) is transmitted and that 0 1 0 0 0 1 1 is received. The receiver does not know what was transmitted. Determine bit location where error has occurred using received code.

Solution :

Step 1 : Construct the bit location table.

Bit designation	D_7	D_6	D_5	P_4	D_3	P_2	P_1
Bit location	7	6	5	4	3	2	1
Binary location number	111	110	101	100	011	010	001
Received code	0	1	0	0	0	1	1

Step 2 : Check for parity bits

For P_1 : P_1 checks locations 1, 3, 5, and 7.

There is one 1 in the group.

∴ Parity checks for even parity is wrong → 1 (LSB)

For P_2 : P_2 checks locations 2, 3, 6 and 7.

There are two 1s in the group

∴ Parity check for even parity is correct → 0

For P_4 : P_4 checks locations 4, 5, 6 and 7.

There are one 1 in the group

∴ Parity check for even parity is wrong → 1

The resultant word is 1 0 1. This says that the bit in the number 5 location is in error. It is 0 and should be a 1. Therefore, the correct code is 0 1 1 0 0 1 1, which agrees with the transmitted code.

Example 1.11.7 The Hamming code 1 0 1 1 0 1 1 0 1 is received. Correct it if any errors. There are four parity bits and odd parity is used.

Solution :

Step 1 : Construct a bit location table

Bit designation	D_9	P_8	D_7	D_6	D_5	P_4	D_3	P_2	P_1
Bit location	9	8	7	6	5	4	3	2	1
Binary location number	1001	1000	0111	0110	0101	0100	0011	0010	0001
Received code	1	0	1	1	0	1	1	0	1

Step 2 : Check for parity bits

For P_1 : P_1 checks locations 1, 3, 5, 7 and 9.

There are four 1s in the group

∴ Parity check for odd parity is wrong → 1 (LSB)

For P_2 : P_2 checks locations 2, 3, 6 and 7.

There are three 1s in the group

∴ Parity check for odd parity is correct → 0

For P_4 : P_4 checks locations 4, 5, 6 and 7.

There are three 1s in the group

∴ Parity check for odd parity is correct → 0

For P_8 : P_8 checks locations 8 and 9.

There is one 1 in the group

∴ Parity check for odd parity is correct → 0

The resultant word is 0001. This says that the bit in the number 1 location is in error. It is 1 and should be 0. Therefore, the correct code is 101101100.

1.11.4 Single Error Correction Plus Double Error Detection

A hamming code as explained above provides for the detection and correction of only a single error. With a slight modification, it is possible to construct hamming code for single-error correction and double-error detection. A one more parity bit is added in the hamming code to ensure hamming code (including all parity bits) contains an even number of 1's. The added parity bit is not used in determining the values of the other parity bits. The resulting hamming code enables single error correction and double error detection.

When overall parity bit is correct, there is no single error during the transmission of the code. If overall parity bit is incorrect, then there is single error and the bit position of the error can be indicated by binary number formed after checking the parity bits. Hence, single error correction can be achieved. If overall parity bit is correct and binary number formed after checking the parity bits is other than 0-0-0, there are two errors. In this case, double error detection is achieved. However, no correction is possible.

Examples for Practice

Example 1.11.8 : Construct hamming codes for the decimal numbers 1, 4, 8.

[Ans. : Considering odd parity 1 : 0001100, 4 : 0100001, 8 : 1000000]

Example 1.11.9 : Generate the even parity Hamming codes for following binary data.

a) 1101 b) 1001 [Ans. : a) 1100110 b) 1001100]

Example 1.11.10 : A seven bit Hamming code is received as 1111101. What is the correct code ?

[Ans. : 1111111]

Example 1.11.11 : Generate Hamming code for the following binary data. i) 1101 ii) 1001

[Ans. : i) 1100110 ii) 1001100]

Example 1.11.12 : Determine whether single error has occurred and if so correct the error using Hamming code for 1100010.

[Ans. : Corrected code = 1100110]

Review Questions

1. What is parity bit ? Explain its use.
2. Explain the 7 bit hamming code.
3. Explain the procedure of generating hamming code from the information.
4. Explain how Hamming code is useful for correcting and detecting the errors using an example.

5. Explain error detection and correction.

6. What is hamming code ? How is the hamming code word tested and corrected ?

Oral Questions and Answers

Q.1 Which system is used in digital computers because all electrical and electronic circuits can be made to respond to the states concept ?

Ans. : Binary number.

Q.2 Which numbers are used to represent decimal numbers in computer ?

Ans. : BCD numbers.

Q.3 Which number system uses binary numbers in most compressed form ?

Ans. : Hexadecimal numbers.

Q.4 In which numeral every position has a value 2 times the value of the position to its right ?

Ans. : Binary.

Q.5 Which number system has a base of 16 ?

Ans. : Hexadecimal number system.

Q.6 What is meant by weighted and non-weighted coding ?

Ans. : **Weighted codes :** In weighted codes, each digit position of the number represents a specific weight. For example, in decimal code, if number is 567 then weight of 5 is 100, weight of 6 is 10 and weight of 7 is 1. In weighted binary codes each digit has a weight 8, 4, 2 or 1.

The codes 8421, 2421 and 5211 are all weighted codes. (Refer Tables 1.10.1, 1.10.3 and 1.10.5)

Non-weighted codes : Non-weighted codes are not assigned with any weight to each digit position, i.e., each digit position within the number is not assigned fixed value. Excess-3 and gray codes are the non-weighted codes.

Q.7 In which type of codes the positional weights are not assigned ?

Ans. : Non-weighted code.

2

Logic Gates and Boolean Algebra

Contents

2.1	Logic Gates	Dec.-12, 13, May-13, 14,
2.2	Boolean Algebra	Summer-15, 16, 17, 18,
		Winter-14, 16, 18, Marks 8

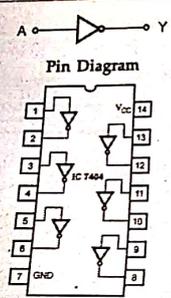
Oral Questions and Answers

2.1 Logic Gates

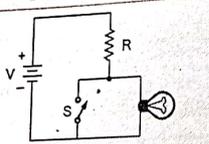
- The three primitive logic functions are represented by distinctive logic symbols known as basic gates : AND gate, OR gate and NOT gate.
- From these primitive logic functions we have derived logic functions and hence derived logic gates. There are NAND gate, NOR gate, EX-OR gate and EX-NOR gate.

NOT gate (Inverter) : The output is a complement of input.

Logic Diagram (Symbol)



Switch Equivalent



Input	Output
Switch open (Low)	Lamp ON (High)
Switch close (High)	Lamp OFF (Low)

Application : Used to complement (invert) digital signal.

Truth Table

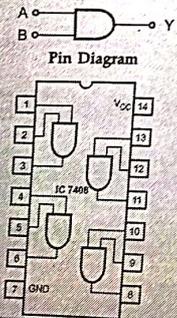
Input	Output
A	Y
0	1
1	0

Boolean Expression

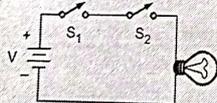
$$Y = \bar{A}$$

AND gate : The output is high only when all inputs are high.

Logic Diagram (Symbol)



Switch Equivalent



Input		Output
S ₁	S ₂	
Open (Low)	Open (Low)	Lamp OFF (Low)
Open (Low)	Close (High)	Lamp OFF (Low)
Close (High)	Open (Low)	Lamp OFF (Low)
Close (High)	Close (High)	Lamp ON (High)

Application : Used to implement logical AND operation.

Truth Table

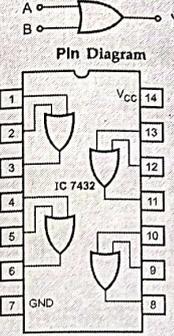
Input	Output	
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Boolean Expression

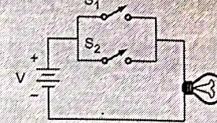
$$Y = A \cdot B$$

OR gate : The output is high when any of the inputs is high.

Logic Diagram (Symbol)



Switch Equivalent



Input		Output
S ₁	S ₂	
Open (Low)	Open (Low)	Lamp OFF (Low)
Open (Low)	Close (High)	Lamp ON (High)
Close (High)	Open (Low)	Lamp ON (High)
Close (High)	Close (High)	Lamp ON (High)

Application : Used to implement logical OR operation.

Truth Table

Input	Output	
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Boolean Expression

$$Y = A + B$$

Buffer : The output is same as input.

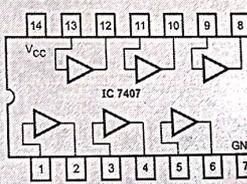
Symbol



Boolean Expression

$$Y = A$$

Pin Diagram



Application : It is used to increase output driving capacity.

Truth Table

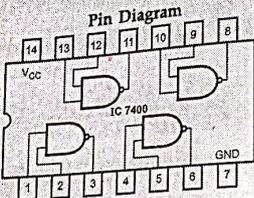
Input	Output
A	Y
0	0
1	1

NAND gate : The output is high only when one of the inputs is low.

Symbol



Boolean Expression
 $Y = A \cdot B$



Truth Table

Input	Output	
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

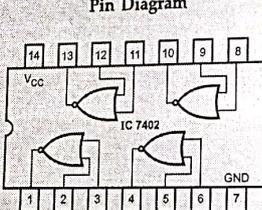
Application : It can be used to implement any digital circuit.

NOR Gate : The output is high when all the inputs are low.

Symbol



Boolean Expression
 $Y = A + B$



Truth Table

Input	Output	
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

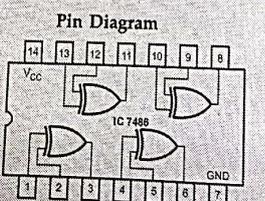
Application : It can be used to implement any digital circuit.

Exclusive OR (EX-OR) gate : The output is high only when odd number of inputs are high.

Symbol



Boolean Expression
 $Y = A \oplus B$



Truth Table

Input	Output	
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

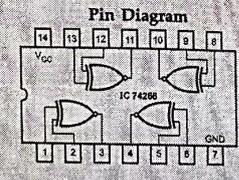
Application : It is used to implement magnitude comparator, gray code converter, adder/subtractor circuits, parity generator, modulo-2 adder, etc.

Exclusive NOR (EX-NOR) gate : The output is high only when even number of ones at the input or all inputs are high.

Symbol



Boolean Expression
 $Y = A \oplus B$



Truth Table

Input	Output	
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Applications : It is used to implement even parity generator, comparator, even parity checker, etc.

Note EX-OR and EX-NOR gates are also known as mutually exclusive gates.

Wave-forms / Timing diagrams of all the gates

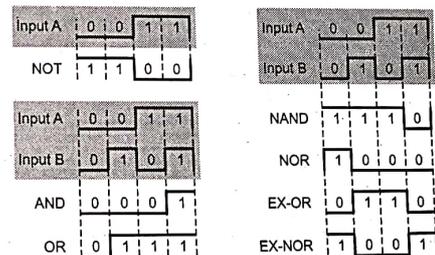


Fig. 2.1.1

Note : EX-OR and EX-NOR gates are also known as mutually exclusive gates.

2.1.1 Positive and Negative Logic

- The binary logic used in the digital systems assumes only two values, either HIGH or LOW. The HIGH and LOW voltage levels are used to denote these two values.

- The two levels or states, of a signal variable, can be considered to represent the two numerals, viz. 1 and 0 of the binary number system or the two logic states, viz. TRUE and FALSE in logic operations.
- Two voltage levels used to represent two logic states are also called **logic levels**.
- In binary logic, two voltage levels represent the two binary digits, 1 and 0.
- If the higher of the two voltages represents a 1 and the lower voltage represents a 0, the system is called a **positive logic system**.
- If the lower voltage represents a 1 and the higher voltage represents a 0, we have a **negative logic system**.
- As an example, assume that we have positive 5 V and 0 V as logic-level voltages.
- Then positive and negative logic can be defined as :
Positive Logic : HIGH = 1 (i.e. +5 V)
 LOW = 0 (i.e. 0 V)
Negative Logic : HIGH = 0 (i.e. +5 V)
 LOW = 1 (i.e. 0 V)

- Both positive and negative logic are used in digital systems, but positive logic is the more common.
- In practice, the voltages at different nodes in the digital circuit may differ slightly due to internal resistances, parasitic effects and loading effects. Therefore, to define a logic level, a range of voltage is assigned instead of a particular voltage level. This is illustrated in Fig. 2.1.2.

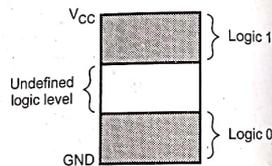


Fig. 2.1.2 Voltage range for positive logic system

Review Question

1. Draw the logic symbol, expression and truth table for following logic gates :
 1. AND 2. OR 3. NOT 4. NAND 5. NOR 6. EX-OR 7. EX-NOR

2.2 Boolean Algebra

GTU : Dec.-12, 13, May-13, 14, Summer-15, 16, 17, 18, Winter-14, 16, 18

- Boolean algebra is a mathematical system that defines a series of logical operations (AND, OR, NOT) performed on sets of variables (a, b, c, ...). When stated in this form, the expression is called a **Boolean equation** or **switching equation**.

2.2.1 Boolean Algebra Terminology

Variable : The symbol which represent an arbitrary elements of an Boolean algebra is known as **variable**. Any single variable or a function of several variables can have either a 1 or 0 value. For example, in expression $Y = A + BC$, variables A, B and C can have either a 1 or 0 value, and function Y also can have either a 1 or 0 value; however its value depends on the value of Boolean expression.

Constant : In expression $Y = A + 1$, the first term A is a variable and have value either a 1 or 0. The second term has a fixed value 1. So 1 is a constant here. The constant term may be 0 or 1.

Complement : A complement of a variable is represented by a "bar" over the letter. For example, the complement of a variable A will be denoted by \bar{A} . So if $A = 1, \bar{A} = 0$ and if $A = 0, \bar{A} = 1$. Sometimes a prime symbol (') is used to denote the complement. For example, the complement of A can be written as A' .

Literal : Each occurrence of a variable in Boolean function either in a complemented or an uncomplemented form is called a **literal**.

Boolean function : Boolean expressions are constructed by connecting the Boolean constants and variables with the Boolean operations. These Boolean expressions are also known as **Boolean formulae**.

- We use Boolean expressions to describe **Boolean functions**.
- For example, if the Boolean expression $(A + \bar{B}) C$ is used to describe the function f, then Boolean function is written as
 $f(A, B, C) = (A + \bar{B}) C$ or $f = (A + \bar{B}) C$

2.2.2 Axiomatic Definitions of Boolean Algebra

- The postulates of a mathematical system form the basic assumption from which it is possible to deduce the theorems, laws and properties of the system. Boolean algebra is formulated by a defined set of elements, together with two binary operators, + and \cdot , provided that the given postulates are satisfied.

Closure Property

- **Closure (a) :** Closure with respect to the operator + : When two binary elements are operated by operator + the result is a unique binary element.
- **Closure (b) :** Closure with respect to the operator \cdot (dot) : When two binary elements are operated by operator \cdot (dot), the result is a unique binary element.

Identity Property

- An identity element with respect to \cdot , designated by 1 : $A \cdot 1 = 1 \cdot A = A$

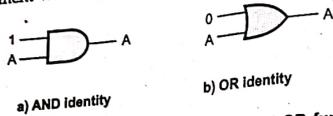


Fig. 2.2.1 Identity elements for the AND and OR functions

Commutative Property

- Commutative with respect to $+$: $A + B = B + A$
- Commutative with respect to \cdot : $A \cdot B = B \cdot A$

Distributive Property

- Distributive property of \cdot over $+$: $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$
- Distributive property of $+$ over \cdot : $A + (B \cdot C) = (A + B) \cdot (A + C)$

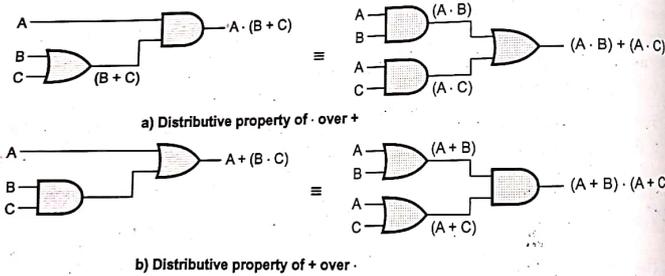


Fig. 2.2.2 Distributive property

Associative Property

- Associative property of $+$: $A + (B + C) = (A + B) + C$
- Associative property of \cdot : $(A \cdot B) \cdot C = A \cdot (B \cdot C)$

Complement Property

- For every binary element $A = 1, \bar{A} = 0$
- Complementary property of \cdot : $A \cdot \bar{A} = 0$
- Complementary property of $+$: $A + \bar{A} = 1$

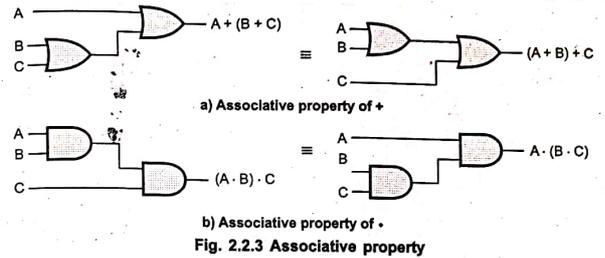


Fig. 2.2.3 Associative property

Idempotency Property

- Idempotency refers to the property of sameness : $A + A = A$ or $A \cdot A = A$
- Any variable ANDed or ORed with itself results in the original variable.

Absorption Property

- We know that, in OR function if any one input is logic 1, output is logic 1. Therefore, we have an important relationship : $A + 1 = 1$

- Using this relationships we can derive two absorption properties as follows :

- $A + AB = A(1 + B)$... Distributive property
 $= A$ $\because 1 + B = 1$
- $A(A + B) = AA + AB$... Distributive property
 $= A + AB$... Idempotency property
 $\therefore A(A + B) = A$... Absorption property

Involution Property

- Double inversion of any variable results in the original variable
 $\overline{\overline{A}} = A$

2.2.3 Basic Theorems and Properties of Boolean Algebra

- From the above discussion we can summarize the postulates and theorems of Boolean algebra as shown in Table 2.2.1.

Postulates	(a)	(b)
Postulate 1	Result of each operation is either 0 or 1 $\in B$	
Postulate 2 (Identity)	$A + 0 = A$	$A \cdot 1 = A$
Postulate 3 (Commutative)	$A + B = B + A$	$AB = BA$

Postulate 4 (Distributive)	$A(B+C) = AB+AC$	$A+BC = (A+B)(A+C)$
Postulate 5 (Complement)	$A+\bar{A} = 1$	$A \cdot \bar{A} = 0$
Theorems	(a)	(b)
Theorem 1 (Idempotency)	$A+A = A$	$A \cdot A = A$
Theorem 2	$A+1 = 1$	$A \cdot 0 = 0$
Theorem 3 (Involution)		$\bar{\bar{A}} = A$
Theorem 4 (Absorption)	$A+AB = A$	$A(A+B) = A$
Theorem 5	$A+\bar{A}B = A+B$	$A \cdot (\bar{A}+B) = AB$
Theorem 6 (Associative)	$A+(B+C) = (A+B)+C$	$A(BC) = (AB)C$

Table 2.2.1 Postulates and basic theorems of Boolean algebra

Example 2.2.1 Prove that $A + \bar{A}B = A + B$

GTU : Winter-18, Marks 2

Solution : $A + \bar{A}B = A + AB + \bar{A}B$ by Theorem : 4(a)
 $= A + B \cdot (A + \bar{A})$ by Postulate : 4(a)
 $= A + B \cdot 1$: 5(a)
 $= A + B$: 2(b)

Example 2.2.2 Prove that $A \cdot (\bar{A} + B) = AB$

GTU : Winter-18, Marks 2

Solution : $A \cdot (\bar{A} + B) = (A + AB) \cdot (\bar{A} + B)$ by Theorem : 4(a)
 $= A\bar{A} + AB + ABB$ by Postulate : 4(a)
 $= AB + ABB$: 5(b)
 $= AB + AB$: 2(b)
 $= AB$ by Theorem : 1(a)

2.2.4 DeMorgan's Theorems

DeMorgan suggested two theorems that form an important part of Boolean algebra. In the equation form, they are : 1. $\overline{AB} = \bar{A} + \bar{B}$
 2. $\overline{A+B} = \bar{A} \cdot \bar{B}$
 1. $\overline{AB} = \bar{A} + \bar{B}$: The complement of a product is equal to the sum of the complements. This is illustrated by truth Table 2.2.2.

A	B	AB	\overline{AB}
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Table 2.2.2 Truth table

2. $\overline{A+B} = \bar{A} \cdot \bar{B}$: The complement of a sum is equal to the product of the complements. The truth Table 2.1.3 illustrates this law.

A	B	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Table 2.2.3 Truth table

2.2.5 Principle of Duality

The principle of duality theorem says that, starting with a Boolean relation, you can derive another Boolean relation by

1. Changing each OR sign to an AND sign
2. Changing each AND sign to an OR sign and
3. Complementing any 0 or 1 appearing in the expression.

For example : Dual of relation $A + \bar{A} = 1$ is $A \cdot \bar{A} = 0$

Illustrative Examples

Example 2.2.3 Apply DeMorgans theorem to simplify $A + \bar{B}\bar{C}$

Solution : $A + \bar{B}\bar{C} = \bar{A} \cdot \overline{\bar{B}\bar{C}}$
 $= \bar{A} \cdot (\bar{B} + C) = \bar{A}\bar{B} + \bar{A}C$

Example 2.2.4 Simplify $\overline{ABCD} + \overline{BCD} + \overline{BC}D + B\bar{C}D$

Solution : $= \overline{BCD}(\bar{A} + 1) + \overline{BC}D + B\bar{C}D$ Distributive
 $= \overline{BCD} + \overline{BC}D + B\bar{C}D$ Theorem 2(a) : $[A + 1 = 1]$
 $= \overline{BD}(C + \bar{C}) + B\bar{C}D$ Distributive
 $= \overline{BD} + B\bar{C}D$ Postulate 5(a) : $[A + \bar{A} = 1]$
 $= B(\bar{D} + \bar{C}D)$ Distributive
 $= B(\bar{D} + \bar{C})$ Theorem 5(a) : $[A + \bar{A}B = A + B]$

Example 2.2.5 Simplify $\overline{AB} + \overline{AC} + \overline{ABC} + \overline{AB}C$

$= \overline{AB} + \overline{AC} + \overline{ABC} + \overline{AB}C$ Distributive
 $= \overline{AB} + \overline{AC} + \overline{AB}C$ Postulate 5(b) : $[A \cdot \bar{A} = 0]$
 $= \overline{AB} + \overline{AC} + \overline{AB}C$ Theorem 1(b) : $[A \cdot A = A]$
 $= \overline{AB} + \overline{A} + \bar{C} + \overline{AB}C$ DeMorgan's Theorem 1 : $[\overline{AB} = \bar{A} + \bar{B}]$
 $= \overline{A} + \bar{B} + \bar{C} + \overline{AB}C$ Theorem 5(a) : $[A + \bar{A}B = A + B]$
 $= \overline{A} + \overline{AB}C + B + \bar{C}$ Commutative
 $= \overline{A} + \bar{B}C + B + \bar{C}$ Theorem 5(a) : $[A + \bar{A}B = A + B]$
 Here $B = \bar{B}C$

$$\begin{aligned} &= \bar{A} + B + \bar{C} + \bar{B}C \\ &= \bar{A} + B + \bar{C} + \bar{B} \\ &= \bar{A} + \bar{C} + 1 \\ &= 1 \end{aligned}$$

Commutative
Theorem 5(a) : [A + $\bar{A}B$ = A + B]
Postulate 5(a) : [A + \bar{A} = 1]
Theorem 2(a) : [A + 1 = 1]

Example 2.2.6 Simplify $\bar{A}B + \bar{A} + AB$

Solution :

$$\begin{aligned} &= \bar{A} + \bar{B} + \bar{A} + AB \\ &= \bar{A} + \bar{B} + \bar{A} + B \\ &= \bar{A} + 1 \\ &= 1 \\ &= \bar{0} \\ &= 0 \end{aligned}$$

DeMorgan's Theorem 1 : [$\overline{AB} = \bar{A} + \bar{B}$]
Theorem 5(a) : [A + $\bar{A}B$ = A + B]
Theorem 1(a) : [A + A = A] and
Postulate 5(a) : [A + \bar{A} = 1]
Theorem 2(a) : [A + 1 = 1]

Example 2.2.7 Realize expression using minimum NAND gates only.

Solution :

$$\begin{aligned} y &= \bar{A}B + \bar{A}C + C + AD + \bar{A}BC + ABC \\ &= \bar{A}B(1+C) + \bar{A}C + C(1+AB) + AD \\ &= \bar{A}B + \bar{A}C + C + AD \quad \because 1+C=1 \text{ and } 1+AB=1 \\ &= \bar{A}B + A + C + AD \quad \because A + \bar{A}B = A + B \\ &= A(\bar{B} + 1 + D) + C \quad \because 1 + A = 1 \\ &= A + C \\ &= \overline{\bar{A} \cdot \bar{C}} \quad \because A = \bar{\bar{A}} \\ &= \bar{\bar{A} \cdot \bar{C}} \end{aligned}$$

Realization using NAND gates

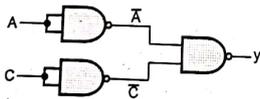


Fig. 2.2.4

Example 2.2.8 Prove the following using Boolean theorems.

- i) $[(C + \bar{C}D)(C + \bar{C}\bar{D})][AB + \bar{A}\bar{B} + A \oplus B] = C$
- ii) $\bar{A}BC + \bar{A}\bar{B}C + A\bar{B}C + ABC = AB + AC + BC$

Solution :

$$\begin{aligned} \text{i) } &[(C + \bar{C}D)(C + \bar{C}\bar{D})][AB + \bar{A}\bar{B} + A \oplus B] \\ &= [(C + D)(C + \bar{D})][AB + \bar{A}\bar{B} + A\bar{B} + \bar{A}B] \quad \dots A + \bar{A}B = A + B \\ &= [CC + C\bar{D} + CD + D\bar{D}][A(B + \bar{B}) + \bar{A}(\bar{B} + B)] \\ &= [C + C\bar{D} + CD][A + \bar{A}] \\ &= [C(1 + \bar{D} + D)] [A + \bar{A}] \quad \because A\bar{A} = 0 \text{ and } B + \bar{B} = 1 \\ &= [C(1 + \bar{D} + D)] [A + \bar{A}] \quad \because A + \bar{A} = 1 \\ &= C \quad \dots \text{Proved} \quad \because 1 + A = 1 \\ \text{ii) } &\bar{A}BC + \bar{A}\bar{B}C + A\bar{B}C + ABC \\ &= BC(\bar{A} + A) + AC(\bar{B} + B) + AB(\bar{C} + C) \\ &= BC + AC + AB \quad \because A + \bar{A} = 1 \\ &= AB + AC + BC \quad \dots \text{Proved} \end{aligned}$$

Example 2.2.9 Simplify : 1) $\bar{A}B + \bar{A}BC + \bar{A}BCD + \bar{A}BCDE$
2) $(P+Q+R)(\bar{P}+\bar{Q}+\bar{R})P$

GTU : May-14, Marks 8

Solution : 1) $\bar{A}B + \bar{A}BC + \bar{A}BCD + \bar{A}BCDE$

$$\begin{aligned} &= \bar{A}B(1 + \bar{C} + CD + CDE) \\ &= \bar{A}B \quad \because 1 + A = 1 \\ \text{2) } &(P+Q+R)(\bar{P}+\bar{Q}+\bar{R})P \\ &= (P \cdot \bar{P} + P \cdot \bar{Q} + P \cdot \bar{R} + \bar{P} \cdot Q + Q \cdot \bar{Q} + Q \cdot \bar{R} + \bar{P} \cdot R + \bar{Q} \cdot R + \bar{R} \cdot P)P \\ &= (P\bar{Q} + P\bar{R} + \bar{P}Q + Q\bar{R} + \bar{P}R)P \quad \dots \because A \cdot \bar{A} = 0 \\ &= P \cdot P\bar{Q} + P \cdot P\bar{R} + \bar{P} \cdot P\bar{Q} + P \cdot Q\bar{R} + \bar{P} \cdot P\bar{R} + P \cdot \bar{P}R \\ &= P\bar{Q} + P\bar{R} + P\bar{Q} + P\bar{R} \quad \dots \because A \cdot A = A \text{ and } A \cdot \bar{A} = 0 \\ &= P\bar{Q}(1+R) + P\bar{R}(1+Q) \quad \dots \because 1 + A = 1 \\ &= P\bar{Q} + P\bar{R} \quad \dots \because 1 + A = 1 \end{aligned}$$

Example 2.2.10 Simplify the following boolean functions to a minimum numbers of literals.

GTU : May-13, Marks 7

- a) $xyz + \bar{x}y + x\bar{y}z$ and
- b) $(A+B)(\bar{A}+B)$

Solution : a) $xyz + \bar{x}y + x\bar{y}z$

$$\begin{aligned} &= xy(z + \bar{z}) + \bar{x}y \\ &= xy + \bar{x}y \quad \dots \because A + \bar{A} = 1 \\ &= y(x + \bar{x}) \\ &= y \quad \dots \because A + \bar{A} = 1 \end{aligned}$$

b) $(A+B)(\overline{A+B})$

$$= \overline{A+B} + A+B$$

$$= \overline{A+B} + A+B$$

$$= \overline{A+B} + A+B$$

... De Morgan's theorem

... $\therefore A + \overline{A} = 1$

Example 2.2.11 Prove that: 1) $((\overline{AB} + ABC) + A(B + \overline{AB})) = 0$
 2) $ABC + \overline{A}BC + A\overline{B}C = AC + BC$

GTU : May-14, Marks 7

Solution : 1) $((\overline{A\overline{B}} + ABC) + A(B + \overline{A\overline{B}}))$

$$= (\overline{A\overline{B}} + ABC)(A(B + \overline{A\overline{B}}))$$

$$= (\overline{A\overline{B}} + ABC)(A(\overline{A\overline{B}} + B))$$

$$= (\overline{A\overline{B}} + ABC)(\overline{A} + A \cdot \overline{A\overline{B}})$$

$$= (\overline{A\overline{B}} + ABC)(\overline{A} + A \cdot \overline{A} \cdot \overline{\overline{B}})$$

$$= (\overline{A\overline{B}} + ABC)(\overline{A} + 0)$$

$$= (\overline{A\overline{B}} + ABC) \cdot \overline{A}$$

$$= 0$$

... $\therefore A \cdot \overline{A} = 0$

... $\therefore A \cdot \overline{A} = 0$, hence proved

2) L.H.S. = $A\overline{B}C + \overline{A}BC + ABC$

$$= A\overline{B}C + BC(\overline{A} + A)$$

$$= A\overline{B}C + BC$$

$$= C(A\overline{B} + B)$$

$$= C(A + B)$$

$$= AC + BC$$

... $\therefore A + \overline{A} = 1$

... $\therefore A + \overline{A}B = A + B$

Example 2.2.12 Find the complement of the following Boolean function and reduce to a minimum number of literals.

$\overline{BD} + \overline{ABC} + ACD + \overline{ABC}$

GTU : Dec.-12, Marks 7

Solution : $Y = \overline{BD} + \overline{ABC} + ACD + \overline{ABC}$

$Y = \overline{BD} + \overline{AB} + ACD$

$\overline{Y} = (B + \overline{D})(A + \overline{B})(\overline{A} + C + \overline{D})$

$= (AB + A\overline{D} + \overline{B}D)(\overline{A} + C + \overline{D})$

$= ABC + AB\overline{D} + A\overline{C}\overline{D} + A\overline{D} + \overline{A}\overline{B}D + \overline{B}C\overline{D} + \overline{B}D$

$= ABC + A\overline{D}(B + \overline{C} + 1) + \overline{B}D(\overline{A} + C + 1)$

$= ABC + A\overline{D} + \overline{B}D$

Example 2.2.13 Show that the dual of the EX-OR is equal to its complement.

GTU : May-13, Marks 7

Solution : $A \oplus B = A\overline{B} + \overline{A}B$

... equation of EX-OR

According to duality property,

$A \oplus \overline{B} = (\overline{A} + B) \cdot (A + \overline{B})$

... (i)

According to complement property,

$\overline{A \oplus B} = \overline{A\overline{B} + \overline{A}B}$

$= (\overline{A} + B) \cdot (A + \overline{B})$

... (ii)

\therefore From equation (i) and (ii) it is proved that duality of EX-OR is equal to its complement.

Example 2.2.14 Show that $A \odot B = AB + A'B' = (A \oplus B) = (A'B' + AB)$. Also construct the corresponding logic diagrams.

GTU : Summer-16, Marks 7

Solution : $A \odot B = A\overline{B} + \overline{A}B = (A\overline{B}) \cdot (\overline{A}B)$

$= (\overline{A} + \overline{B}) \cdot (\overline{A} + B) = (\overline{A} + B) \cdot (A + \overline{B})$

$= \overline{A}A + \overline{A}\overline{B} + AB + B\overline{B} = AB + \overline{A}\overline{B}$

$= A \odot B$

... Proved

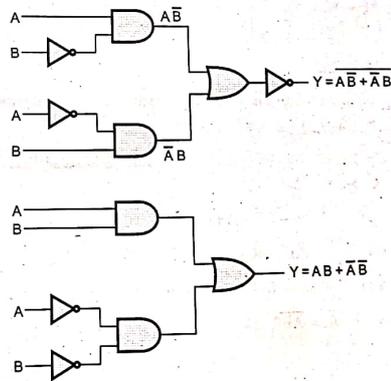


Fig. 2.2.5

Example 2.2.15 Design a NOT gate using a two input EX-OR gate.

GTU : Winter-16, Mark 1

Solution : EX-OR gate : $A \bar{B} + \bar{A} B$ considering one input say $B = 1$ we have,

$$Y = A \cdot (\bar{1}) + \bar{A} \cdot (1) = A \cdot 0 + \bar{A} = \bar{A}$$

Thus by connecting any one input to logic 1 two input EX-OR gate can be used as a NOT gate.

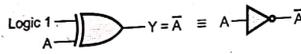


Fig. 2.2.6

Example 2.2.16 Show that $(A+C)(A+D)(B+C)(B+D) = AB+CD$.

GTU : Winter-16, Marks 3

Solution : L.H.S = $(A+C)(A+D)(B+C)(B+D)$
 $= [AA+AD+AC+CD][BB+BD+BC+CD]$
 $= [A+AD+AC+CD] \cdot [B+BD+BC+CD]$
 $= [A(1+D+C)+CD] \cdot [B(1+D+C)+CD]$
 $= (A+CD) \cdot (B+CD)$
 $= AB+ACD+BCD+CDCD$
 $= AB+ACD+BCD+CD$
 $= AB+CD(A+B+1)$
 $= AB+CD$

Example 2.2.17 Simplify using boolean laws and draw the logic diagram for the simplified expression. $F = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C$

GTU : Winter-14, Summer-17, Marks 4

Solution :

$$F = \overline{ABC} + \overline{ABC} + \overline{ABC} + A\overline{BC} + A\overline{BC}$$

$$= \overline{A+B+C} + \overline{A+C} + \overline{B+C} + \overline{A}B\overline{C} + A\overline{B+C} + A\overline{B+C}$$

$$= \overline{A}(1+C+B\overline{C}) + \overline{B}(1+C+A+AC) + \overline{C}(1+A)$$

$$= \overline{A} + \overline{B} + \overline{C} = \overline{ABC}$$

Logic Diagram :

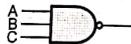


Fig. 2.2.7

Example 2.2.18 State and prove D'Morgan theorem for three variables.

Solution : 1) $ABC = \overline{\overline{A} + \overline{B} + \overline{C}}$ Demorgan's Theorem for 3 - variables

2) $\overline{A+B+C} = \overline{A} \overline{B} \overline{C}$

A	B	C	ABC	$\overline{A+B+C}$
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Same

A	B	C	$\overline{A+B+C}$	$\overline{A} \cdot \overline{B} \cdot \overline{C}$
0	0	0	1	1
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

Same

Example 2.2.19 Using laws of Boolean algebra prove that $AB + BC + A'C = \overline{AB} + A'C$.

GTU : Summer-18, Marks 7

Solution :

$$AB + BC + \overline{A}C = AB + BC(A + \overline{A}) + \overline{A}C(B + \overline{B})$$

$$= AB + ABC + \overline{A}BC + \overline{A}BC + \overline{A}B\overline{C}$$

$$= AB(1+C) + \overline{A}C(B+B\overline{B})$$

$$= AB + \overline{A}C \quad \dots \text{proved}$$

Example 2.2.20 Simplify the following Boolean functions to a minimum numbers of literals.

GTU : Winter-18, Marks 4

$$xyz + x'z + yz$$

Solution :

- $\overline{xy}z + \overline{xy}z + xy = \overline{x}z(\overline{y} + y) + xy = \overline{x}z + xy$
- $xy + \overline{x}z + yz = xy + \overline{x}z + yz(x + \overline{x})$
 $= xy + \overline{x}z + xyz + \overline{xy}z = xy(1+z) + \overline{x}z(1+y)$
 $= xy + \overline{x}z$

Review Questions

1. Define the following terms : Boolean variable, complement, literal.
2. State the fundamental postulates of Boolean algebra.
3. State various laws of Boolean algebra.
4. State the associative law of Boolean algebra.
5. State and prove DeMorgan's theorem with help of truth tables.
6. Explain the principle of duality with the help of example.
7. State and prove the postulates of Boolean algebra.
8. State and prove idempotent laws of Boolean algebra.
9. State De Morgan's theorems and prove with the help of truth table.

GTU : Dec.-13, Mark 1

GTU : Dec.-13, Marks 7

Summer-15, 18, Marks 4

Oral Questions and Answers

Q.1 What is a logic gate ?

Ans. : The logic gate is an electronic circuit that has one or more input binary variables but only one output. It is called logic gate because of its ability to operate on a number of binary inputs to perform a logical function, i.e. its output is a logical function of inputs.

Q.2 What are the basic digital logic gates ?

Ans. : The three basic logic gates are

- AND gate
- OR gate
- NOT gate

Q.3 Draw the logic symbol and construct the truth table of the following gates :

a) Three input OR gate b) Three input EX-NOR gate

Ans. : a) Three input OR gate :

Inputs			Output
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

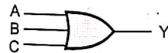


Fig. 2.1 Three input OR gate

Table 2.1 Truth table for three input OR gate

b) Three input EX-NOR gate :

Inputs			Output
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

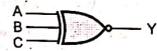


Fig. 2.2 Three input EX-NOR gate

Table 2.2 Truth table for three input EX-NOR

Q.4 Give the Boolean expression used for following gates

a) AND b) NOR c) EX-OR d) OR e) NOT

Ans. :

- AND : $Y = AB$
- NOR : $Y = \overline{A + B}$
- EX-OR : $Y = A\overline{B} + \overline{A}B = A \oplus B$
- OR : $Y = A + B$
- NOT : $Y = \overline{A}$

Q.5 Which gate is equal to AND-invert gate ?

Ans. : NAND gate.

Q.6 Which gate is equal to OR-invert gate ?

Ans. : NOR gate.

Q.7 Show that a bubbled AND gate works like a NOR gate.

Ans. :

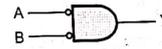


Fig. 2.3

A	B	\overline{A}	\overline{B}	Y
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

Here, output Y presents the output of NOR gate.

Q.8 What do you mean by literal ?
Ans. : Definition : In Boolean Function, the total number of variables in complemented or uncomplemented form are called literals.

For example : The function $F(A, B, C, D) = A + \overline{B}C + AC\overline{D}$ contains 4 literals.

Q.9 State two absorption properties of Boolean algebra.
Ans. : 1. $A + AB = A$. and $A(A + B) = A$

Q.10 State the associative law of Boolean algebra.
Ans. : Associative laws are as follows :

1. Law 1 (The associative law of addition) :

In the Oring of several variables, the result is the same regardless of the grouping of the variables. For three variables, A ORed with B OR C is the same as A OR B ORed with C.

i.e. $A + (B + C) = (A + B) + C$

2. Law 2 (The associative law of multiplication) :

It makes no difference in what order the variables are grouped when ANDing several variables. For three variables, A AND B ANDed with C is the same as A ANDed with B and C.

i.e. $(AB)C = A(BC)$

Q.11 Explain the De Morgan's theorem in Boolean algebra.
Ans. : Refer section 2.2.4.

Q.12 Explain the principle of duality with the help of example.
Ans. : The duality theorem says that, starting with a Boolean relation, you can derive another Boolean relation by -

1. Changing each OR sign to an AND sign
2. Changing each AND sign to an OR sign and
3. Complementing any 0 to 1 appearing in the expression.

For example : $A + 0 = A$. Using duality theorem, we can say that, $A \cdot 1 = A$.



3

Digital Logic Families

Contents

3.1	Introduction	Summer-18,	Marks 2
3.2	Characteristics of Digital ICs	Summer-15, 18,	Winter-15, 18,
			Marks 4
3.3	Transistor-Transistor Logic (TTL)	Winter-18,	Marks 3
3.4	CMOS Logic		
3.5	Interfacing of CMOS to TTL and TTL to CMOS		
3.6	Comparison between TTL and CMOS	Winter-15, Summer-18,	Marks 7
Oral Questions and Answers			

3.1 Introduction

A digital logic family is a group of compatible devices with the same logic levels and supply voltages. According to components used in the logic family, digital logic families are classified as shown in the Fig. 3.1.1.

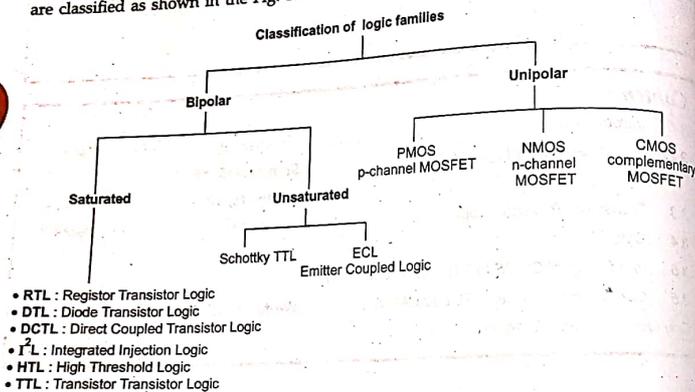


Fig. 3.1.1 Classification of logic families

Advantages of digital integrated circuits

1. ICs pack a lot more circuitry in a small package, so that the overall size of almost any digital system is reduced.
 2. The cost of ICs is very low, which makes them economical to operate.
 3. They have high reliability against failure, so the digital system needs less repair.
 4. Their reduced power consumption makes the digital system more economical to operate.
 5. The operating speed is higher, which makes them suitable for high-speed operations.
 6. The use of ICs reduces the number of external wiring connections because many of them are internal to the package.
- With the widespread use of ICs, it becomes necessary to know and understand the electrical characteristics of the IC logic families such as TTL and CMOS.

Review Questions

1. What is logic family? List out various logic families.
2. What are the advantages of digital integrated circuits?

GTU : Summer-18, Marks 2

3.2 Characteristics of Digital ICs

GTU : Summer-15, 18, Winter-15, 18

Propagation Delay

The propagation delay of a gate is basically the time interval between the application of an input pulse and the occurrence of the resulting output pulse.

- The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate.
- The shorter the propagation delay, the higher the speed of the circuit and vice-versa.
- The propagation delay is determined using two basic time intervals :
 1. t_{PLH} : It is the delay time measured when output is changing from logic 0 to logic 1 state (LOW to HIGH).
 2. t_{PHL} : It is the delay time measured when output is changing from logic 1 to logic 0 state (HIGH to LOW).
- When t_{PHL} and t_{PLH} are not equal, the larger value is considered as a propagation delay time for that logic gate, i.e.

$$t_p = \max(t_{PLH}, t_{PHL})$$

Power Dissipation

The amount of power that an IC dissipates is determined by the average supply current, I_{CC} , that it draws from the V_{CC} supply. It is the product of I_{CC} and V_{CC} .

- For ICs, the value of I_{CC} for a LOW gate output (I_{CCL}) is different from a HIGH output (I_{CCH}).
- Average I_{CC} is determined based on the 50 % duty cycle operation of the gate (LOW half of the time and HIGH half of the time).

$$I_{CC(avg)} = \frac{I_{CCH} + I_{CCL}}{2}$$

- Average power dissipation as,

$$P_{D(avg)} = I_{CC(avg)} \times V_{CC}$$

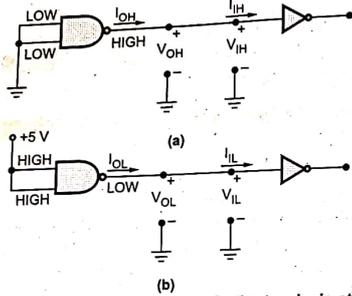


Fig. 3.2.1 Currents and voltages in the two logic states

Current and Voltage Parameters

$V_{IH(min)}$ - High-Level Input Voltage : It is the minimum voltage level required for a logical 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

$V_{IL(max)}$ - Low-Level Input Voltage : It is the maximum voltage level required for a logic 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic circuit.

$V_{OH(min)}$ - High-Level Output Voltage : It is the minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.

$V_{OL(max)}$ - Low-Level Output Voltage : It is the maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

I_{IH} - High-Level Input Current : It is the current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL} - Low-Level Input Current : It is the current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH} - High-Level Output Current : It is the current that flows from an output in the logical 1 state under specified load conditions.

I_{OL} - Low-Level Output Current : It is the current that flows from an output in the logical 0 state under specified load conditions.

Note The current directions shown in the Fig. 3.2.1 may be opposite to those shown depending on the logic family.

Noise Margin and Logic Voltages Levels

- In digital circuits, the binary 0 and 1 are represented by a pair of voltage levels.
- Each logic family has a different standard. The Table 3.2.1 shows the voltages used by several families.
- These are the ideal voltage levels. But in practice, it is difficult to get these ideal voltages.
- Stray electric and magnetic field can induce voltages on the connecting wires between logic circuits. These unwanted signals are called noise and can sometimes cause the voltage at the input to a logic circuit to drop below $V_{IH(min)}$ or rise above $V_{IL(max)}$, which could produce unpredictable operation.
- The noise immunity of a logic circuit refers to the circuit's ability to tolerate the noise without causing spurious changes in the output voltage. To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept at a few fraction of volts below $V_{OH(min)}$ and voltage level $V_{IL(max)}$ is kept above $V_{OL(max)}$, at the design time. This is illustrated in Fig. 3.2.2.

Family	Logic 0	Logic 1
TTL	0 V	+ 5 V
ECL	- 1.7 V	- 0.9 V
CMOS	0 V	3 - 15 V

Table 3.2.1

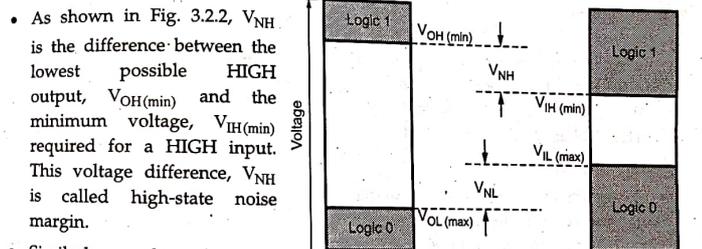


Fig. 3.2.2 Noise margins

- As shown in Fig. 3.2.2, V_{NH} is the difference between the lowest possible HIGH output, $V_{OH(min)}$ and the minimum voltage, $V_{IH(min)}$ required for a HIGH input. This voltage difference, V_{NH} is called high-state noise margin.
- Similarly, we have low-state noise margin. It is the voltage difference between the largest possible low output, $V_{OL(max)}$ and the maximum voltage, $V_{IL(max)}$ required for a LOW input.
- In short we can write as,

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$
 and

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$
- The noise margin allows the digital circuit to function properly if noise voltages are within the limits of V_{NH} and V_{NL} for a particular logic family.

Fan-In and Fan-out

- In a digital system, we typically find many types of digital ICs interconnected to perform various functions. In these situations, the output of a logic gate may be connected to the inputs of several other similar gates. The maximum number of inputs of several gates that can be driven by the output of a logic gate is decided by the parameter called **fan-out**. In general, the fan-out is defined as the maximum number of inputs of the same IC family that the gate can drive maintaining its output levels within the specified limits. For example, a logic gate with fan-out 10 can drive maximum 10 logic inputs from the same family. It depends on current sourcing and sinking capacity of input and output signals of same IC family.
- The **fan-in** of a digital logic gate refers to the number of inputs. For example, an inverter has a fan-in of 1, a 2-input NOR gate has a fan-in of 2, a 4-input NAND gate has a fan-in of 4 and so on. A logic designer has to select the fan-in of the gate to accommodate the number of inputs. At the hardware level, however, the fan-in provides information about the intrinsic speed of the gate itself. In general, the propagation delay increases with the fan-in. This means that 2-input NAND gate is faster than the 4-input NAND if both are from same logic family.

Current Sinking

- A device output is said to **sink current** when current flows from the power supply, through the load and through the device output to ground. This is illustrated in Fig. 3.2.3 (a).

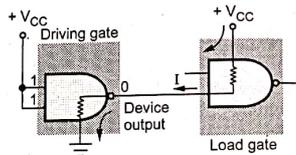


Fig. 3.2.3 (a) Current sinking

Current Sourcing

- A device output is said to **source current** when current flows from the power supply, out of the device output and through the load to ground. This is illustrated in Fig. 3.2.3 (b).

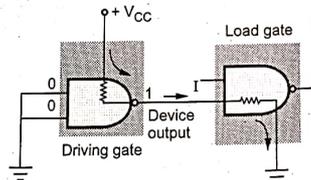


Fig. 3.2.3 (b) Current sourcing

Speed Power Product (Figure of Merit)

- In general, for any digital IC, it is desirable to have shorter propagation delays (higher speed) and lower values of power dissipation. There is usually a trade-off between switching speed and power dissipation in the design of a logic circuit i.e. speed is gained at the expense of increased power dissipation. Therefore, a common means for measuring and comparing the overall performance of an IC family is the **Speed-Power Product (SPP)**. It is also called **Figure of Merit**.

Illustrative Examples

Example 3.2.1 If a manufacture specifies the minimum logical 1 at a gate output a 4.0 V and also specifies that any voltage done up to 3.6 V will be considered as logical 1, find the noise margin.

Solution : Given : $V_{OH(min)} = 4.0 \text{ V}$ and $V_{IH(min)} = 3.6 \text{ V}$
 \therefore Noise margin = $V_{OH(min)} - V_{IH(min)} = 4.0 \text{ V} - 3.6 \text{ V} = 0.4 \text{ V}$

Example 3.2.2 Determine the fan-out given $I_{IH(max)} = 40 \mu\text{A}$ and $I_{OH(max)} = 400 \mu\text{A}$.

Solution : Fan-out = $\frac{I_{OH(max)}}{I_{IH(max)}} = \frac{400 \mu\text{A}}{40 \mu\text{A}} = 10$

Example 3.2.3 A certain gate draws 2 mA when its output is high and 3.6 mA when its output is low. What is the average power dissipation if V_{CC} is 5 V and it is operated on a 50 % duty cycle ?

Solution : Given $I_{OH} = 2 \text{ mA}$
 $I_{OL} = 3.6 \text{ mA}$
 $P_D = \frac{2 \text{ mA} + 3.6 \text{ mA}}{2} \times 5 = 2.8 \text{ mA} \times 5 = 14 \text{ mW}$

Example 3.2.4 For a certain IC family, propagation delay is 10 ns with an average power dissipation of 6 mW. What is its speed power product ?

Solution : The speed-power product is given as,
 $SPP = \text{Propagation delay} \times \text{Average power dissipation}$
 $= 10 \text{ ns} \times 6 \text{ mW} = 60 \text{ pico joules (pJ)}$

Example 3.2.5 If $V_{CC} = 5 \text{ V}$, $I_{CC(0)} = 22 \text{ mA}$, $I_{CC(1)} = 8 \text{ mA}$, $V_{OH} = 2.4 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{OL} = 0.45 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $t_{PHL} = 15 \text{ nsec}$, $t_{PLH} = 22 \text{ nsec}$, $I_{IH} = 40 \mu\text{A}$, $I_{OH} = 5.2 \text{ mA}$, calculate :
 i) Noise margin logic 1 and logic 0. ii) Power dissipation.
 iii) Propagation delay and figure of merit. iv) Fan-out.

Solution :

i) Noise margin logic 1

$$V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 \text{ V} - 2 \text{ V}$$

$$V_{NH} = 0.4 \text{ V}$$

Noise margin logic 0

$$V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.8 \text{ V} - 0.45 \text{ V}$$

$$V_{NL} = 0.35 \text{ V}$$

ii) Power dissipation = $I_{CC(av)} \times V_{CC}$

$$I_{CC(av)} = \frac{I_{CC(0)} + I_{CC(1)}}{2} = 15 \text{ mA}$$

∴ Power dissipation = $15 \text{ mA} \times 5 \text{ V} = 75 \text{ mW}$

iii) Propagation delay

$$t_p = \max(t_{PLH}, t_{PHL})$$

$$t_p = t_{PLH} = 22 \text{ nsec}$$

OR $t_p = \frac{1}{2}(t_{PLH} + t_{PHL}) = \frac{1}{2}(22 + 15) \text{ nsec} = 18.5 \text{ nsec}$

Figure of merit = $SPP = \text{Delay} \times \text{Power dissipation} = 18.5 \text{ nsec} \times 75 \text{ mW}$
 = 1387.5 pico joule

iv) Fan-out = $\frac{I_{OH(max)}}{I_{IH(max)}} = \frac{5.2 \text{ mA}}{40 \mu\text{A}} = 130$

Review Questions

- List various characteristics of digital ICs and explain their significance in brief.
- Define 1) V_{OH} , V_{IL} 2) V_{OL} , V_{IH} 3) Noise margin.
- Define fan-out.
- Define fan-in.
- What is propagation delay ?
- What is noise margin ?
- Define current sinking and current sourcing.
- What is speed power product ? List the characteristics of digital ICs.

GTU : Summer-18, Marks 2

- Explain following characteristics of logic families with examples :
 i) Figure of merit ii) Fan-out iii) Voltage parameters iv) Speed v) Noise margin.
- Explain parameter's of logic families.
- Explain the current parameters of logic families.
- Define followings with respect to logic families.
 i) Fan in ii) Fan out iii) Noise Margin iv) Propagation delay

GTU : Summer-15, Marks 4

- Define fan-out.
- Explain following terms w.r.t. Digital Logic Family : 1) Fan - in 2) Noise Margin 3) Power Dissipation.

GTU : Winter-15, Mark 1
 GTU : Winter-18, Marks 3

3.3 Transistor-Transistor Logic (TTL)

GTU : Winter-18

- Transistor transistor logic, TTL, is named for its dependence on transistors alone to perform basic logic operations. The first version, which is now known as standard TTL, was developed in 1965 and is rarely used in today's systems. Through the years, the basic design has been modified to improve its performance in several respects and as a consequence, a number of subfamilies have evolved.

3.3.1 2-Input TTL NAND Gates

- The Fig. 3.3.1 (a) shows the circuit diagram of 2-input NAND gate.
- Its input structure consists of multiple-emitter transistor and output structure consists of totem-pole output.
- Q_1 is an NPN transistor having two emitters, one for each input to the gate.
- Although this circuit looks complex, we can simplify its analysis by using the diode equivalent of the multiple-emitter transistor Q_1 , as shown in Fig. 3.3.1 (b).

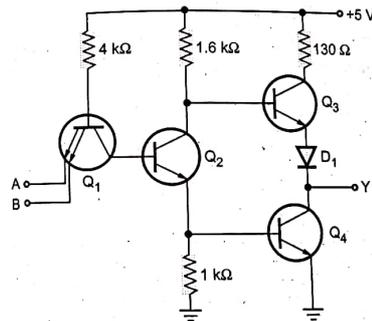


Fig. 3.3.1 (a) Two input TTL NAND gate

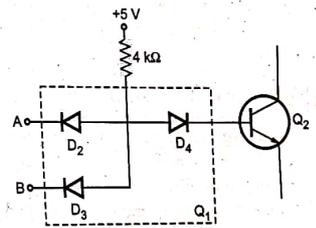


Fig. 3.3.1 (b) Diode equivalent for Q_1

- Diodes D_2 and D_3 represent the two E-B junctions of Q_1 and D_4 is the collector-base (C-B) junction.
- The input voltages A and B are either LOW (ideally grounded) or HIGH (ideally +5 volts).
- If either A or B or both are low, the corresponding diode conducts and the base of Q_1 is pulled down to approximately 0.7 V. This reduces the base voltage of Q_2 to almost zero. Therefore, Q_2 cuts off. With Q_2 open, Q_4 goes into cut-off and the

Q_3 base is pulled HIGH. Since Q_3 acts as an emitter follower, the Y output is pulled up to a HIGH voltage.

- When A and B both are HIGH, the emitter diode of Q_1 are reversed biased making them off. This causes the collector diode D_4 to go into forward conduction. This forces Q_2 base to go HIGH. In turn, Q_4 goes into saturation, producing a low output.
- Table 3.3.1 summarizes all input and output conditions.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 3.3.1 Truth table for 2-input NAND gate

- Without diode D_1 in the circuit, Q_3 will conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of Q_3 reverse-biased. In this way, only Q_4 conducts when the output is low.

3.3.2 3-Input TTL NAND Gate

- The Fig. 3.3.2 shows the three input TTL NAND gate. It is same as that of two input TTL NAND gate except that its Q_1 (NPN) transistor has three emitters instead of two.
- For three input NAND gate if all the inputs are logic 1 then and then only output is logic 0; otherwise output is logic 1. The operation is similar to the 2-input NAND gate.
- The Table 3.3.2 shows the truth table for 3-input NAND gate. (See Table 3.3.2 on next page)

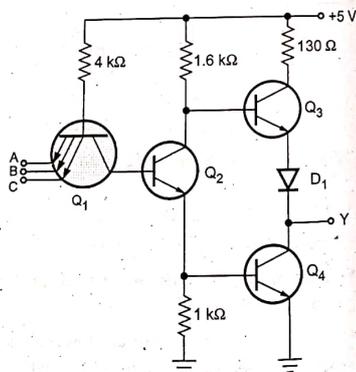


Fig. 3.3.2 Three input TTL NAND gate

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 3.3.2 Truth table of 3-input NAND gate

3.3.3 Totem-Pole Output / Active Pull-Up

- Fig. 3.3.3 shows a highlighted output configuration. Transistor Q_3 and Q_4 form a totem-pole. Such a configuration is known as active pull-up or totem pole output.

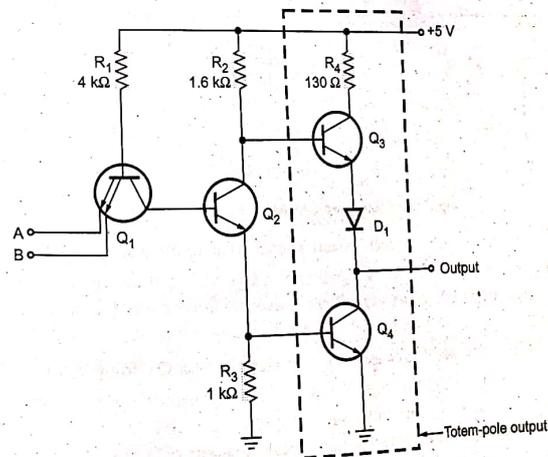


Fig. 3.3.3 Two input NAND gate with totem-pole output

- The active pull-up formed by Q_3 and Q_4 has specific advantage. Totem-pole transistors are used because they produce a LOW output impedance. Either Q_3 acts as an emitter follower (HIGH output), or Q_4 is saturated (LOW output). When Q_3 is conducting, the output impedance is approximately 70Ω ; when Q_4 is saturated, the output impedance is only 12Ω . Either way, the output impedance is low.
- The output voltage can change quickly from one state to the other because any stray output capacitance is rapidly charged or discharged through the low output impedance. Thus the propagation delay is low in totem-pole TTL logic.
- Fig. 3.3.4 shows static analysis of one gate in a 7400 quad 2-input NAND gate, including the totem-pole output.

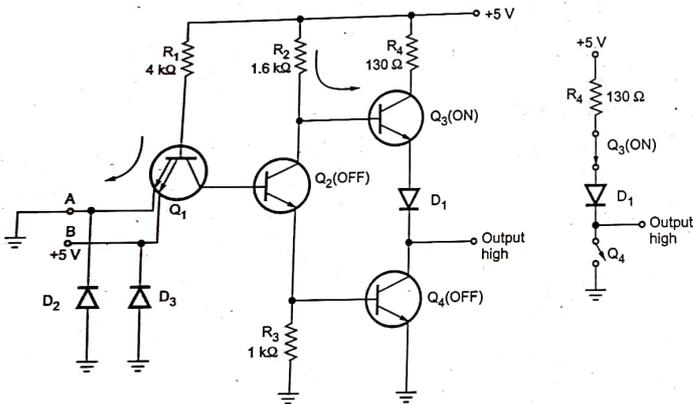


Fig. 3.3.4 Static analysis when output is HIGH

- Diodes D_2 and D_3 have been added at the input terminals. These diodes protect the circuit from large negative transients on input lines. If an input attempts to go more than about 1 V negative, the protective diode conducts like a short circuit to ground.
- $A = 0 \text{ V}$ and $B = +5 \text{ V}$, this makes Q_1 to conduct and Q_2 to switch off. Since Q_2 is like an open switch, no current flows through it. Instead, current flows through the $1.6 \text{ k}\Omega$ resistor and into the base of Q_3 , turning it ON. Q_4 remains off because there is no path through which it can receive base current.

- The equivalent switches in the totem-pole under these conditions are shown in the Fig. 3.3.5. The output current, I_L flows through R_4 (130Ω) and diode D_1 . Therefore, the HIGH output voltage is given as,

$$V_{OH} = V_{CC} - V_{CE(sat)} - V_D - I_L \times (130 \Omega)$$
 where V_D is the forward drop across diode D_1 , about 0.7 V .
 $V_{CE(sat)}$ is the saturation voltage of Q_3 , about 0.1 V .

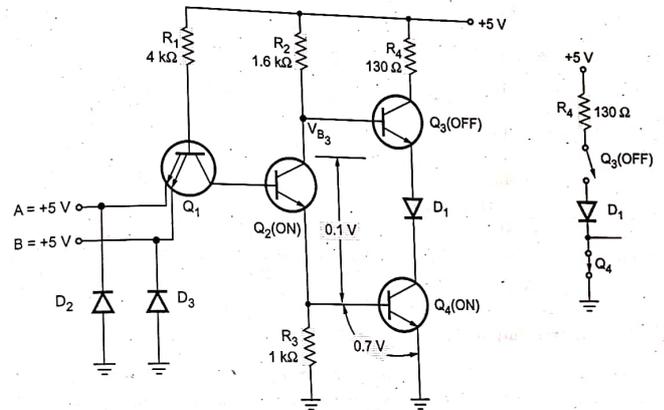


Fig. 3.3.5 Static analysis when output is LOW

- We have seen that when both inputs are HIGH Q_2 is ON and it drives Q_4 turning it ON. Note that in this condition the voltage at the base of Q_3 equals the sum of the base-to-emitter drop of Q_4 and the $V_{CE(sat)}$ of Q_2 .

$$V_{B3} = V_{BE}(Q_4) + V_{CE(sat)}(Q_2) = 0.7 \text{ V} + 0.1 \text{ V} = 0.8 \text{ V}$$
- Now we can easily understand the purpose of diode D_1 . It does not allow base-emitter junction of Q_3 to be forward-biased and thus ensures that Q_3 remains OFF when Q_4 is ON.

Example 3.3.1 A two input NAND gate has $V_{CC} = +5 \text{ V}$ and $1 \text{ k}\Omega$ load connected to its output. Calculate the output voltage
 a) When both inputs are LOW b) When both inputs are HIGH.

Solution : a) When both inputs of NAND gate are LOW, the output is HIGH and it is given as,

$$V_{OH} = V_{CC} - V_{CE(sat)} - V_D - I_L \times (130 \Omega) = 5 - 0.1 - 0.7 - I_L (130 \Omega) = 4.2 \text{ V} - I_L (130 \Omega) \quad \dots (1)$$

where the load current is,

$$I_L = \frac{V_{OH}}{R_L} = \frac{V_{OH}}{1 \text{ k}\Omega}$$

Substituting for I_L in the equation (1) we get,

$$V_{OH} = 4.2 \text{ V} - \frac{V_{OH}}{1 \text{ k}\Omega} (130 \Omega)$$

$$\therefore V_{OH} + \frac{130 V_{OH}}{1000} = 4.2$$

$$\therefore 1130 V_{OH} = 4200$$

$$\therefore V_{OH} = \frac{4200}{1130} = 3.716 \text{ V}$$

b) When both inputs of NAND gate are HIGH, the output is LOW and it is given as,

$$V_{OL} = V_{CE(sat)} \approx 0.1 \text{ V}$$

3.3.4 Input and Output Currents

- We have seen that TTL output stage is a totem pole. It consists of two transistors Q_3 and Q_4 . When Q_3 is ON, the output is HIGH and it supplies current I_{IH} to drive the load. Hence Q_3 is called a pull-up transistor. When Q_4 is ON, the output is low and it draws current from the load to pull the load voltage down. Hence transistor Q_4 is called a pull-down transistor.
- Since current flows out of the totem pole when the output is HIGH, Q_3 acts as a current source to a load. When the output is low, current flows into Q_4 , and we say that Q_4 is a current sink.
- Fig. 3.3.6 shows the output stage of the TTL driver connected to the input stage of the TTL load.
- In Fig. 3.3.6 (a) the driver output is low and Q_4 sinks current from the forward biased base-emitter junction of the input transistor of the load. This current is approximately 1.6 mA, and is designated I_{OL} at the output and I_{IL} at the input.
- In Fig. 3.3.6 (b) the driver output is HIGH and Q_3 source current to the load. It is small leakage current supplied to the reverse biased emitter base junction of the

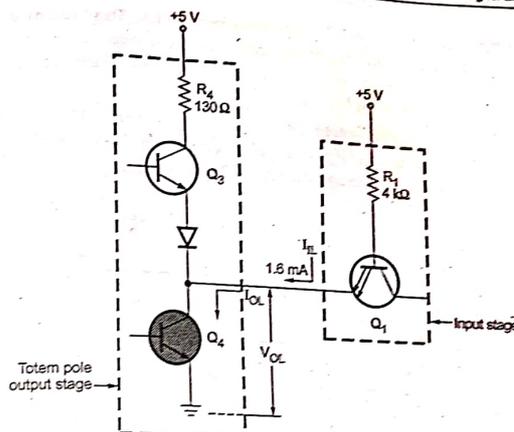


Fig. 3.3.6 (a) Q_4 acting as a current sink when output is LOW

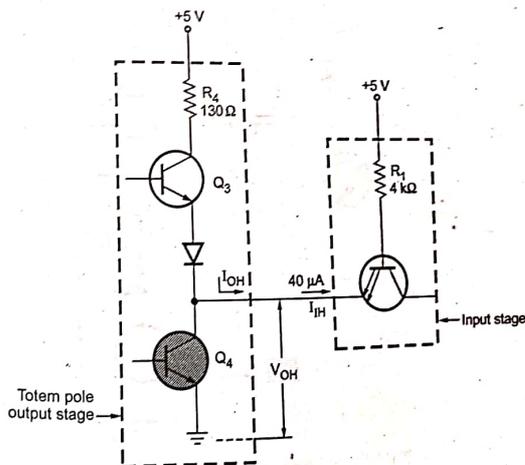


Fig. 3.3.6 (b) Q_3 acting as a current source when output is HIGH

input transistor of the load. It is approximately 40 μA . This current is designated as I_{OH} at the output and I_{IH} at the input. By convention current flowing into a device is positive and current flowing out is negative. Therefore, manufacturers specify negative values for I_{OH} and I_{IL} .

- Fig. 3.3.7 shows a TTL output connected to the several TTL loads. When the output is HIGH, it is necessary to supply load current (I_{IH}) to each TTL load, so Q_3 must be capable of sourcing the sum of these currents.

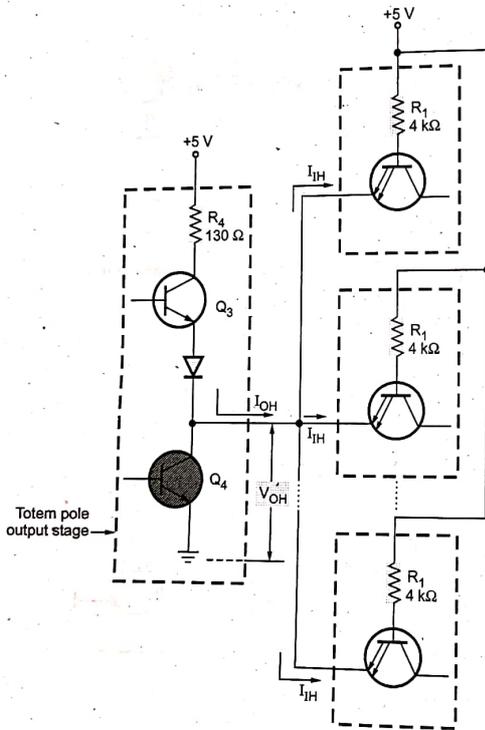


Fig. 3.3.7 (a) When output is HIGH

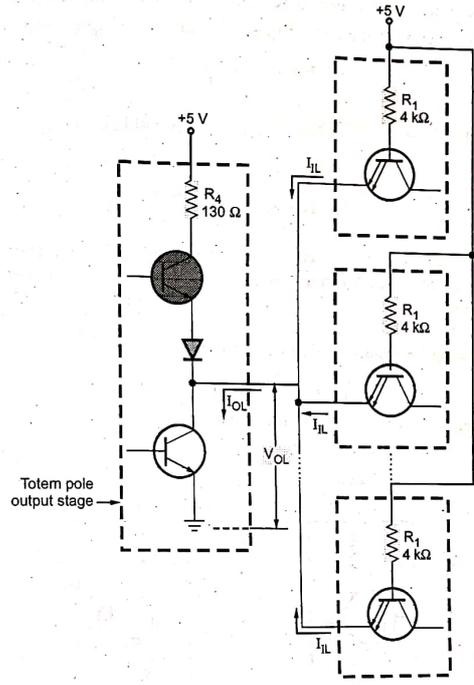


Fig. 3.3.7 (b) When output is LOW

- Fan-out is the maximum number of loads belonging to same family that a logic gate can drive,

So
$$\text{Fan-out} = \frac{|I_{OH(max)}|}{I_{IH(max)}}$$

- For standard TTL, $I_{OH(max)} = -400 \mu\text{A}$ and $I_{IH(max)} = 40 \mu\text{A}$.

Therefore,

$$\text{Fan-out} = \frac{|-400 \mu\text{A}|}{40 \mu\text{A}} = 10$$

- When the output is low, each load supplies current to the totem pole, so Q_4 must be capable of sinking the sum of these currents. In this case, fan-out is defined as,

$$\text{Fan-out} = \frac{I_{OL(max)}}{|I_{IL(max)}|}$$

- For standard TTL,

$$I_{OL(max)} = 16 \text{ mA and } I_{IL(max)} = -1.6 \text{ mA}$$

Therefore,

$$\text{Fan-out} = \frac{16 \text{ mA}}{|-1.6 \text{ mA}|} = 10$$

- We have seen that fan-out can be determined in two ways. Here, in both cases fan-out is 10. But if they differ, the actual fan-out is always the smaller of the two computations.

3.3.5 Wired Logic - Open Collector Output

- One problem with totem pole output is that two outputs cannot be tied together.
- See the Fig. 3.3.8, where the totem pole outputs of two separate gates are connected together at point X.

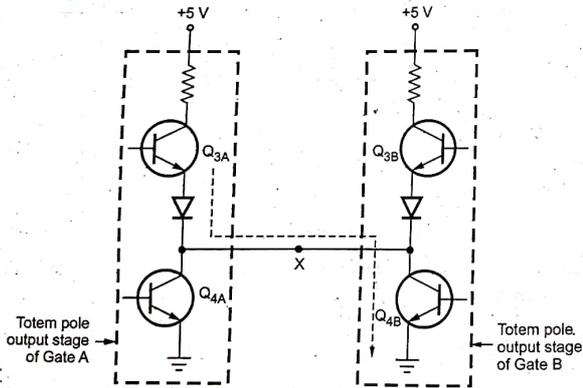


Fig. 3.3.8 Totem-pole outputs tied together can produce harmful current

- Suppose that the output of gate A is high (Q_{3A} ON and Q_{4A} OFF) and the output of gate B is low (Q_{3B} OFF and Q_{4B} ON). In this situation transistor Q_{4B} acts as a load for Q_{3A} .

- Since Q_{4B} is a low resistance load, it draws high current around 55 mA. This current might not damage Q_{3A} or Q_{4B} immediately, but over a period of time can cause overheating and deterioration in performance and eventual device failure.

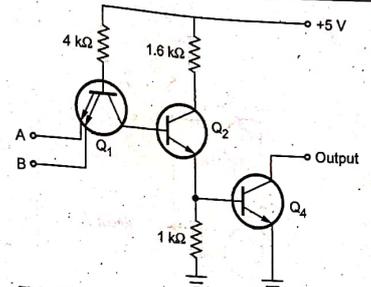


Fig. 3.3.9 Open collector 2-input TTL NAND gate

- Some TTL devices provide another type of output called open collector output. The outputs of two different gates with open collector output can be tied together. This is known as wired logic.

- Fig. 3.3.9 shows a 2-input NAND gate with an open-collector output eliminates the pull-up transistor Q_3 , D_1 and R_4 . The output is taken from the open collector terminal of transistor Q_4 .

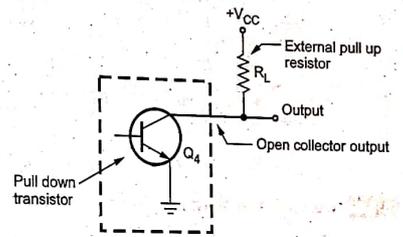


Fig. 3.3.10 Open collector output with pull-up resistor

- Because the collector of Q_4 is open, a gate like this will not work properly until you connect an external pull-up resistor, as shown in Fig. 3.3.10.
- When Q_4 is ON, output is low and when Q_4 is OFF output is tied to V_{CC} through an external pull up resistor.
- As mentioned earlier, the open collector outputs of two or more gates can be connected together, as shown in the Fig. 3.3.11 (a). The connection is called a wired-AND and represented schematically by the special AND gate symbol as shown in Fig. 3.3.11 (b). (See Fig. 3.3.11 on next page)

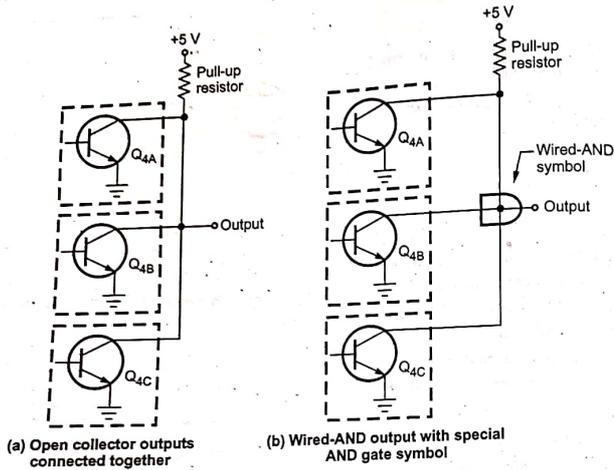


Fig. 3.3.11

3.3.6 Comparison between Totem-Pole and Open-Collector Outputs

Table 3.3.3 summarizes the difference between totem-pole and open collector outputs.

Sr. No.	Totem-pole	Open collector
1.	Output stage consists of pull-up transistor (Q_3), diode resistor and pull-down transistor (Q_4).	Output stage consists of only pull-down transistor.
2.	External pull-up resistor is not required.	External pull-up resistor is required for proper operation of gate.
3.	Output of two gates cannot be tied together.	Output of two gates can be tied together using wired AND technique.
4.	Operating speed is high.	Operating speed is low.

Table 3.3.3 Comparison of totem-pole and open collector output

3.3.7 Standard TTL Characteristics

Let us see the characteristics of standard TTL family.

Supply voltage and temperature range

- Both the 74 series and 54 series operate on supply voltage of 5 V.
 - The 74 series works reliably over the range 4.75 V to 5.25 V, while the 54 series can tolerate a supply variation of 4.5 to 5.5 V.
 - The 74 series devices are guaranteed to work reliably over a temperature range of 0 to 70°C where as 54 series devices can handle temperature variations from -55 to +125°C.
- From the above values we can say that 54 series devices have greater tolerance of voltage and temperature variations. Hence, these devices are used where it is necessary to maintain reliable operation over an extreme range of conditions. For example, in military and space application.
 - The only disadvantage of these devices is that they are expensive.

Voltage levels and noise margin

Table 3.3.4 shows the input and output logic voltage levels for the standard 74 series. The minimum and maximum values shown in the Table 3.3.4 are for worst case conditions of power supply, temperature and loading conditions.

Voltages	Minimum	Typical	Maximum
V_{OL}	-	0.2	0.4
V_{OH}	2.4	3.4	-
V_{IL}	-	-	0.8
V_{IH}	2.0	-	-

Table 3.3.4 Voltage levels

- In the worst case, there is difference of 0.4 V between the driver output voltages and the required load input voltages. For instance, the worst-case low values are

$$V_{OL(max)} = 0.4 \text{ V driver output}$$

$$V_{IL(max)} = 0.8 \text{ V load input}$$

Similarly, the worst-case high values are

$$V_{OH(min)} = 2.4 \text{ V driver output}$$

$$V_{IH(min)} = 2 \text{ V load input}$$

In either case, the difference is 0.4 V. This difference is called *noise margin*.

- For TTL, Low state noise margin, V_{NL} and high state noise margin, V_{NH} both are equal and 0.4 V. This is illustrated in Fig. 3.3.12. It provides built-in protection against noise. It ensures reliable operation of the device for induced noise voltages less than 0.4 V. (See Fig. 3.3.12 on next page)

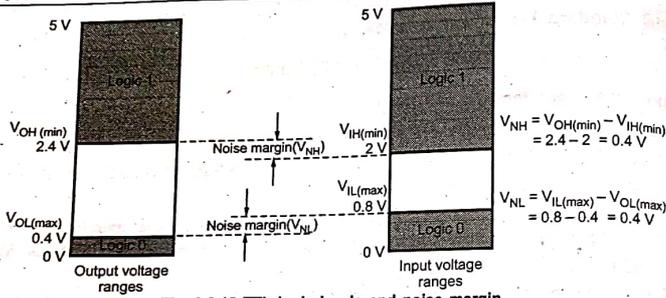


Fig. 3.3.12 TTL logic levels and noise margin

Power dissipation

A standard TTL gate has an average power dissipation of about 10 mW. It may vary from this value because of signal levels, tolerances etc.

Propagation delay

The propagation delay time is the time it takes for the output of a gate to change after the inputs have changed. The propagation delay time of a TTL gate is approximately 10 nanoseconds.

Fan-out

A standard TTL output can typically drive 10 standard TTL inputs. Therefore, standard TTL has fan-out 10.

Table 3.3.5 summarizes the characteristics of standard TTL (74XX).

Characteristics	Values
Supply voltage	For 74 series - (4.75 to 5.25) units For 54 series - (4.5 to 5.5) units
Temperature range	For 74 series - (0 °C to 70 °C) For 54 series - (-55 °C to 125 °C)
Voltage levels	$V_{OL(max)}$ - 0.4 V $V_{OH(min)}$ - 2.4 V $V_{IL(max)}$ - 0.8 V $V_{IH(min)}$ - 2.0 V
Noise margin	0.4 V
Power dissipation	10 mW per gate
Propagation delay	Typically 10 ns
Fan-out	10

Table 3.3.5 Standard TTL characteristics

3.3.8 Advantages and Disadvantages of TTL Family

Advantages of TTL

1. High speed operation. Fastest among the saturated logic families. The propagation delay time is about 10 ns.
2. Moderate power dissipation.
3. Available in commercial and military versions.
4. Available for wide range of functions.
5. Low cost.
6. Moderate packaging density.

Disadvantages of TTL

1. Higher power dissipation than CMOS.
2. Lower noise immunity than CMOS.
3. Less fan-out than CMOS.

3.3.9 Unconnected Inputs

If any input of TTL gate is left open or unconnected, then the corresponding base emitter junction of the input transistor Q_1 is reverse biased. See Fig. 3.3.13 (a). Therefore, the open or unconnected input behaves exactly same way as if a logic 1 is applied to that input. Thus, in TTL ICs all the unconnected inputs are treated as logic 1. However, it is recommended that the unused inputs should be either connected to some used input or tied to V_{CC} through pull-up resistor, as shown in the Fig. 3.3.13 (b).

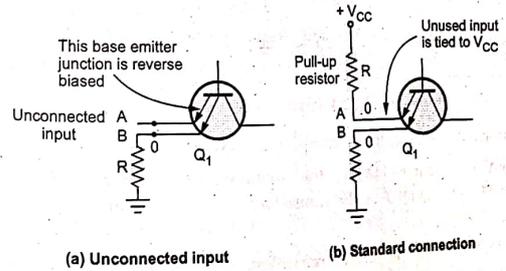


Fig. 3.3.13

3.3.10 Tri-State TTL Inverter

- The tristate configuration is a third type of TTL output configuration.
- It utilizes the high-speed operation of the totem-pole arrangement while permitting outputs to be wired-ANDed (connected together).
- It is called tristate TTL because it allows three possible output stages : HIGH, LOW and high-impedance.
- Transistor Q_3 is ON when output is HIGH and Q_4 is ON when output is LOW.
- In the high impedance state both transistors, transistors Q_3 and Q_4 in the totem-pole arrangement are turned OFF. As a result, the output is open or floating, it is neither LOW nor HIGH.
- Fig. 3.3.14 shows the simplified circuit for tristate inverter. It has two inputs A and E.

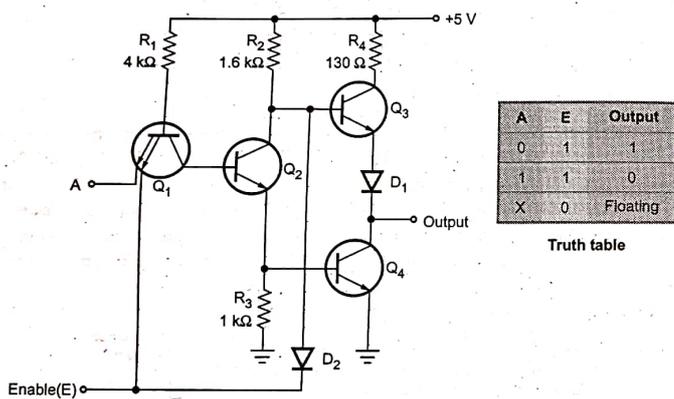


Fig. 3.3.14 Tristate TTL inverter

A	E	Output
0	1	1
1	1	0
X	0	Floating

Truth table

- A is the normal logic input whereas E is an ENABLE input.
- When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state of the transistor Q_1 (either ON or OFF) depends on the logic input A.
- When ENABLE input is LOW, regardless of the state of logic input A, the base-emitter junction of Q_1 is forward biased and as a result it turns ON.
- This shunts the current through R_1 away from Q_2 making it OFF.

- As Q_2 is OFF, there is no sufficient drive for Q_4 to conduct and hence Q_4 turns OFF.
- The LOW at ENABLE input also forward-biases diode D_2 , which shunt the current away from the base of Q_3 , making it OFF.
- In this way, when ENABLE input is LOW, both transistors are OFF and output is at high impedance state.

Transfer characteristics

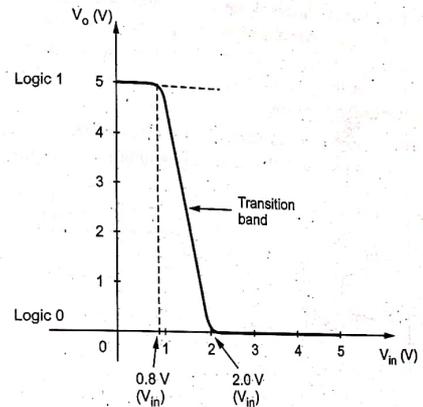


Fig. 3.3.15 Transfer characteristics of TTL inverter

- Fig. 3.3.15 shows transfer characteristics of TTL inverter.
- For $V_{in} \leq V_{IL(max)}$ ($V_{in} \leq 0.8$ V), the output voltage is High (5 V).
- For $V_{IL(max)} < V_{in} \leq V_{IH(min)}$ the output voltage is undefined.
- For $V_{in} \geq V_{IH(min)}$ ($V_{in} \geq 2.0$ V), the output voltage is low (0 V).

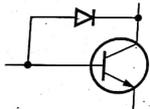
3.3.11 Schottky TTL

With standard TTL, high-speed TTL and low-power TTL, when transistors are ON, they are driven into hard saturation. This causes a surplus of carriers to be stored in the base. This excess charge carriers in the base region must be removed before the transistors is switched from ON to OFF. The time required to remove these carriers, called storage time, is responsible for high propagation delays or low switching times.

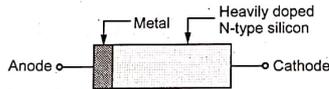
One way to counter this problem is to prevent the transistor from going into deep saturation when it is turned ON i.e. to restrict the forward bias of its base-to-collector junction to few tenths of a volt. This can be accomplished by connecting a diode across the base-to-collector junction, as shown in the Fig. 3.3.16 (a). The diode does not allow to increase the forward bias voltage at base-to-collector junction above its cut-in voltage. In other words, it clamps base-to-collector voltage upto its small cut-in voltage. As a result the junction cannot be heavily forward biased and the transistor is kept out of deep saturation.

We know that germanium diodes have less cut-in voltage but they cannot be fabricated in silicon integrated circuits. The Schottky diode, consisting of a silicon-metal junction with a cut-in voltage of 0.3 to 0.4 volts is ideal for this purpose. Fig. 3.3.16 (b) and (c) show the construction, and Fig. 3.3.16 (d) and (e) show Schottky clamped NPN transistor and its symbol.

Another important parameter of Schottky diode is that it has very little capacitance and fast recovery time. So it can be switched rapidly without storage time delays.



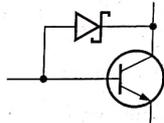
(a) Transistor with clamping diode



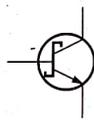
(b) Schottky diode construction



(c) Schottky diode symbol



(d) Schottky clamped transistor



(e) Symbol for Schottky clamped transistor

Fig. 3.3.16

Review Questions

1. With neat circuit diagram explain the operation of two-input TTL NAND gates.
2. Draw circuit of TTL with totem-pole output and justify speed of operation is improved.
3. Prove that TTL gates have a typical fan-out of 10.
4. With the help of diagrams explain the current sinking and current sourcing actions for TTL gate output.
5. Explain the wired logic output of TTL with neat diagram.

6. Does totem-pole output support wired-logic connectors? Justify your answer.
7. Why totem-pole output stages cannot be connected together except open collector logic?
8. Define wired-AND connection
9. Give the advantages and disadvantages of totem-pole output stage arrangement.
10. Explain the advantages of open collector output.
11. Draw three input standard TTL NAND gate circuit and explain its operation.
12. Explain the following characteristics of TTL logic families :
 - i) Power dissipation
 - ii) Noise margin
 - iii) Propagation delay
 - iv) Fan out.
13. Comment on unconnected inputs in TTL.
14. Draw and explain the operation of Tri-state TTL inverter.
15. Draw and explain the transfer characteristics of TTL inverter.
16. Draw standard TTL inverter, discuss its operation and draw its transfer characteristics.
17. Discuss the advantages and disadvantages of TTL Logic Family.
18. Write a short note on TTL schottky family.
19. What is the advantage of schottky TTL family.

GTU - Winter-18, Marks 3

3.4 CMOS Logic

3.4.1 CMOS Inverter

Fig. 3.4.1 shows the basic CMOS inverter circuit. It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to +V_{DD} (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

1. When input is HIGH, the gate of Q₁ (P-channel) is at 0 V relative to the source of Q₁ i.e. V_{gs1} = 0 V. Thus, Q₁ is OFF. On the other hand, the gate of Q₂ (N-channel) is at +V_{DD} relative to its source i.e. V_{gs2} = +V_{DD}. Thus, Q₂ is ON. This will produce V_{OUT} ≈ 0 V, as shown in the Fig. 3.4.2 (a). (See Fig. 3.4.2 on next page).
2. When input is LOW, the gate of Q₁ (P-channel) is at a negative potential relative to its source while Q₂ has V_{gs} = 0 V. Thus, Q₁ is ON and Q₂ is OFF. This produces output voltage approximately +V_{DD}, as shown in the Fig. 3.4.2 (b).

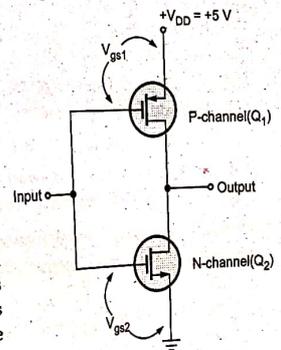


Fig. 3.4.1 CMOS inverter circuit

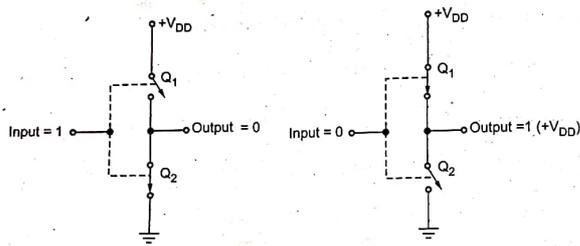


Fig. 3.4.2 Operation of CMOS inverter for both input conditions

Table 8.5.1 summarizes the operation of CMOS inverter circuit

A	Q ₁	Q ₂	Output
0	ON	OFF	1
1	OFF	ON	0

Table 3.4.1 Truth table of inverter

- The Fig. 3.4.3 shows, different symbols used for the p-channel and n-channel transistors to reflect their logical behaviour.
- The n-channel transistor (Q₂) is switched 'ON' when a HIGH voltage is applied at the input.
- The p-channel transistor (Q₁) has the opposite behaviour, it is switched ON when a LOW voltage is applied at the input. It is indicated by placing bubble in the symbol.

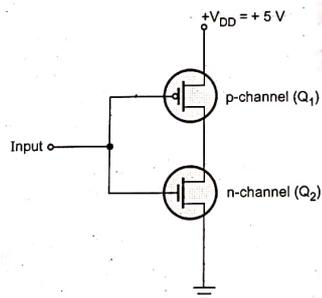


Fig. 3.4.3 The CMOS inverter

Transfer Characteristics of CMOS Inverter

- Fig. 3.4.4 shows transfer characteristics of CMOS inverter. (See Fig. 3.4.4 on next page).
- For CMOS family $V_{IH(min)} = 3.5\text{ V}$ and $V_{IL(max)} = 1.5\text{ V}$.
- For $V_{in} < V_{IL(max)}$ ($V_{in} \leq 1.5\text{ V}$), the output voltage is high.

- For $V_{IL(max)} \leq V_{in} \leq V_{IH(min)}$ the output voltage is in the transition phase.
- For $V_{in} \geq V_{IH(min)}$ ($V_{in} \geq 3.5\text{ V}$), the output voltage is low.

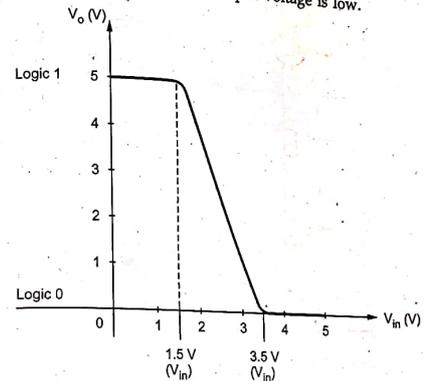


Fig. 3.4.4 Transfer characteristics of CMOS inverter

3.4.2 CMOS NAND Gate

- Fig. 3.4.5 shows CMOS 2-input NAND gate. It consists of two P-channel MOSFETs, Q₁ and Q₂, connected in parallel and two N-channel MOSFETs, Q₃ and Q₄ connected in series. (See Fig. 3.4.5 on next page)
- Fig. 3.4.5 (a) shows the equivalent switching circuit when both inputs are low. Here, the gates of both P-channel MOSFETs are negative with respect to their sources, since the sources are connected to +V_{DD}. Thus, Q₁ and Q₂ are both ON. Since the gate-to-source voltages of Q₃ and Q₄ (N-channel MOSFETs) are both 0 V, those MOSFETs are OFF. The output is therefore connected to +V_{DD} (HIGH) through Q₁ and Q₂ and is disconnected from ground, as shown in the Fig. 3.4.5 (b).
- Fig. 3.4.5 (c) shows the equivalent switching circuit when A = 0 and B = +V_{DD}. In this case, Q₁ is on because $V_{GS1} = -V_{DD}$ and Q₄ is ON because $V_{GS4} = +V_{DD}$. This MOSFETs Q₂ and Q₃ are off because their gate-to-source voltages are 0 V. Since Q₁ is ON and Q₃ is OFF, the output is connected to +V_{DD} and it is disconnected from ground. When A = +V_{DD} and B = 0 V, the situation is similar (not shown); the output is connected to +V_{DD} through Q₂ and it is disconnected from ground because Q₄ is OFF. Finally, when both inputs are high (A = B = +V_{DD}), MOSFETs Q₁ and Q₂ are both OFF and Q₃ and Q₄ are both ON. Thus, the output is connected to the ground through Q₃ and Q₄ and it is disconnected from +V_{DD}.

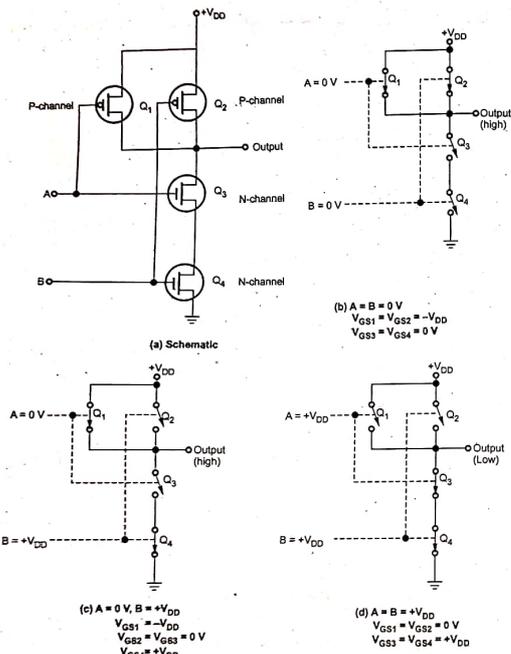


Fig. 3.4.5 CMOS NAND gate

P-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas N-channel MOSFET is ON when its gate voltage is positive with respect to its source.

- The Table 3.4.2 summarizes the operation of 2-input CMOS NAND gate.
- The Fig. 3.4.6 shows the circuit diagram, function table and logic symbol of CMOS 3-input NAND gate.

A	B	Q ₁	Q ₂	Q ₃	Q ₄	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 3.4.2 Truth table of NAND gate

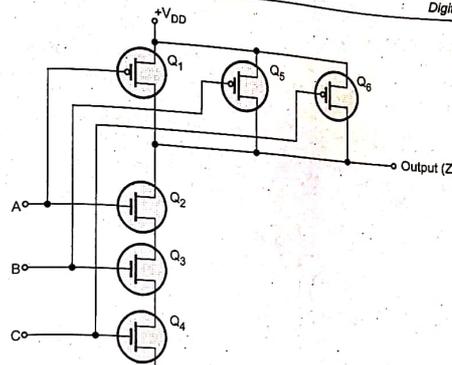


Fig. 3.4.6 (a) Circuit diagram

A	B	C	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Z
0	0	0	ON	OFF	OFF	OFF	ON	ON	1
0	0	1	ON	OFF	OFF	ON	ON	OFF	1
0	1	0	ON	OFF	ON	OFF	OFF	ON	1
0	1	1	ON	OFF	ON	ON	OFF	OFF	1
1	0	0	OFF	ON	OFF	OFF	ON	ON	1
1	0	1	OFF	ON	OFF	ON	ON	OFF	1
1	1	0	OFF	ON	ON	OFF	OFF	ON	1
1	1	1	OFF	ON	ON	ON	OFF	OFF	0

Fig. 3.4.6 (b) Function table

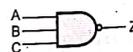
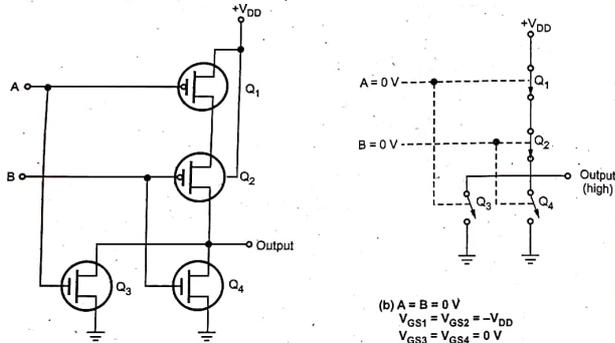


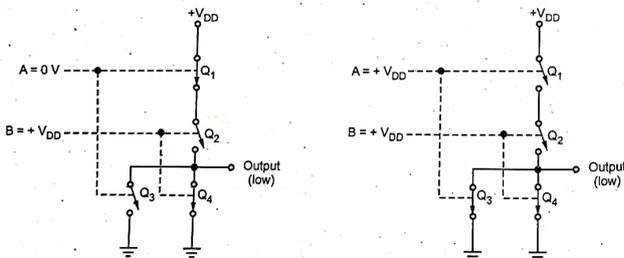
Fig. 3.4.6 (c) Logic symbol

3.4.3 CMOS NOR Gate

- Fig. 3.4.7 shows 2-input CMOS NOR gate. Here, P-channel MOSFETs Q_1 and Q_2 are connected in series and N-channel MOSFETs Q_3 and Q_4 are connected in parallel.
- Like NAND circuit, this circuit can be analyzed by realizing that a LOW at any input turns ON its corresponding P-channel MOSFET and turns OFF its corresponding N-channel MOSFET, and vice versa for a HIGH input. This is illustrated in Fig. 3.4.7.



(a) Schematic



(c) $A = 0\text{ V}, B = +V_{DD}$
 $V_{GS1} = -V_{DD}$
 $V_{GS2} = V_{GS3} = 0\text{ V}$
 $V_{GS4} = +V_{DD}$

(d) $A = B = +V_{DD}$
 $V_{GS1} = V_{GS2} = 0\text{ V}$
 $V_{GS3} = V_{GS4} = +V_{DD}$

Fig. 3.4.7 CMOS NOR gate

- The Table 3.4.3 summarizes the operation of 2-input NOR gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 3.4.3 Truth table for NOR gate

3.4.4 CMOS Characteristics

Operating Speed :

1. Slower than TTL series.
2. Approximately 25 to 100 ns depending on the subfamily of CMOS.
3. It also depends on the power supply voltage.

Voltage Levels and Noise Margins :

1. The voltage levels for CMOS varies according to their subfamilies. These are listed in Table 3.4.4.
2. Noise margins in table are calculated as follows.

$$V_{NH} = V_{OH(\min)} - V_{IH(\min)}$$

$$V_{NL} = V_{IL(\max)} - V_{OL(\max)}$$

Fan-out :

1. The CMOS inputs have an extremely large resistance ($10^{12} \Omega$) that draws essentially no current from the signal source. Each CMOS input, however, typically presents a 5 pF load to ground as shown in the Fig. 3.4.8. This input capacitance limits the number of CMOS inputs that one CMOS output can drive.
2. The CMOS output has to charge and discharge the parallel combination of all the input capacitances. This charging and discharging time increases as we increase

Parameter	CMOS series				
	4000 B	74 HC	74 HCT	74 AC	74 ACT
$V_{IH(\min)}$	3.5	3.5	2.0	3.5	2.0
$V_{IL(\max)}$	1.5	1.0	0.8	1.5	0.8
$V_{OH(\min)}$	4.95	4.9	4.9	4.9	4.9
$V_{OL(\max)}$	0.05	0.1	0.1	0.1	0.1
V_{NH}	1.45	1.4	2.9	1.4	2.9
V_{NL}	1.45	0.9	0.7	1.4	0.7

Table 3.4.4

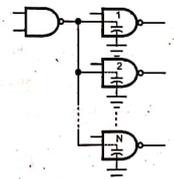


Fig. 3.4.8 One CMOS output driving several CMOS inputs

number of loads. Typically, each CMOS load increases the driving circuit's propagation delay by 3 ns. Thus, fan-out for CMOS depends on the permissible maximum propagation delay.

- Typically, CMOS outputs are limited to a fan-out of 50 for low-frequency operation (≤ 1 MHz). Of course, for high-frequency operation the fan-out would have to be less.

Power Dissipation (P_D) :

- The power dissipation of a CMOS IC is very low as long as it is in a d.c. condition.
- Unfortunately, power dissipation of CMOS IC increases in proportion to the frequency at which the circuits are switching states.
- For example, a CMOS NAND gate that has $P_D = 10$ nW under d.c. conditions will have $P_D = 0.1$ mW at a frequency of 100 kHz and 1 mW at 1 MHz.
- When CMOS output switches from LOW to HIGH, a transient charging current has to be supplied to the load capacitance. Therefore, as the switching frequency increases, the average current drawn from V_{DD} also increases, resulting increase in power dissipation.

Propagation Delay :

- The propagation delay in CMOS is the sum of delay due to internal capacitance and due to load capacitance.
- The delay due to internal capacitance is called the intrinsic propagation delay.
- The delay due to load capacitance can be approximated as follows.

$$t_p(C_L) \approx 0.5 R_o C_L \text{ seconds}$$

where $t_p(C_L)$ is either t_{pLH} or t_{pHL} .

R_o is the output resistance of the gate and C_L is the total load capacitance.

The R_o depends on the supply voltage and it can be approximated as

$$R_o \approx \frac{V_{CC}}{I_{os}}$$

where I_{os} is the short circuit output current.

Unconnected Inputs :

- CMOS inputs should never be left disconnected. All CMOS inputs have to be tied either to a fixed voltage level (0 V or V_{DD}) or to another input. This rule applies even to the inputs of extra unconnected logic gates on a chip.

- An unconnected CMOS input is susceptible to noise and static charges that could easily bias both the P and N-channel MOSFETs in the conductive state, resulting in increased power dissipation and possible overheating.

Static-charge Susceptibility (CMOS Hazards) :

- Every CMOS device is vulnerable to the building up of electrical charge on its insulated gate. Recall that the relationship between charge Q and voltage V on a capacitor having capacitance C is

$$V = \frac{Q}{C}$$

- Since the input capacitance at the gate is usually quite small (a few picofarads), a relatively small amount of charge can create a large voltage which may be greater than the breakdown voltage of a MOS gate (typically 100 V).
- The primary source of charge is "static" electricity, usually produced by handling and the motion of various kinds of plastics and textiles.
- The CMOS devices are protected against this static charge by on-chip diode-resistor network, as shown in the Fig. 3.4.9. These diodes are designed to turn ON and limit the size of the input voltage to well below any damaging value.

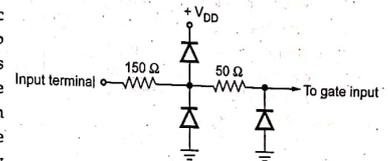


Fig. 3.4.9 Typical network used to protect CMOS from static charges

Latch-up :

- CMOS integrated circuits contain parasitic PNP and NPN transistors : Transistors that exist because of the proximity of P and N materials embedded in the substrate. Their existence is not intentional but is unavoidable. Because of conducting paths between a pair of such transistors, a device can be triggered into a heavy conduction mode, known as latch-up.
- This heavy conduction mode, results large current flow which can destroy IC.
- Most CMOS circuits contain protective measures to prevent latch-up, but it can still occur if the manufacturers specified maximum ratings are exceeded.

3.4.5 Wired Logic

- Fig. 3.4.10 shows two CMOS inverters with their outputs connected together.

- This circuit does not work properly when B input is logic 0 and A input is logic 1. In this situation, Q_3 and Q_2 are ON and large current flows through Q_3 and Q_2 damaging these transistors. Therefore, wired-logic must not be used for CMOS logic circuits.

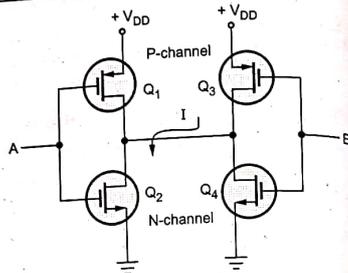


Fig. 3.4.10

3.4.6 Open Drain Outputs

- CMOS gates are available with open drain outputs, as shown in Fig. 3.4.11.
- In open drain outputs, PMOS transistor is replaced by a diode D_1 which provides protection from electrostatic discharge.
- Open drain gates can be used with external pull-up resistors to perform wired-AND operation, as discussed in TTL logic.

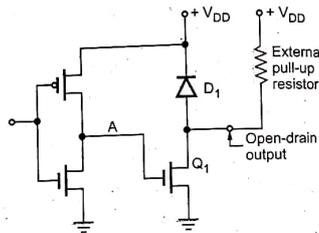


Fig. 3.4.11

3.4.7 Advantages and Disadvantages of CMOS Family

Advantages

1. Consumes less power.
2. Can be operated at high voltages, resulting in improved noise immunity.
3. Fan-out is more.
4. Better noise margin.

Disadvantages

1. Susceptible to static charge.
2. Switching speed low.
3. Greater propagation delay.

Review Questions

1. What are salient features of CMOS logic family ?
 2. Draw the structure of CMOS inverter gate. Explain its working.
 3. Draw and explain the transfer characteristics of CMOS inverter.
 4. Explain with neat diagram two input CMOS NAND gate.
 5. Explain with neat diagram two input CMOS NOR gate.
 6. Define the following parameters and give typical values of these parameters w.r.t. CMOS logic family : i) Speed of operation ii) Power dissipation iii) Sourcing current iv) Fan out v) Sinking current.
 7. Explain, why wired-logic is not used for CMOS logic circuits.
 8. What do you mean by open drain output ? Where is it used ?
 9. List differences between open drain and wired logic CMOS.
 10. State merits and demerits of CMOS logic family.
 11. Explain with a neat diagram interfacing of TTL gate driving CMOS gates and vice-versa.
 12. Which parameters are significant while interfacing TTL and CMOS ? Draw and explain TTL driving CMOS gate.
 13. Compare TTL and CMOS logic families w.r.t. : i) Power dissipation per gate ii) Propagation delay iii) Figure of merit iv) Fan-out.
 14. List differences between CMOS and TTL.
 15. Explain OR gate using CMOS logic.
- [Hints : Connect CMOS inverter at the output of CMOS NOR gate]
16. Write a note on CMOS logic family.

3.5 Interfacing of CMOS to TTL and TTL to CMOS

- Interfacing means connecting the output(s) of one circuit or system to the input(s) of another circuit or system that may have different electrical characteristics. When two circuits have different electrical characteristics direct connection cannot be made. In such cases driver and load circuits are connected through interface circuit. Its function is to take the driver output signal and condition it so that it is compatible with requirements of the load.
- One must consider following important points while interfacing two circuits or systems.
 1. The driver output must satisfy the voltage and current requirements of the load circuit.
 2. The driver and load circuit may require different power supplies. In such cases the output of both circuit must swing between its specified voltage ranges.

3.5.1 TTL Driving CMOS

- Here, TTL is a driver circuit and CMOS is a load circuit. The two circuits are from different families with different electrical characteristics. Therefore, we must check that the driving device can meet the current and voltage requirements of the load device.

	CMOS			TTL	
	4000B	74HC/HCT	74	74LS	74AS
$I_{IH} (max)$	1 μA	1 μA	40 μA	20 μA	200 μA
$I_{IL} (max)$	1 μA	1 μA	1.6 mA	0.4 mA	2 mA
$I_{OH} (max)$	0.4 mA	4 mA	0.4 mA	0.4 mA	2 mA
$I_{OL} (max)$	0.4 mA	4 mA	16 mA	8 mA	20 mA

Table 3.5.1 Input/output currents for standard devices with supply voltage of 5 V

- Table 3.5.1 indicates that the input current values for CMOS are extremely low compared with the output current capabilities of any TTL series. Thus, TTL has no problem meeting the CMOS input current requirements.
- When we compare the TTL output voltages with the CMOS input voltage requirements we find that:

$V_{OH} (min)$ for TTL $\ll V_{IH} (min)$ for CMOS for these situations TTL output must be raised to an acceptable level for CMOS. This can be done by connecting pull-up resistor at the output of TTL, as shown in the Fig. 3.5.1. The pull-up resistor causes the TTL output to rise to approximately 5 V in the HIGH state, thereby providing an adequate CMOS input voltage level.

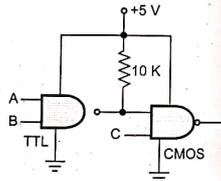


Fig. 3.5.1 TTL driving CMOS using external pull-up resistor

TTL Driving HIGH Voltage CMOS : When output CMOS circuit is operating with V_{DD} greater than 5 V, the situation becomes more difficult. The outputs of many TTL devices cannot be operated at more than 5 V. In such cases some alternative arrangements are made. Two of them are discussed below :

- When the TTL output cannot be pulled up to V_{DD} , one can use open collector buffer as an

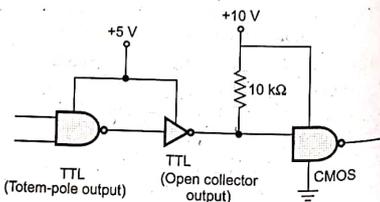


Fig. 3.5.2 Open collector buffer used as interface circuit

interface between totem-pole TTL output and CMOS operating at $V_{DD} > 5 V$, as shown in the Fig. 3.5.2.

- The second alternative is to use level translator circuit, such as the 40104. This is a CMOS chip that is designed to take a low-voltage input (e.g. from TTL) and translate it to high voltage output for CMOS. Fig. 3.5.3 shows the circuit arrangement.

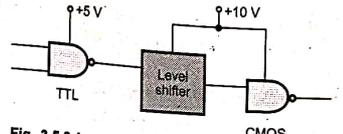


Fig. 3.5.3 Level shifter used as interface circuit

3.5.2 CMOS Driving TTL

- Before we consider the problem of interfacing CMOS outputs to TTL inputs, it will be helpful to review the CMOS output and TTL input characteristics for the two logic states.

For CMOS (4000B)	For TTL
$V_{OH} (min) : 4.95 V$	$V_{IH} (min) : 2.0 V$
$V_{OL} (max) : 0.05 V$	$V_{IL} (max) : 0.8 V$
$I_{OH} (max) : 0.4 mA$	$I_{IH} (max) : 40 \mu A$
$I_{OL} (max) : 0.4 mA$	$I_{IL} (max) : 1.6 mA$

Table 3.5.2

CMOS Driving TTL in the HIGH state :

- Above voltage parameters show that CMOS outputs can easily supply enough voltage (V_{OH}) to satisfy the TTL input requirement in the HIGH state (V_{IH}).
- The parameters also show that CMOS outputs can supply more than enough current (I_{OH}) to meet the TTL input current requirements (I_{IH}). Thus no special consideration is required for CMOS driving TTL in the HIGH state.

CMOS Driving TTL in LOW state :

- The parameters in the Table 3.5.2 show that CMOS output voltage (V_{OL}) satisfies TTL input requirement in the LOW state (V_{IL}). However, the current requirements in the LOW state are not satisfied.
- The TTL input has a relatively high input current in the LOW state (1.6 mA) and CMOS output current at LOW state (I_{OL}) is not sufficient to drive even one input of the TTL. In such situations some type of

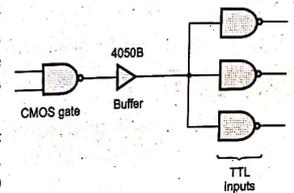


Fig. 3.5.4 CMOS driving TTL in LOW state using buffer

interface circuit is needed between the CMOS and TTL devices. Fig. 3.5.4 shows the possible interface circuit.

3. In Fig. 3.5.4 the CMOS 4050B, non-inverting buffer is used as an interfacing circuit. It has an output current rating of $I_{OL(max)} = 3\text{ mA}$ which satisfies the TTL input current requirement.

HIGH Voltage CMOS Driving TTL :

1. Some IC manufacturers have provided several 74LS TTL devices that can withstand input voltages as high as 15 V. These devices can be driven directly from CMOS outputs operating at $V_{DD} = 15\text{ V}$.
2. Most TTL inputs cannot handle more than 7 V and so interface is necessary if they are to be driven from high-voltage CMOS. In such situations voltage level translators are used. They convert the high-voltage input to a 5 V output that can be connected to TTL.

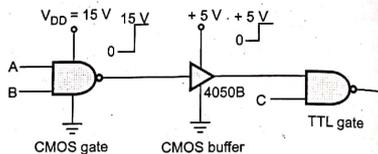


Fig. 3.5.5 Level translation using CMOS buffer

3. Fig. 3.5.5 shows how the 4050B can be used to perform this level translation between 15 V and 5 V.

Example 3.5.1 Why is a buffer required between some CMOS outputs and TTL inputs ?

Solution : The current requirement of CMOS output at LOW state are not satisfied by TTL input. The TTL input has a relatively high input current in the LOW state (1.6 mA) and CMOS output current at LOW state (I_{OL}) is not sufficient to drive even one input of the TTL. Hence buffer is used for interfacing.

Example 3.5.2 Which CMOS series can have its inputs driven directly from a TTL output ? Justify your answer.

Solution : VHC and VHCT CMOS families are TTL compatible.

Review Question

1. Explain interfacing of TTL and CMOS logic families.

3.6 Comparison between TTL and CMOS

GTU : Winter-15

Sr. No.	Parameter	CMOS	TTL
1.	Device used	n-channel and p-channel MOSFET	Bipolar junction transistor
2.	$V_{IH(min)}$	3.5 V	2 V
3.	$V_{IL(max)}$	1.5 V	0.8 V
4.	$V_{OH(min)}$	4.95 V	2.7 V
5.	$V_{OL(max)}$	0.005 V	0.4 V
6.	High level noise margin	$V_{NH} = 1.45\text{ V}$	0.4 V
7.	Low level noise margin	$V_{NL} = 1.45\text{ V}$	0.4 V
8.	Noise immunity	Better than TTL	Less than CMOS
9.	Propagation delay	70 ns	10 ns
10.	Switching speed	Less than TTL	Faster than CMOS
11.	Power dissipation per gate	0.1 mW	10 mW
12.	Speed power product	0.7 pJ	100 pJ
13.	Fan-out	50	10
14.	Power supply voltage	3 - 15 V	Fixed 5 V
15.	Power dissipation	Increase with frequency	Increase with frequency
16.	Application	Portable instrument where battery supply is used.	Laboratory instruments.

Table 3.6.1 Comparison between TTL and CMOS families

Review Question

1. Compare TTL and CMOS logic families.

GTU : Winter-15, Summer-18, Marks 7

Oral Questions and Answers

Q.1 What are the types of TTL logic ?

Ans. : 1. Open collector output 2. Totem-pole output 3. Tri-state output.

Q.2 List the different versions of TTL.

Ans. : 1. TTL (Std.TTL) 2. LITL (Low Power TTL) 3. HTTL (High Speed TTL) 4. STTL (Schottky TTL) 5. LSTTL (Low power Schottky TTL).

Q.3 Distinguish between 7400 series and 5400 series.

Ans. :

Supply voltage	For 74 series - (4.75 to 5.25) V For 54 series - (4.5 to 5.5) V
Temperature range	For 74 series - (0 °C to 70 °C) For 54 series - (-55 °C to 125 °C)

Q.4 What is meant by tristate capability ?

Ans. : Tristate capability is the capability of output level to take three stages (output levels) as HIGH, LOW and High-impedance. For example, tristate TTL.

Q.5 Explain open collector output.

Ans. : When the collector terminal of a transistor is kept open without any pull up transistor the arrangement is called open collector output. The output is taken directly from the open collector terminal of a transistor at the output. But, a gate with open collector will not work properly until an external resistor is connected.

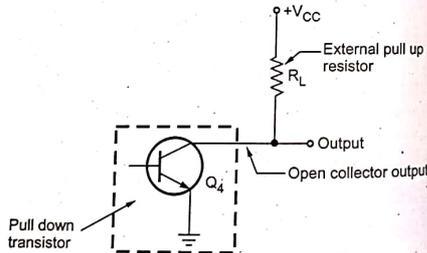


Fig. 3.1 Open collector output with pull-up resistor

When Q_4 is ON, output is low and when Q_4 is OFF, output is tied to V_{CC} through an external pull up resistor.

Q.6 Differentiate : Source and sink current.

Ans. :

Sr. No.	Current sinking	Current sourcing
1.	When the output of the logic circuit is low, the current flows from load into the pull down transistor of the totem-pole. This is known as current sinking.	When the output of the logic circuit is high, the current flows from pull up transistor of the totem-pole to the load. This is known as current sourcing.
2.	During current sinking base-emitter diode of the load is forward biased. Hence sinking current is in milliamperes.	During current sourcing only leakage current flows hence sourcing current is in microamperes.

Q.7 How Schottky transistors are formed and state its use ?

Ans. : A Schottky diode is formed by the combination of metal and semiconductor. The presence of schottky diode between the base and the collector prevents the transistor from going into saturation. The resulting transistor is called Schottky transistor.

The use of Schottky transistor in TTL decreases the propagation delay without a sacrifice of power dissipation.

Q.8 Why totem pole outputs cannot be connected together ?

Ans. : Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

Q.9 What happens to output when a tristate circuit is selected for high impedance.

Ans. : Output is disconnected from rest of the circuits by internal circuitry.

Q.10 State advantages and disadvantages of totem-pole output.

Ans. : Advantages of totem-pole output are :

1. External pull up resistor is not required
2. Operating speed is high.

Disadvantages of totem-pole output :

1. Output of two gates cannot be tied together.

Q.11 Explain the wired-AND connection.

Ans. : When the open collector outputs of two or more gates can be connected together, the connection is called a wired-AND. In wired-AND connection, the output is high only when all switches are open i.e. when output of each stage is high.

Hence, the output is equivalent to the logical AND operation of the logic function performed by the gates.

Q.12 Give any two applications of open collector logic.

Ans. : 1. It is used when we require to connect outputs of two or more gates.

2. It is used when sourcing current requirements is larger than the standard totem-pole output.

Q.13 State advantages and disadvantages of TTL.

Ans. : Refer section 3.3.8.

Q.14 What is the effect of increasing the supply voltage on the propagation delay of the CMOS gates ?

Ans. : Increasing the supply voltage reduce the propagation delay of the CMOS gates.

Q.15 Which is the fastest logic family ?

Ans. : ECL.

Q.16 Which TTL logic gate is used for wired ANDing ?

Ans. : The output of open collector TTL logic gates can be tied together using wired AND technique.



4

Combinational Digital Circuits

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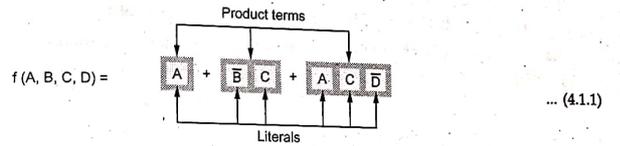
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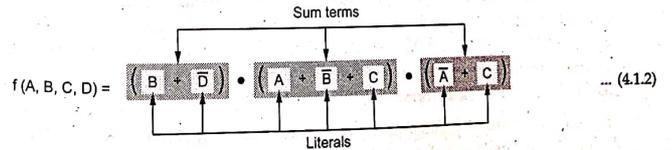
4.1 Standard Representation for Logic Functions

GTU : May-12, 13, 14, Dec.-13, Winter-17

- Boolean expressions are constructed by connecting the Boolean constants and variables with the Boolean operations. These Boolean expressions are also known as **Boolean formulae**.
- We use Boolean expressions to describe switching function or **Boolean functions**. For example, if the Boolean expression $(A + \bar{B}) C$ is used to describe the function f , then Boolean function is written as $f(A, B, C) = (A + \bar{B}) C$ or $f = (A + \bar{B}) C$
- Based on the structure of Boolean expression, it can be categorized in different formulae. One such categorization are the normal formulae.
- Consider the four-variable Boolean function.



- In this Boolean function the variables are appeared either in a complemented or an uncomplemented form.
- Each occurrence of a variable in either a complemented or an uncomplemented form is called a **literal**. Thus, the above Boolean function 4.1.1 consists of six literals. They appear in the product terms.
- A **product term** is defined as either a literal or a product (also called conjunction) of literals. Function 4.1.1 contains three product terms, namely, A , $\bar{B} C$ and $A C \bar{D}$.
- Consider another four variable Boolean function.

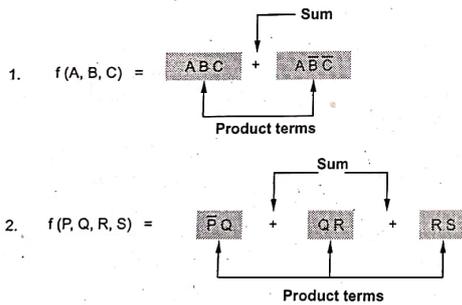


- The above Boolean function consists of seven literals. Here, they appear in the sum terms.

- A **sum term** is defined as either a literal or a sum (also called disjunction) of literals. Function 4.1.2 contains three sum terms, namely, $(B + \bar{D})$, $(A + \bar{B} + C)$ and $(\bar{A} + C)$. These literals and terms are arranged in one of the two forms :
 - Sum Of product form (SOP) and
 - Product Of Sum form (POS).

4.1.1 Sum of Product Form

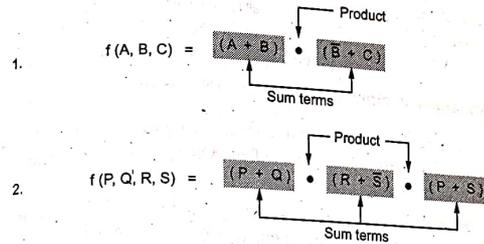
- The words sum and product are derived from the symbolic representations of the OR and AND functions by + and · (addition and multiplication), respectively. But we realize that these are not arithmetic operators in the usual sense. A product term is any group of literals that are ANDed together.
- For example, ABC , XY and so on. A sum term is any group of literals that are ORed together such as $A + B + C$, $X + Y$ and so on. A Sum Of Products (SOP) is a group of product terms ORed together. Some examples of this form are :
- Each of these sum of products expressions consist of two or more product terms (AND) that are ORed together.



- Each product term consists of one or more literals appearing in either complemented or uncomplemented form. For example, in the sum of products expression $ABC + A\bar{B}\bar{C}$, the first product term contains literals A, B and C in their uncomplemented form. The second product term contains B and C in their complemented (inverted) form.
- The sum of product form is also known as **disjunctive normal form** or **disjunctive normal formula**.

4.1.2 Product of Sum Form

- A product of sums is any groups of sum terms ANDed together. Some examples of this form are :



- Each of these product of sums expressions consist of two or more sum terms (OR) that are ANDed together.
- Each sum term consists of one or more literals appearing in either complemented or uncomplemented form.
- The product of sum form is also known as **conjunctive normal form** or **conjunctive normal formula**.

4.1.3 Standard SOP and Standard POS Forms

- We can realize that in the SOP form, all the individual terms do not involve all literals.
- For example, in expression $AB + A\bar{B}\bar{C}$ the first product term do not contain literal C.
- If each term in SOP form contains all the literals then the SOP form is known as **standard or canonical SOP form**.
- Each individual term in the standard SOP form is called **minterm**.
- One standard sum of products expression is as shown in Fig. 4.1.1.
- If each term in POS form contains all the literals then the POS form is known as **standard or canonical POS form**.

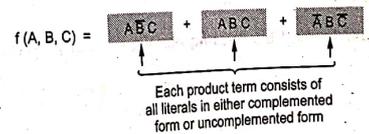


Fig. 4.1.1 Standard SOP form

- Each individual term in the standard POS form is called **maxterm**.
- One standard product of sums expression is as shown in Fig. 4.1.2.

$$f(A, B, C) = (A + B + C) \cdot (A + \bar{B} + C)$$

Each sum term consists of all literals in either complemented form or uncomplemented form

Fig. 4.1.2 Standard POS form

4.1.4 Converting Expressions in Standard SOP or POS Form

- Sum of product form can be converted to standard sum of products by ANDing the terms in the expression with terms formed by ORing the literal and its complement which are not present in that term.
- For example for a three literal expression with literals A, B and C, if there is a term AB, where C is missing, then we form term $(C + \bar{C})$ and AND it with AB. Therefore, we get $AB(C + \bar{C}) = ABC + AB\bar{C}$.

4.1.4.1 Steps to Convert SOP to Standard SOP Form

- Step 1 :** Find the missing literal in each product term if any.
- Step 2 :** AND each product term having missing literal/s with term/s form by ORing the literal and its complement.
- Step 3 :** Expand the terms by applying distributive law and reorder the literals in the product terms.
- Step 4 :** Reduce the expression by omitting repeated product terms if any. Because $A + A = A$.

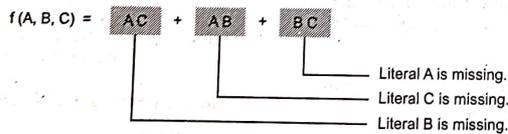
Illustrative Examples

Example 4.1.1 Convert the given expression in standard SOP form.

$$f(A, B, C) = AC + AB + BC$$

Solution :

Step 1 : Find the missing literal/s in each product term.



Step 2 : AND product term with (missing literal + its complement).

$$f(A, B, C) = AC \cdot (B + \bar{B}) + AB \cdot (C + \bar{C}) + BC \cdot (A + \bar{A})$$

Original product terms

Missing literals and their complements

Step 3 : Expand the terms and reorder literals.

Expand : $f(A, B, C) = ACB + AC\bar{B} + ABC + AB\bar{C} + BCA + BC\bar{A}$
 Reorder : $f(A, B, C) = ABC + A\bar{B}C + ABC + AB\bar{C} + ABC + \bar{A}BC$

Note After having sufficient practice student should expand product term and reorder literals in it in a single step.

Step 4 : Omit repeated product terms.

$$f(A, B, C) = ABC + A\bar{B}C + \cancel{ABC} + AB\bar{C} + \cancel{ABC} + \bar{A}BC$$

$$\therefore f(A, B, C) = ABC + A\bar{B}C + AB\bar{C} + \bar{A}BC$$

Example 4.1.2 Convert the given expression in standard SOP form. $f(A, B, C) = A + ABC$

Solution :

Step 1 : Find the missing literal/s in each product term.

$$f(A, B, C) = A + ABC$$

Literals B and C are missing

Step 2 : AND product term with (missing literal + its complement).

$$f(A, B, C) = A \cdot (B + \bar{B}) \cdot (C + \bar{C}) + ABC$$

Original terms

Missing literals and their complements

Step 3 : Expand the terms and reorder literals.

$$f(A, B, C) = ABC + A\bar{B}C + A\bar{B}\bar{C} + AB\bar{C} + ABC$$

Step 4 : Omit repeated product term

$$f(A, B, C) = ABC + A\bar{B}C + A\bar{B}\bar{C} + AB\bar{C} + \cancel{ABC}$$

Repeated product term

$$\therefore f(A, B, C) = ABC + A\bar{B}C + A\bar{B}\bar{C} + AB\bar{C}$$

Examples for Practice

Example 4.1.3 : Express the following function in standard SOP form

$$F_1 = AB + \overline{C}D + ABC$$

[Ans. : $\overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}D + A\overline{B}\overline{C}D + A\overline{B}C\overline{D} + A\overline{B}C\overline{D} + AB\overline{C}\overline{D} + AB\overline{C}D + ABC\overline{D} + ABCD$]

Example 4.1.4 : Determine the canonical SOP form of $f(x, y, z) = (x + y + \overline{z})(y + x\overline{z})$

[Ans. : $xyz + xy\overline{z} + \overline{x}y\overline{z} + \overline{x}y\overline{z}$]

4.1.4.2 Steps to Convert POS to Standard POS Form

- Step 1 :** Find the missing literals in each sum term if any.
- Step 2 :** OR each sum term having missing literal/s with term/s form by ANDing the literal and its complement.
- Step 3 :** Expand the terms by applying distributive law and reorder the literals in the sum terms.
- Step 4 :** Reduce the expression by omitting repeated sum terms if any. Because $A \cdot A = A$.

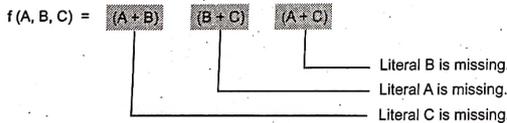
Illustrative Examples

Example 4.1.5 Convert the given expression in standard POS form.

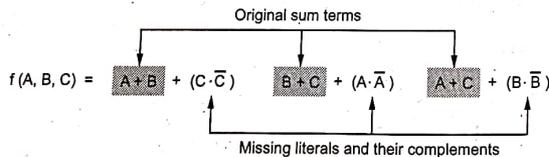
$$f(A, B, C) = (A + B)(B + C)(A + C)$$

Solution :

Step 1 : Find the missing literal/s in each sum term.



Step 2 : OR sum term with (missing literal • its complement).



Step 3 : Expand the terms and reorder literals.

Expand :

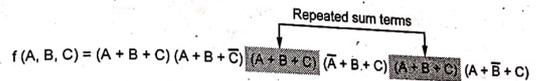
Since $A + BC = (A + B)(A + C)$ we have,

$$f(A, B, C) = (A + B + C)(A + B + \overline{C})(B + C + A)(B + C + \overline{A})(A + C + B)(A + C + \overline{B})$$

Reorder :

$$f(A, B, C) = (A + B + C)(A + B + \overline{C})(A + B + C)(\overline{A} + \overline{B} + C)(A + B + C)(A + \overline{B} + C)$$

Step 4 : Omit repeated sum terms.



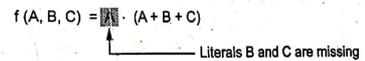
$$\therefore f(A, B, C) = (A + B + C)(A + B + \overline{C})(\overline{A} + \overline{B} + C)(A + \overline{B} + C)$$

Example 4.1.6 Convert the given expression in standard POS form.

$$Y = A \cdot (A + B + C)$$

Solution :

Step 1 : Find the missing literal/s in each sum term.



Step 2 : OR sum term with (missing literal • its complement).

$$f(A, B, C) = (A + B + \overline{B} + C + \overline{C})(A + B + C)$$

Step 3 : Expand the terms and reorder literals.

Since $A + BC = (A + B)(A + C)$ we have,

$$f(A, B, C) = (A + B + \overline{B} + C)(A + B + \overline{C})(A + B + C) = (A + B + C)(A + \overline{B} + C)(A + B + \overline{C})(A + \overline{B} + C)(A + B + C)$$

Step 4: Omit repeated sum terms.

$$f(A, B, C) = (A+B+C)(A+\bar{B}+C)(A+B+\bar{C})(A+\bar{B}+\bar{C}) \quad \text{Repeated sum term } (A+B+C)$$

$$f(A, B, C) = (A+B+C)(A+\bar{B}+C)(A+B+\bar{C})(A+\bar{B}+\bar{C})$$

Example for Practice

Example 4.1.7: Convert the given expression in standard POS form
 $f(P, Q, R) = (P+Q)(P+R)$

[Ans. : $(P + \bar{Q} + R)(P + \bar{Q} + \bar{R})(P + Q + R)$]

4.1.5 M Notations : Minterms and Maxterms

- Each individual term in standard SOP form is called minterm and each individual term in standard POS form is called maxterm.
- The concept of minterms and maxterms allows us to introduce a very convenient shorthand notations to express logical functions.
- Table 4.1.1 gives the minterms and maxterms for a three literal/variable logical function where the number of minterms as well as maxterms is $2^3 = 8$. In general, for an n-variable logical function there are 2^n minterms and an equal number of maxterms.
- As shown in Table 4.1.1 each minterm is represented by m_i and each maxterm is represented by M_i , where the subscript i is the decimal number equivalent of the natural binary number. With these shorthand notations logical function can be represented as follows:

Variables			Minterms	Maxterms
A	B	C	m_i	M_i
0	0	0	$\bar{A}\bar{B}\bar{C} = m_0$	$A+B+C = M_0$
0	0	1	$\bar{A}\bar{B}C = m_1$	$A+B+\bar{C} = M_1$
0	1	0	$\bar{A}B\bar{C} = m_2$	$A+\bar{B}+C = M_2$
0	1	1	$\bar{A}BC = m_3$	$A+\bar{B}+\bar{C} = M_3$
1	0	0	$A\bar{B}\bar{C} = m_4$	$\bar{A}+B+C = M_4$
1	0	1	$A\bar{B}C = m_5$	$\bar{A}+B+\bar{C} = M_5$
1	1	0	$AB\bar{C} = m_6$	$\bar{A}+\bar{B}+C = M_6$
1	1	1	$ABC = m_7$	$\bar{A}+\bar{B}+\bar{C} = M_7$

Table 4.1.1 Minterms and maxterms for three variables

1. $f(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$
 $= m_0 + m_1 + m_2 + m_4$
 $= \sum m(0, 1, 2, 4)$

2. $f(A, B, C) = (A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)$
 $= M_1 \cdot M_3 \cdot M_6$
 $= \Pi M(1, 3, 6)$

- where \sum denotes sum of product while Π denotes product of sum.
- Logical expression can be represented in the truth table form.
- It is possible to write logic expression in standard SOP or POS form corresponding to a given truth table.
- The logic expression corresponding to a given truth table can be written in a standard sum of products form by writing one product term for each input combination that produces an output of 1.
- These product terms are ORed together to create the standard sum of products. The product terms are expressed by writing complement of a variable when it appears as an input 0, and the variable itself when it appears as an input 1.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table 4.1.2

- Consider, for example, the truth Table 4.1.2.
- The product corresponding to input combination 010 is $\bar{A}BC$, the product corresponding to input combination 011 is $\bar{A}BC$ and product corresponding to input combination 110 is $AB\bar{C}$. Thus the standard sum of products form is
 $f(A, B, C) = \bar{A}BC + \bar{A}BC + AB\bar{C}$
 $= m_2 + m_3 + m_6$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Table 4.1.3

- The logic expression corresponding to a truth table can also be written in a standard product of sums form by writing one sum term for each output 0.
- The sum terms are expressed by writing complement of a variable when it appears as an input 1 and the variable itself when it appears as an input 0.
- Consider, for example, the truth Table 4.1.3.

- The sum corresponding to input combinations 010 is $A + \bar{B} + C$, and the sum corresponding to input 101 is $\bar{A} + B + \bar{C}$. Thus, the standard product of sum form is

$$f(A, B, C) = (A + \bar{B} + C)(\bar{A} + B + \bar{C})$$

$$= M_2 \cdot M_5$$

4.1.6 Complements of Standard Forms

- The POS and SOP functions derived from the same truth table are logically equivalent.
- In terms of minterms and maxterms we can then write

$$f(A, B, C) = m_0 + m_1 + m_3 + m_4 + m_6 + m_7 = M_2 + M_5$$

$$\therefore f(A, B, C) = \sum m(0, 1, 3, 4, 6, 7) = \prod M(2, 5)$$

From the above expressions we can easily notice that there is a complementary type of relationship between a function expressed in terms of maxterms. Using this complementary relationship we can find logical function in terms of maxterms if function in minterms is known or vice-versa. For example, for a four variables if

$$f(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 10, 12, 14)$$

$$\text{then } f(A, B, C, D) = \pi M(1, 3, 5, 7, 9, 11, 13, 15)$$

Example 4.1.8 Express $F = A + B'C$ as sum of minterms.

Solution :

$$A + \bar{B}C = A(B + \bar{B})(C + \bar{C}) + (A + \bar{A})\bar{B}C$$

$$= (AB + A\bar{B})(C + \bar{C}) + (A + \bar{A})\bar{B}C$$

$$= ABC + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C + \bar{A}\bar{B}C$$

$$= ABC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$$

$$\therefore F = \sum m(1, 4, 5, 6, 7)$$

Example 4.1.9 Express the Boolean function $F = XY + \bar{X}Z$ in product of maxterm.

Solution :

$$F = XY + \bar{X}Z$$

$$= XY(Z + \bar{Z}) + \bar{X}Z(Y + \bar{Y}) = XYZ + XY\bar{Z} + \bar{X}YZ + \bar{X}\bar{Y}Z$$

$$\therefore F = \sum m(7, 6, 3, 1)$$

$$= \prod M(0, 2, 4, 5)$$

$$= (X + Y + Z)(X + \bar{Y} + Z)(\bar{X} + Y + Z)(\bar{X} + Y + \bar{Z})$$

Example 4.1.10 Express the Boolean function as

- 1) POS form
- 2) SOP form

$$D = (A' + B)(B' + C)$$

Solution :

$$1. \text{ POS form : } D = (\bar{A} + B)(\bar{B} + C)$$

$$2. \text{ SOP form : } D = \bar{A}\bar{B} + \bar{A}C + B\bar{B} + BC$$

$$= \bar{A}\bar{B} + \bar{A}C + BC \quad \because B\bar{B} = 0$$

Example 4.1.11 Express the following function in product of maxterms.

$$F(x, y, z) = (xy + z)(y + xz)$$

GTU : May-12, Marks 3

$$\text{Solution : } F(x, y, z) = (xy + z)(y + xz)$$

$$= xy + xyz + yz + xz$$

$$= xy(1 + z) + yz + xz$$

$$= xy + yz + xz$$

$$= xy(z + \bar{z}) + yz(x + \bar{x}) + xz(y + \bar{y})$$

$$= xyz + xy\bar{z} + x\bar{y}z + \bar{x}yz + xyz + x\bar{y}\bar{z}$$

$$F(x, y, z) = xyz + xy\bar{z} + \bar{x}yz + x\bar{y}\bar{z}$$

$$\therefore F(x, y, z) = \sum m(3, 5, 6, 7) = \prod M(0, 1, 2, 4)$$

$$\therefore F(x, y, z) = (x + y + z)(x + y + \bar{z})(x + \bar{y} + z)(\bar{x} + y + z)$$

Example 4.1.12 Obtain the truth table of the function $F = xy + x\bar{y} + \bar{y}z$.

GTU - May-13, Marks 7

$$\text{Solution : } F = xy + x\bar{y} + \bar{y}z$$

$$= xy(z + \bar{z}) + x\bar{y}(z + \bar{z}) + \bar{y}z(x + \bar{x})$$

$$= xyz + xy\bar{z} + x\bar{y}z + x\bar{y}\bar{z} + x\bar{y}z + x\bar{y}\bar{z}$$

$$F = xyz + xy\bar{z} + x\bar{y}z + x\bar{y}\bar{z}$$

x	y	z	o/p
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0

1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Truth table of the function F

Example 4.1.13 Attempt following : 1) Convert into sum-of-minterms : $A+B+CA$

2) Convert into product-of-maxterms : $A(\bar{A}+B)\bar{C}$

GTU : May-14, Marks 7

Solution : 1) $A+B+CA$

$$\begin{aligned} &= \bar{A} \cdot (B+\bar{B}) \cdot (C+\bar{C}) + B \cdot (A+\bar{A}) \cdot (C+\bar{C}) + CA(B+\bar{B}) \\ &= \bar{A} \cdot (BC+B\bar{C}+\bar{B}C+\bar{B}\bar{C}) + B \cdot (AC+A\bar{C}+\bar{A}C+\bar{A}\bar{C}) + ABC+A\bar{B}C \\ &= \bar{A}BC+\bar{A}B\bar{C}+\bar{A}\bar{B}C+\bar{A}\bar{B}\bar{C}+ABC+AB\bar{C}+\bar{A}BC+A\bar{B}C+ABC+A\bar{B}C \\ &= \bar{A}BC+\bar{A}B\bar{C}+\bar{A}\bar{B}C+\bar{A}\bar{B}\bar{C}+ABC+AB\bar{C}+A\bar{B}C \end{aligned}$$

2) $A(\bar{A}+B)\bar{C}$

$$\begin{aligned} &= (A+B\bar{B}+C\bar{C})(\bar{A}+B+C\bar{C})(A\bar{A}+B\bar{B}+\bar{C}) \\ &= (A+B\bar{B}+C)(A+B\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+B+\bar{C}) \\ &\quad (A+B\bar{B}+\bar{C})(\bar{A}+B+\bar{C}) \\ &= (A+B\bar{B}+C)(A+B\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+B+\bar{C})(\bar{A}+B\bar{B}+\bar{C}) \\ &\quad \because A \cdot A = A \\ &= (A+B+C)(A+\bar{B}+C)(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+B+C) \\ &\quad (\bar{A}+B+\bar{C})(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+\bar{C}) \\ &= (A+B+C)(A+\bar{B}+C)(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+B+C) \\ &\quad (\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+\bar{C}) \end{aligned}$$

Example 4.1.14 Express the Boolean function $F = AB + \bar{A}C$ in a product of maxterm.

GTU : Winter-17, Marks 4

Solution : $F = AB(C+\bar{C}) + \bar{A}C(B+\bar{B})$

$$\begin{aligned} &= ABC + AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}C \\ &= \sum m(7, 6, 3, 1) \\ &= \sum m(1, 3, 6, 7) \\ &= \pi M(0, 2, 4, 5) \\ &= (A+B+C)(A+\bar{B}+C)(\bar{A}+B+C)(\bar{A}+B+\bar{C}) \end{aligned}$$

Review Questions

1. Define the following terms : 1) Minterm 2) Maxterm.
2. Define switching function.
3. Define literal, product term and sum term.
4. Explain sum of product form.
5. What do you mean by SOP and POS form also convert the expression $y = (A+BC)(B+\bar{A}C)$ into SOP and POS form.
6. Explain how to convert SOP or POS expressions in their standard forms.
7. What do you mean by minterms and maxterms ?

GTU : Dec.-13, Marks 2

4.2 Karnaugh-Maps (K-Map) Representation

GTU : May-14

- During the process of simplification of Boolean expression we have to predict each successive step.
- We can never be absolutely certain that an expression simplified by Boolean algebra alone is the simplest possible expression.
- On the other hand, the map method gives us a systematic approach for simplifying a Boolean expression.
- The map method, first proposed by Veitch and modified by Karnaugh, hence it is known as the Veitch diagram or the Karnaugh map.

4.2.1 One-Variable, Two-Variable, Three-Variable and Four-Variable Maps

- The basis of this method is a graphical chart known as Karnaugh map (K-map).
- It contains boxes called cells.
- Each of the cell represents one of the 2^n possible products that can be formed from n variables. Thus, a 2-variable map contains $2^2=4$ cells, a 3-variable map contains $2^3=8$ cells and so forth.
- Fig. 4.2.1 shows outlines of 1, 2, 3 and 4-variable maps.

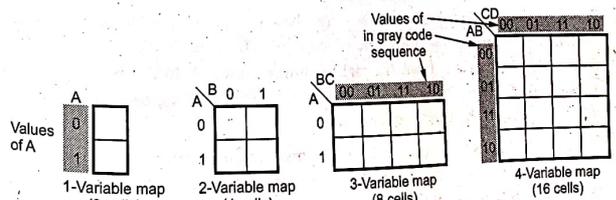


Fig. 4.2.1 Outlines of 1, 2, 3 and 4-variable Karnaugh maps

- Product terms are assigned to the cells of a Karnaugh map by labeling each row and each column of the map with a variable, with its complement, or with a combination of variables and complements.
- The product term corresponding to a given cell is then the product of all variable in the row and column where the cell is located.
- Fig. 4.2.2 shows the way to label the rows and columns of a 1, 2, 3 and 4-variable maps and the product terms corresponding to each cell.

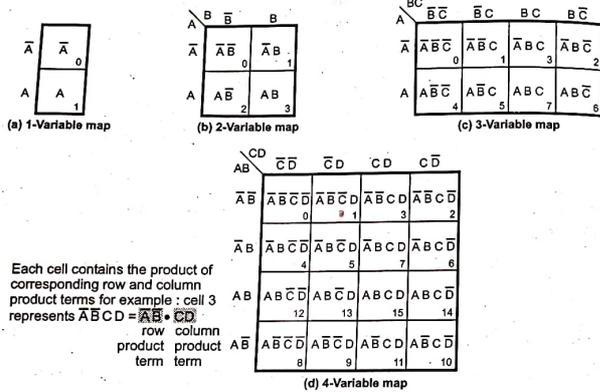


Fig. 4.2.2 1, 2, 3 and 4-variable maps with product terms

- When we move from one cell to the next along any row or from one cell to the next along any column, one and only one variable in the product term changes (to a complemented or to an uncomplemented form).
- For example, in Fig. 4.2.2 (b) the only change that occurs in moving along the bottom row from $\bar{A}\bar{B}$ to $A\bar{B}$ is the change from \bar{B} to B . Similarly, the only change that occurs in moving down the right column from $\bar{A}\bar{B}$ to $A\bar{B}$ is the change from \bar{A} to A . Irrespective of number of variables the labels along each row and column must conform to the single-change rule.
- The gray code has same properties (only one variable change when we proceed to next number or previous number) hence gray code is used to label the rows and columns of K-map as shown in Fig. 4.2.3.

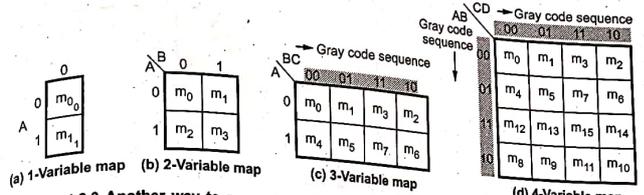


Fig. 4.2.3 Another way to represent 1, 2, 3 and 4-variable maps for SOP expressions

- The Fig. 4.2.3 shows how to label the rows and columns of a 1, 2, 3 and 4-variable maps using gray code and the product terms corresponding to each cell.
- Instead of writing actual product terms, corresponding shorthand minterm notations are written in the cell and row and columns are marked with gray code instead of variables.
- In case of POS expressions we assign maxterms (sum terms) to the cells of a Karnaugh map.
- The Fig. 4.2.4 shows the way to label the rows and columns of a 1, 2, 3 and 4-variable maps using gray code and the sum terms corresponding to each cell.

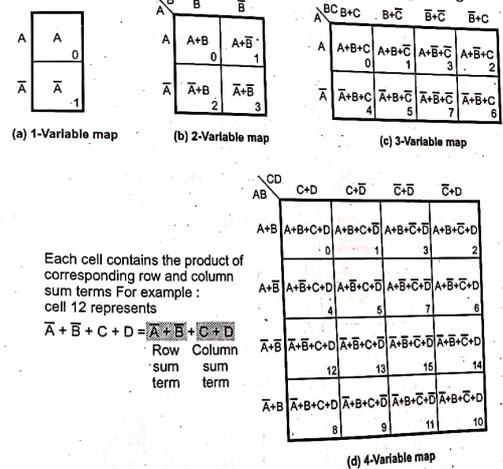


Fig. 4.2.4 1, 2, 3 and 4-variable maps with sum terms

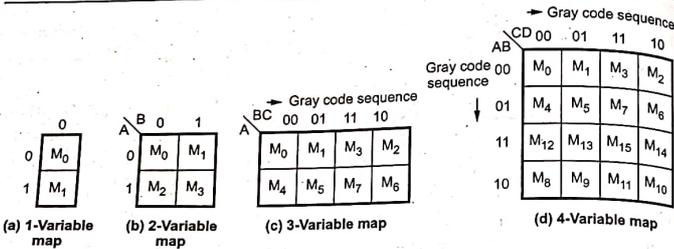


Fig. 4.2.5 Another way to represent 1, 2, 3 and 4-variable map for POS expressions

- Instead of writing actual sum terms, corresponding shorthand maxterm notations are written in the cell and row and columns are marked with gray code instead of variables.

4.2.2 Plotting a Karnaugh Map

- Logic function can be represented in various forms such as truth table, SOP Boolean expression and POS Boolean expression. In this section we will see the procedures to plot the given logic function in any form on the Karnaugh map.

4.2.2.1 Representation of Truth Table on Karnaugh Map

Cell : The smallest unit of a Karnaugh map, corresponding to one line of a truth table. The input variables are the cell's co-ordinates and the output variable is the cell's contents.

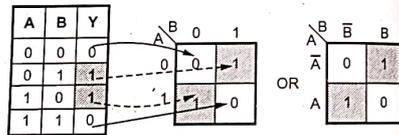


Fig. 4.2.6 (a) Representation of 2-variable truth table on K-map

- Fig. 4.2.6 shows K-maps plotted from truth tables with 2, 3 and 4-variables.

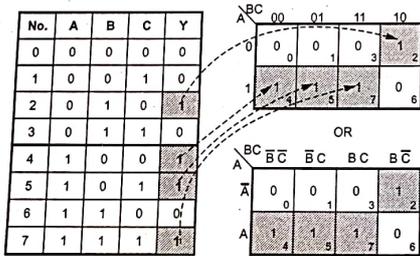
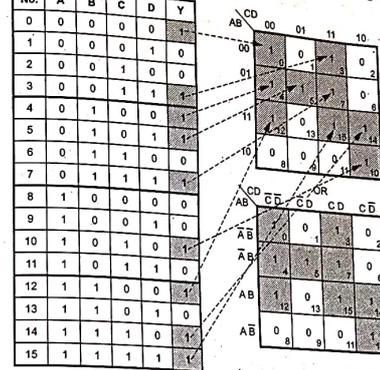


Fig. 4.2.6 (b) Representation of 3-variable truth table on K-map.

- The terms which are having output 1, have the corresponding cells marked with 1s. The other cells are marked with zeros.



(c) Representation of 4-variable truth table on K-map
Fig. 4.2.6 Plotting truth table on K-map

Note The student can verify the data in each cell by checking the data in the column Y for particular row number and the data in the same cell number in the K-map.

4.2.2.2 Representing Standard SOP on K-Map

- A Boolean expression in the sum of products form can be plotted on the Karnaugh map by placing a 1 in each cell corresponding to a term (minterm) in the sum of products expression. Remaining cells are filled with zeros. This is illustrated in the following examples.

Illustrative Examples

Example 4.2.1 Plot Boolean expression $Y = A\bar{B}C + ABC + \bar{A}BC$ on the Karnaugh map.

Solution : The expression has 3-variables and hence it can be plotted using 3-variable as in Fig. 4.2.7.

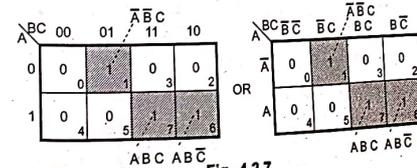


Fig. 4.2.7

Example 4.2.2 Plot Boolean expression $Y = ABC\bar{D} + A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D}$ on the Karnaugh map.

Solution: The expression has 4-variables and hence it can be plotted using 4-variable map as shown in Fig. 4.2.8.

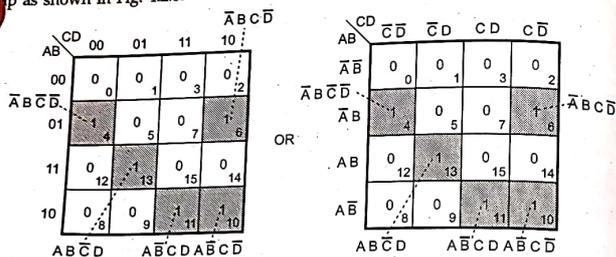


Fig. 4.2.8

4.2.2.3 Representing Standard POS on K-Map

- A Boolean expression in the product of sums can be plotted on the Karnaugh map by placing a 0 in each cell corresponding to a term (maxterm) in the expression. Remaining cells are filled with ones. This is illustrated in the following examples.

Illustrative Examples

Example 4.2.3 Plot Boolean expression $Y = (A + \bar{B} + C)(A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + C)(A + B + \bar{C})$ on the Karnaugh map.

Solution: The expression has 3-variables and hence it can be plotted using 3-variable map as shown in Fig. 4.2.9.

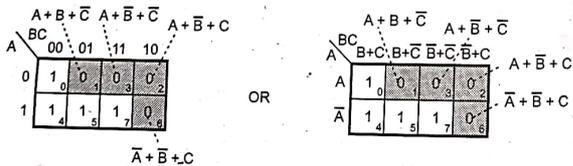


Fig. 4.2.9

$(A + \bar{B} + C) = M_2, (A + \bar{B} + \bar{C}) = M_3, (\bar{A} + \bar{B} + C) = M_6, (A + B + \bar{C}) = M_1$

Example 4.2.4 Plot Boolean expression.

$Y = (A + B + C + D)(A + \bar{B} + \bar{C} + D)(A + B + \bar{C} + \bar{D})(\bar{A} + \bar{B} + C + \bar{D})(\bar{A} + \bar{B} + \bar{C} + D)$

Solution: The expression has 4-variables and hence it can be plotted using 4-variable map as shown in Fig. 4.2.10.

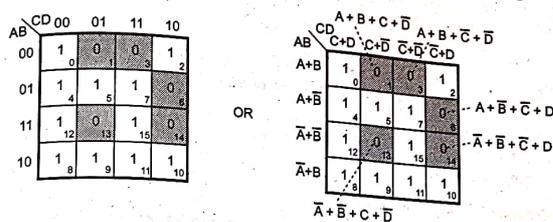
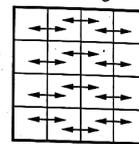


Fig. 4.2.10

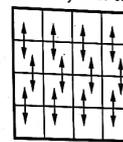
$(A + B + C + \bar{D}) = M_1, (A + \bar{B} + \bar{C} + D) = M_6, (A + B + \bar{C} + \bar{D}) = M_3, (\bar{A} + \bar{B} + C + \bar{D}) = M_{13}, (\bar{A} + \bar{B} + \bar{C} + D) = M_{14}$

4.2.3 Grouping Cells for Simplification

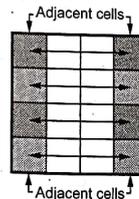
- Once the Boolean function is plotted on the Karnaugh map we have to use grouping technique to simplify the Boolean function.
- The grouping is nothing but combining terms in adjacent cells.



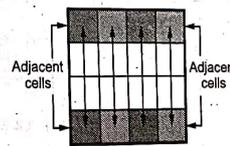
(a) Neighbouring cells in the row are adjacent



(b) Neighbouring cells in the column are adjacent



(c) Leftmost and corresponding rightmost cells are adjacent



(d) Top and corresponding bottom cells are adjacent

Fig. 4.2.11 Adjacent cells

- Two cells are said to be adjacent if they conform the single change rule. i.e. there is only one variable difference between co-ordinates of two cells. For example, the cells for minterms ABC and $\bar{A}BC$ are adjacent.
- The Fig. 4.2.11 shows the adjacent cells.
- The simplification is achieved by grouping adjacent 1s or 0s in groups of 2^i , where $i = 1, 2, \dots, n$ and n is the number of variables.
- When adjacent 1s are grouped then we get result in the sum of products form; otherwise we get result in the product of sums form. Let us see the various grouping rules.

4.2.3.1 Grouping Two Adjacent Ones (Pair)

- Fig. 4.2.12 (a) shows the Karnaugh map for a particular three variable truth table. This K-map contains a pair of 1s that are horizontally adjacent to each other; the first represents $\bar{A}\bar{B}C$ and the second represents $\bar{A}BC$. Note that in these two terms only the B variable appears in both normal and complemented form (\bar{A} and C remain unchanged). Thus these two terms can be combined to give a resultant that eliminates the B variable since it appears in both uncomplemented and complemented form. This is easily proved as follows :

$$\begin{aligned}
 Y &= \bar{A}\bar{B}C + \bar{A}BC \\
 &= \bar{A}C(\bar{B} + B) && \text{Rule 6 : } [A + \bar{A} = 1] \\
 &= \bar{A}C
 \end{aligned}$$

This same principle holds true for any pair of vertically or horizontally adjacent 1s.

- Fig. 4.2.12 (b) shows an example of two vertically adjacent 1s. These two can be combined to eliminate A variable since it appears in both its uncomplemented and complemented forms. This gives result

$$Y = \bar{A}BC + A\bar{B}C = BC$$

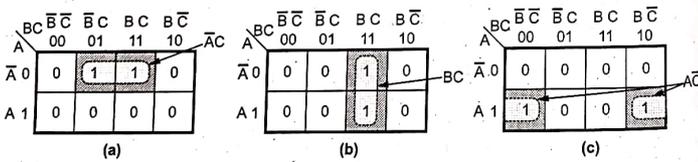


Fig. 4.2.12

- In a Karnaugh map the corresponding cells in the leftmost column and rightmost column are considered to be adjacent. Thus, the two 1s in these columns with a common row can be combined to eliminate one variable. This is illustrated in Fig. 4.2.12 (c).

Here variable B has appeared in both its complemented and uncomplemented forms and hence eliminated as follows :

$$\begin{aligned}
 Y &= A\bar{B}\bar{C} + AB\bar{C} \\
 &= A\bar{C}(\bar{B} + B) \\
 &= A\bar{C}
 \end{aligned}$$

- Let us see another example shown in Fig. 4.2.12 (d). Here two 1s from top row and bottom row of some column are combined to eliminate variable A, since in a K-map the top row and bottom row are considered to be adjacent.

$$\begin{aligned}
 Y &= \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D \\
 &= \bar{B}\bar{C}D(\bar{A} + A) \\
 &= \bar{B}\bar{C}D
 \end{aligned}$$

Rule 6 : $[\bar{A} + A = 1]$

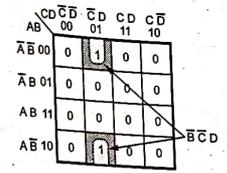


Fig. 4.2.12 (d)

- Fig. 4.2.12 (e) shows a Karnaugh map that has two overlapping pairs of 1s. This shows that we can share one term between two pairs.

$$\begin{aligned}
 Y &= \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC \\
 &= \bar{A}\bar{B}C + \bar{A}BC + \bar{A}BC + ABC \\
 &= \bar{A}C(\bar{B} + B) + BC(\bar{A} + A) \\
 &= \bar{A}C + BC
 \end{aligned}$$

Rule 5 : $[A + \bar{A} = 1]$

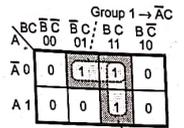


Fig. 4.2.12 (e)

- Fig. 4.2.12 (f) shows a K-map where three group of pairs can be formed. But only two pairs are enough to include all 1s present in the K-map. In such cases third pair is not required.

$$\begin{aligned}
 Y &= \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + A\bar{B}\bar{C} \\
 &= \bar{A}C(\bar{B} + B) + AB(C + \bar{C}) \\
 &= \bar{A}C + AB
 \end{aligned}$$

Rule 6 : $[\bar{A} + A = 1]$

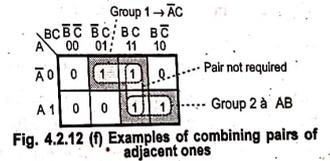


Fig. 4.2.12 (f) Examples of combining pairs of adjacent ones

A pair is a group of two adjacent cells in a Karnaugh map. It cancels one variable in a K-map simplification.

4.2.3.2 Grouping Four Adjacent Ones (Quad)

- In a Karnaugh map we can group four adjacent 1s. The resultant group is called Quad. Fig. 4.2.13 shows several examples of quads.

- Fig. 4.2.13 (a) shows the four 1s are horizontally adjacent.
- Fig. 4.2.13 (b) shows the four 1s are vertically adjacent.
- A K-map in Fig. 4.2.13 (c) contains four 1s in a square and they are considered adjacent to each other.

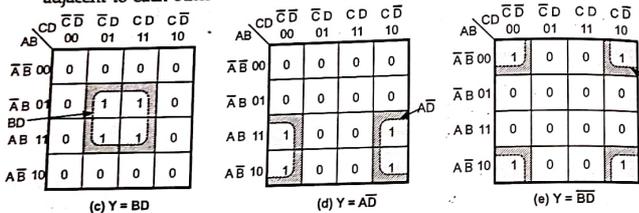


Fig. 4.2.13

- The four 1s in Fig. 4.2.13 (d) are also adjacent.
- In Fig. 4.2.13 (e) the top and bottom rows are considered to be adjacent to each other and the leftmost and rightmost columns are also adjacent to each other.
- When a quad is combined, two variables are eliminated. For example, in Fig. 4.2.13 (c) we have following terms with 4 variables :

$$\begin{aligned}
 Y &= \bar{A} \bar{B} \bar{C} D + \bar{A} \bar{B} C D + A \bar{B} \bar{C} D + A \bar{B} C D \\
 &= \bar{A} \bar{B} D (\bar{C} + C) + A \bar{B} D (\bar{C} + C) \\
 &= \bar{A} \bar{B} D + A \bar{B} D \\
 &= \bar{B} D (\bar{A} + A) \\
 &= \bar{B} D
 \end{aligned}$$

(Only two variables in the result, variables A and C are eliminated)

- Fig. 4.2.13 (f) shows overlapping groups. As mentioned earlier one term can be shared between two or more groups.

Quad is a group of four adjacent cells in a Karnaugh map. It cancels two variables in a K-map simplification.

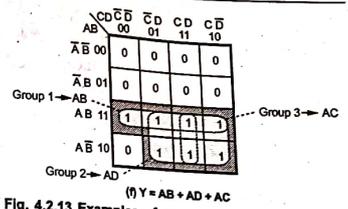


Fig. 4.2.13 Examples of combining quads of adjacent ones

4.2.3.3 Grouping Eight Adjacent Ones (Octet)

- In a Karnaugh map we can group eight adjacent 1s. The resultant group is called as octet. Fig. 4.2.14 shows several examples of octets.
- Fig. 4.2.14 (a) shows the eight 1s are horizontally adjacent.
- Fig. 4.2.14 (b) shows they are vertically adjacent.
- From the Fig. 4.2.14 we can easily observe that when an octet is combined in a four variable map, three of the four variables are eliminated because only one variable remains unchanged.

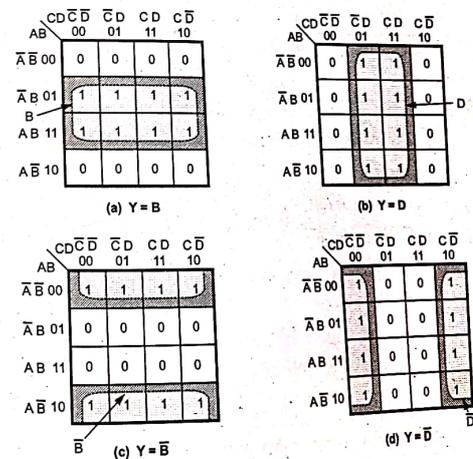


Fig. 4.2.14 Examples of combining octets of adjacent ones

- For example, in K-map shown in Fig. 2.3.14 (a) we have following terms :

$$\begin{aligned}
 Y &= \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD \\
 &+ AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD \\
 &= \bar{A}B\bar{C}(\bar{D} + D) + \bar{A}BC(D + \bar{D}) + AB\bar{C}(\bar{D} + D) + ABC(D + \bar{D}) \\
 &= \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C} + ABC = \bar{A}B(\bar{C} + C) + AB(\bar{C} + C) \\
 &= \bar{A}B + AB \\
 &= B(\bar{A} + A) = B
 \end{aligned}$$

Octet is a group of eight adjacent cells in a Karnaugh map. It cancels three variables in a K-map simplifications.

4.2.4 Illegal Grouping

- The Fig. 4.2.15 shows the examples of illegal grouping of cells.

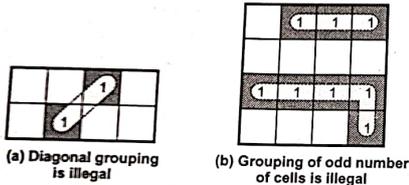


Fig. 4.2.15

Example 4.2.5 Using K-map find the boolean function and its complement for the following :

$$F(A, B, C, D) = \sum(1, 2, 3, 4, 6, 8, 9, 10, 11, 12, 14)$$

GTU : May-14, Marks 7

Solution :

$$\therefore F(A, B, C, D) = \bar{C}\bar{D} + B\bar{D} + A\bar{B} + \bar{B}D$$

and $\bar{F} = \overline{\bar{C}\bar{D} + B\bar{D} + A\bar{B} + \bar{B}D}$

$$\bar{F} = (\bar{C} + D)(\bar{B} + D)(\bar{A} + B)(B + \bar{D})$$

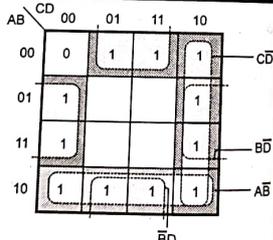


Fig. 4.2.16

Review Question

1. Explain SOP and POS forms of K-map for three variables.

4.3 Simplification SOP Functions using K-Maps

GTU : May-12, 13, Dec-12, 13, Summer-17, 18

- A pair of 1s eliminates one variable, a quad of 1s eliminates two variables and an octet of 1s eliminates three variables.
- In general, when a variable appears in both complemented and uncomplemented form within a group, that variable is eliminated from the resultant expression.
- Variables that are same in all with the group must appear in the final expression.
- Each group gives us a product term and summation of all product term gives us a Boolean expression.
- Each product term implies the function and, hence is an implicant of the function.
- All the implicants of a function determined using a Karnaugh map are the prime implicants.
- From the above discussion we can outline generalized procedure to simplify Boolean expressions as follows :
 1. Plot the K-map and place 1s in those cells corresponding to the 1s in the truth table or sum of product expression. Place 0s in other cells.
 2. Check the K-map for adjacent 1s and encircle those 1s which are not adjacent to any other 1s. These are called isolated 1s.
 3. Check for those 1s which are adjacent to only one other 1 and encircle such pairs.
 4. Check for quads and octets of adjacent 1s even if it contains some 1s that have already been encircled. While doing this make sure that there are minimum number of groups.
 5. Combine any pairs necessary to include any 1s that have not yet been grouped.
 6. Form the simplified expression by summing product terms of all the groups.

Illustrative Examples

Example 4.3.1 Minimize the expression $Y = \bar{A}B\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + \bar{A}B\bar{C}$.

Solution :

Step 1 : Fig. 4.3.1 (a) shows the K-map for three variables and it is plotted according to the given expression.

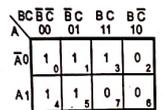


Fig. 4.3.1 (a)

Step 2 : There are no isolated 1s.

Step 3 : 1 in the cell 3 is adjacent only to 1 in the cell 1. This pair is combined and referred to as group 1.

Step 4 : There is no octet, but there is a quad. Cells 0, 1, 4 and 5 form a quad. This quad is combined and referred to as group 2.

Step 5 : All 1s have already been grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1, B variable is eliminated and in group 2, variables A and C are eliminated and we get,

$$Y = \bar{A}C + \bar{B}$$

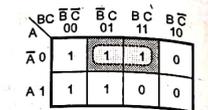


Fig. 4.3.1 (b)

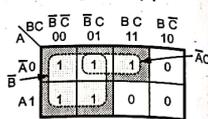


Fig. 4.3.1 (c)

Example 4.3.2 Minimize the expression

$$Y = \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D}$$

Solution :

Step 1 : Fig. 4.3.2 (a) shows the K-map for four variables and it is plotted according to the given expression.

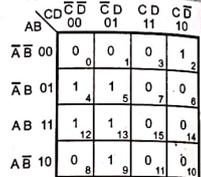


Fig. 4.3.2 (a)

Step 2 : Cell 2 is the only cell containing a 1 that is not adjacent to any other 1. It is referred to separately as group 1.

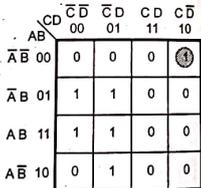


Fig. 4.3.2 (b)

Step 3 : 1 in the cell 9 is adjacent only to 1 in the cell 13. This pair is combined and referred to as group 2.

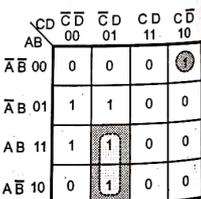


Fig. 4.3.2 (c)

Step 4 : There is no octet, but there is quad cells 4, 5, 12 and 13 form a quad. This quad is combined and referred to as group 3.

Step 5 : All 1s have already been grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1 variable is not eliminated. In group 2 variable B is eliminated and in group 3 variables A and D are eliminated and we get,

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}$$

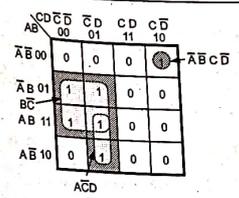


Fig. 4.3.2 (d)

Example 4.3.3 Reduce the following four variable function to its minimum sum of products form :

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D}$$

Solution :

Step 1 : Fig. 4.3.3 (a) shows the K-map for four variables and it is plotted according to the given expression.

Step 2 : There are no isolated 1s.

Step 3 : There are no such 1s which are adjacent to only one other 1.

Step 4 : There are three quads formed by cells 0, 2, 8, 10, cells 8, 10, 12, 14 and cells 2, 3, 10, 11. These quads are combined and referred to as group 1, group 2 and group 3 respectively.

Step 5 : All 1s have already been grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1 variables A and C are eliminated, in group 2 variables B and C are eliminated and in group 3 variables A and D are eliminated and we get,

$$Y = \bar{B}\bar{D} + \bar{A}\bar{D} + \bar{B}\bar{C}$$

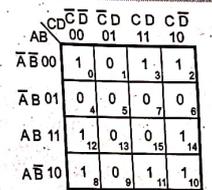


Fig. 4.3.3 (a)

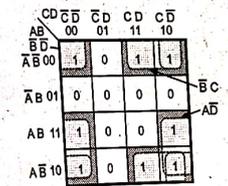


Fig. 4.3.3 (b)

Example 4.3.4 Reduce the following function to its minimum sum of products form :

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD$$

Solution :

Step 1 : Fig. 4.3.4 (a) shows the K-map for four variables and it is plotted according to the given expression.

Step 2 : There are no isolated 1s.

Step 3 : The 1 in the cell 1 is adjacent only to 1 in the cell 5, the 1 in the cell 6 is adjacent only to the 1 in the cell 7, the 1 in the cell 12 is adjacent only to the 1 in the cell 13 and the 1 in the cell 11 is adjacent only to the 1 in the cell 15. These pairs are combined and referred to as group 1-4 respectively.

Step 4 : There is no octet, but there is a quad. However, all 1s in the quad have already been grouped. Therefore this quad is ignored.

Step 5 : All 1s have already been grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1 variable B is eliminated. Similarly, in group 2-4 variables D, D and B are eliminated one in each group. We finally get minimum sum of products form as,

$$Y = \bar{A}\bar{C}D + \bar{A}BC + \bar{A}B\bar{C} + ACD$$

Example 4.3.5 Simplify the logic function specified by the truth Table 4.3.1 using the Karnaugh map method. Y is the output variable, and A, B and C are the input variables.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 4.3.1

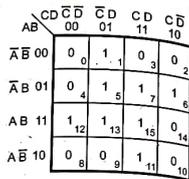


Fig. 4.3.4 (a)

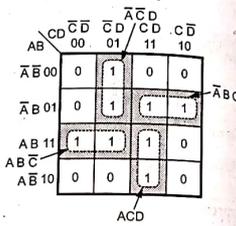


Fig. 4.3.4 (b)

Solution :

Step 1 : Fig. 4.3.5 (a) shows the K-map for three variables and it is plotted according to given truth table.

Step 2 : There are no isolated 1s.

Step 3 : The 1 in the cell 0 is adjacent only to 1 in the cell 4 and the 1 in the cell 3 is adjacent only to 1 in the cell 7. These two pairs are grouped and referred to as group 1 and group 2.

Step 4 : There is no octet and quad.

Step 5 : All 1s have already been grouped.

Step 6 : In group 1 and group 2 variable A is eliminated and we get,

$$Y = \bar{B}\bar{C} + BC$$

Example 4.3.6 Reduce the following function using Karnaugh map technique and implement using basic gates

$$f(A, B, C, D) = \bar{A}\bar{B}D + \bar{A}BC\bar{D} + \bar{A}BD + \bar{A}BC\bar{D}$$

Solution : The given function is not in the standard sum of products form. It is converted into standard SOP form as given below.

$$\begin{aligned} f(A, B, C, D) &= \bar{A}\bar{B}D + \bar{A}BC\bar{D} + \bar{A}BD + \bar{A}BC\bar{D} \\ &= \bar{A}\bar{B}D(C+\bar{C}) + \bar{A}BC\bar{D} + \bar{A}BD(C+\bar{C}) + \bar{A}BC\bar{D} \\ &= \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BCD \end{aligned}$$

Step 1 : Fig. 4.3.6 (a) shows the K-map for four variables and it is plotted according to expression in standard SOP form.

Step 2 : There are no isolated 1s.

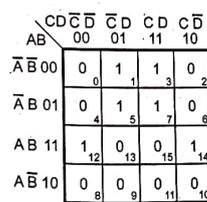


Fig. 4.3.6 (a)

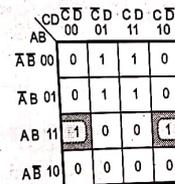


Fig. 4.3.6 (b)

Step 3 : The 1 in the cell 12 is adjacent only to the 1 in the cell 14. This pair is combined and referred to as group 1.

Step 4 : There is a quad. Cells 1, 3, 5 and 7 form a quad. This quad is referred to as group 2.

Step 5 : All 1s have already been grouped.

Step 6 : In group 1 variable C is eliminated and in group 2 variables B and C are eliminated. We get simplified equation as,

$$Y = AB\bar{D} + AD$$

Example 4.3.7 Reduce the following function using K-map technique.

$$f(A, B, C, D) = \sum m(0, 1, 4, 8, 9, 10).$$

Solution :

Step 1 : Fig. 4.3.7 (a) shows the K-map for four variables and it is plotted according to given minterms.

Step 2 : There are no isolated 1s.

Step 3 : Cell 4 is adjacent only to cell 0 and cell 10 is adjacent only to cell 8. These two pairs are combined and referred to as group 1 and group 2 respectively.

Step 4 : There is a quad. Cells 0, 1, 8 and 9 form a quad. This quad is referred to as group 3.

Step 5 : All 1s have already been grouped.

Step 6 : In group 1, B and in group 2, C are eliminated respectively. In group 3, A and D are eliminated and finally we get

$$f(A, B, C, D) = \overline{A}C\bar{D} + A\bar{B}\bar{D} + \overline{B}\bar{C}$$

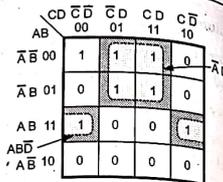


Fig. 4.3.6 (c)

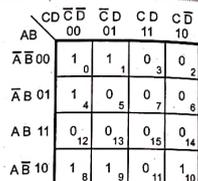


Fig. 4.3.7 (a)

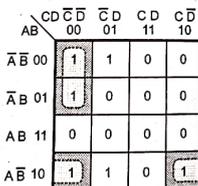


Fig. 4.3.7 (b)

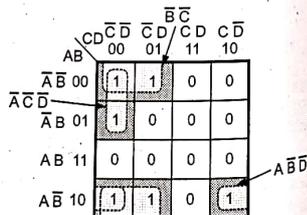


Fig. 4.3.7 (c)

Example 4.3.8 Obtain the simplified expression in sum of product for the following boolean functions.

a) $F = \sum(0, 1, 4, 5, 10, 11, 12, 14)$ b) $F = \sum(11, 12, 13, 14, 15)$

GTU - May-13, Marks 7

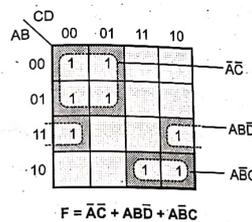
Solution : a) $F = \sum(0, 1, 4, 5, 10, 11, 12, 14)$

$$F = \overline{A}\overline{C} + AB\bar{D} + A\overline{B}\overline{C}$$

$$F = \sum(11, 12, 13, 14, 15)$$

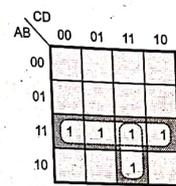
$$F = AB + ACD$$

b)



$$F = \overline{A}\overline{C} + AB\bar{D} + A\overline{B}\overline{C}$$

(a)



$$F = AB + ACD$$

(b)

Fig. 4.3.8

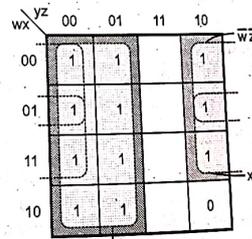
Example 4.3.9 Simplify the boolean function with Karnaugh map.

$$F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$

GTU - Dec-13, Marks 3

Solution : $F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

$$F(w, x, y, z) = \overline{y} + \overline{wz} + xz$$



$$F(w, x, y, z) = \overline{y} + \overline{wz} + xz$$

Fig. 4.3.9

Example 4.3.10 Simplify the boolean function with K-map :

$$F = \overline{A}BC + \overline{B}CD + \overline{A}BCD + A\overline{B}C$$

Solution : $F = \overline{A}BC + \overline{B}CD + \overline{A}BCD + A\overline{B}C$
 $F = \overline{B}C + \overline{B}D + \overline{A}C\overline{D}$

GTU : May-12, Dec.-13, Marks 4

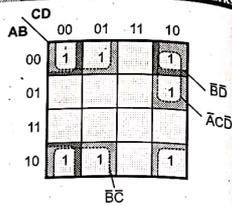


Fig. 4.3.10

Example 4.3.11 Reduce to simplest form using K-map : $F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10)$

GTU : Summer-18, Marks 4

Solution :

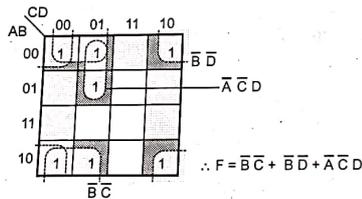


Fig. 4.3.11

Examples for Practice

Example 4.3.12 : Simplify following logical expression using Karnaugh maps
 $Y = A\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}C + \overline{A}BC + ABC$ [Ans. : $Y = A\overline{B} + C$]

Example 4.3.13 : Simplify the following function
 $f_1(A, B, C, D) = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$
 [Ans. : $(A \oplus B) \odot (C \oplus D)$]

Example 4.3.14 : Simplify the following function
 $f_3(A, B, C, D) = \sum m(0, 1, 2, 3, 11, 12, 14)$
 [Ans. : $\overline{A}\overline{B} + AB\overline{D} + \overline{B}CD$]

Example 4.3.15 : Simplify the following using K-map.
 $X = A'B + A'B'C + ABC' + AB'C'$
 [Ans. : $X = \overline{A}C + B$]

Example 4.3.16 : Solve the following using minimization technique
 $Z = f(A, B, C, D) = \sum(0, 2, 4, 7, 11, 13, 15)$
 [Ans. : $Z = \overline{A}\overline{B}D + \overline{A}C\overline{D} + BCD + ABD + ACD$]

4.3.1 Essential Prime Implicants

- After grouping the cells, the sum terms which appear in the K-map are called prime implicants groups.
- It is observed that some cells may appear in only one prime implicants group; while other cells may appear in more than one prime implicants group.
- In Fig. 4.3.7 (c), cells 1, 4, 9 and 10 appear in only one prime implicants group. These cells are called essential cells and corresponding prime implicants are called essential prime implicants.

4.3.2 Incompletely Specified Functions (Don't Care Terms)

- In some logic circuits, certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either HIGH or LOW. These output levels are indicated by 'X' or 'd' in the truth tables and are called don't care outputs or don't care conditions or incompletely specified functions.
- As shown in truth table given by Table 4.3.2, outputs are defined for input conditions from 000 to 101. For remaining two conditions of input, output is not defined, hence these are called don't care conditions for this truth table.
- A circuit designer is free to make the output for any "don't care" condition either a '0' or a '1' in order to produce the simplest output expression.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	X

Table 4.3.2

4.3.2.1 Describing Incomplete Boolean Function

- We can describe the Boolean function using either a minterm canonical formula or a maxterm canonical formula.
- In order to obtain similar-type expressions for incomplete Boolean functions we use additional term to specify don't care conditions in the original expression. This is illustrated in the following examples. In expression,

$$f(A, B, C) = \sum m(0, 2, 4) + d(1, 5)$$

minterms are 0, 2 and 4. The additional term $d(1, 5)$ is introduced to specify the don't care conditions.

- This term specifies that outputs for minterms 1 and 5 are not specified and hence these are don't care conditions.
- Letter d is used to indicate don't care conditions in the expression.
- The above expression indicates how to represent don't care conditions in the minterm canonical formula. In the similar manner, we can specify the don't care conditions in the maxterm canonical formula. For example,

$$f(A, B, C) = \prod M(2, 5, 7) + d(1, 3)$$

4.3.2.2 Don't Care Conditions in Logic Design

- Consider the logic circuit for an even parity generator for 4-bit BCD number. The Table 4.3.3 shows the truth table for even-parity generator.
- The truth table shows that the output for last six input conditions cannot be specified, because such input conditions does not occur when input is in the BCD form.
- The Boolean function for even parity generator with 4-bit BCD input can be expressed in minterm canonical formula as,

$$f(A, B, C, D) = \sum m(1, 2, 4, 7, 8) + d(10, 11, 12, 13, 14, 15)$$

A	B	C	D	P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	-
1	0	1	1	-
1	1	0	0	-
1	1	0	1	-
1	1	1	0	-
1	1	1	1	-

Table 4.3.3 Truth table for even parity generator with 4-bit BCD input

4.3.2.3 Minimization of Incompletely Specified Functions

- A circuit designer is free to make the output for any don't care condition either a 0 or 1 in order to produce the simplest output expression.
- Consider a truth table shown in Table 4.3.4. The K-map for this truth table is shown in Fig. 4.3.12 with x placed in the ABC and ABC cells.
- It is not always advisable to put don't cares as 1s. This is illustrated in Fig. 4.3.12 (b). Here, the don't care

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	X

Table 4.3.4

output for cell ABC is taken as 1 to form a quad and don't care output for cell ABC is taken as 0, since it is not helping any way to reduce an expression. Using don't care conditions in this way we get the simplified Boolean expression as

$$Y = C$$

- It is important to decide which don't cares to change to 0 and which to 1 to produce the best K-map grouping (i.e. the simplest expression).

Illustrative Examples

Example 4.3.17 Find the reduced SOP form of the following function.

$$f(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 4)$$

Solution :

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
AB	00	01	11	10	
$\bar{A}\bar{B}$ 00	X	1	1	X	2
$\bar{A}\bar{B}$ 01	X	4	5	1	0
$\bar{A}B$ 11	0	12	13	15	0
$\bar{A}B$ 10	0	8	9	11	0

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
AB	00	01	11	10	
$\bar{A}\bar{B}$ 00	1	1	1	1	-
$\bar{A}\bar{B}$ 01	0	0	1	0	-
$\bar{A}B$ 11	0	0	1	0	-
$\bar{A}B$ 10	0	0	1	0	-

Fig. 4.3.13

- To form a quad of cells 0, 1, 2 and 3 the don't care conditions 0 and 2 are replaced by 1s.
- The remaining don't care condition is replaced by 0 since it is not required to form any group. With these replacements we get the simplified equation as

$$f(A, B, C, D) = \bar{A}\bar{B} + CD$$

Group 1 Group 2

Example 4.3.18 Find the prime implicants for the following function and determine which are essential. $F(w, x, y, z) = \sum (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

Solution :

- The minterms of the given function are marked with 1's in the map of Fig. 4.3.14.

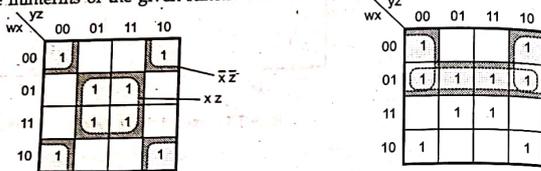


Fig. 4.3.14

- The Fig. 4.3.14 (a) shows two essential prime implicants.
- The term xz is essential because there is only one way to include minterms m_8 and m_{15} within four adjacent squares.
- There is only one way that minterms m_8 and m_{10} can be combined with four adjacent squares and this gives second term $\bar{x}z$.
- The two essential prime implicants cover eight minterms.
- The remaining two minterms, m_4 and m_6 must be considered next.
- The Fig. 4.3.14 shows the two possible ways of including remaining two minterms with prime implicants.
- Minterms m_4 and m_6 can be included with either $\bar{w}x$ or $\bar{w}z$.
- The simplified expression is obtained from the logical sum of the two essential prime implicants and any one prime implicant that includes minterms m_4 and m_6 .
- There are two possible ways that the function can be expressed in the simplified form :

$$F = \bar{x}z + xz + \bar{w}x = \bar{x}z + xz + \bar{w}z$$

Example 4.3.19 Express the following function as the minimal sum of products using a K-map. $f(a,b,c,d) = \Sigma(0,2,4,5,6,8,10,15) + \Sigma\phi(7,13,14)$

Solution :

- As shown in Fig. 4.3.15 the given example has three solutions and all are correct. Students are expected to give any one solution.

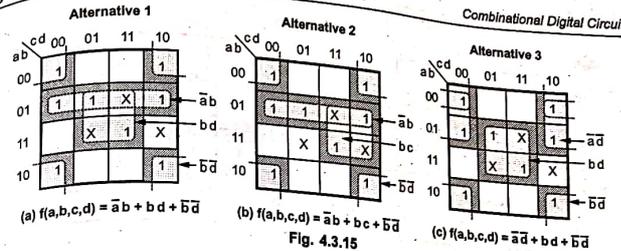


Fig. 4.3.15

Example 4.3.20 Implement the functions $F = \Sigma(1, 3, 7, 11, 15)$ with don't care conditions $d = \Sigma(0, 2, 5)$.

GTU : May-13, Dec.-13, Marks 5

Solution : $F = \Sigma(1, 3, 7, 11, 15) + \Sigma(0, 2, 5)$

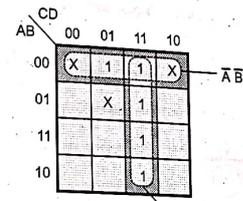


Fig. 4.3.16

$$F = \bar{A}\bar{B} + CD$$

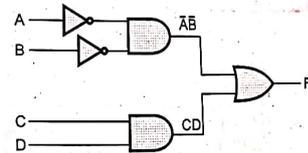


Fig. 4.3.17

Example 4.3.21 Obtain the simplified expression in sum of product using K-map :

$$xz + \bar{w}xy + w(\bar{x}y + x\bar{y})$$

GTU : Dec.-12, Marks 7

Solution : $F = \bar{x}z + \bar{w}x\bar{y} + w(\bar{x}y + x\bar{y})$

$$F = \bar{x}z + \bar{w}x\bar{y} + w\bar{x}y + wx\bar{y}$$

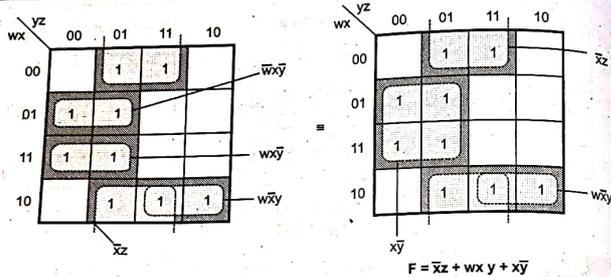


Fig. 4.3.18

$\therefore F = \bar{x}z + w\bar{x}y + x\bar{y}$

Example 4.3.22 Simplify Boolean function using K-map

$F(w, x, y, z) = \sum(1, 3, 5, 8, 9, 11, 15)$

$d(w, x, y, z) = \sum(2, 13)$

GTU : Summer-17, Marks 4

Solution : $F = w\bar{x}y + \bar{y}z + wz + \bar{x}z$

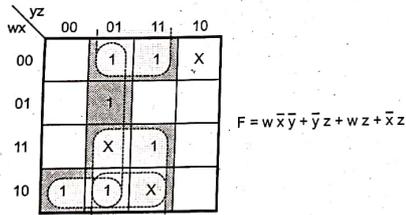


Fig. 4.3.19

Examples for Practice

Example 4.3.23 : Simplify the following switching function using Karnaugh map

$F(A, B, C, D) = \sum(0, 5, 7, 8, 9, 10, 11, 14, 15) + \phi(1, 4, 13)$

[Ans. : $\bar{B}\bar{C} + BD + AC$]

Example 4.3.24 : Determine the minimal sum of product form of

$F(w, x, y, z) = \sum m(4, 5, 7, 12, 14, 15) + d(3, 8, 10)$

[Ans. : $\bar{w}x\bar{y} + xyz + w\bar{z}$]

Review Questions

1. Give the steps for simplification of SOP expression.
2. What do you mean by essential prime implicants ?
3. What is don't care condition ?

4.4 Simplification of POS Functions using K-Maps

GTU : Winter-17

- In practice, the designer should examine both the sum of products and product of sums reductions to ascertain which is more simplified.
 - Once the expression is plotted on the K-map for POS reductions is a simple step by step process and it is similar to the one used earlier.
 - Each group of zero results a sum term and it is nothing but the **prime implicant**. The technique for using maps for POS reductions is a simple step by step process.
1. Plot the K-map and place 0s in those cells corresponding to the 0s in the truth table or maxterms in the product of sums expression.
 2. Check the K-map for adjacent 0s and encircle those 0s which are not adjacent to any other 0s. These are called isolated 0s.
 3. Check for those 0s which are adjacent to only one other 0 and encircle such pairs.
 4. Check for quads and octets of adjacent 0s even if it contains some 0s that have already been encircled. While doing this make sure that there are minimum number of groups.
 5. Combine any pairs necessary to include any 0s that have not yet been grouped.
 6. Form the simplified POS expression for F by taking product of sum terms of all the groups.

To get familiar with these steps we will solve some examples.

Illustrative Examples

Example 4.4.1 Minimize the expression

$Y = (A + B + C)(A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + C)(\bar{A} + B + C)(A + B + C)$

Solution : $(A + B + \bar{C}) = M_1, (A + \bar{B} + \bar{C}) = M_3,$

$(\bar{A} + \bar{B} + \bar{C}) = M_7, (\bar{A} + B + C) = M_4,$

$(A + B + C) = M_0$

Step 1 : Fig. 4.4.1 (a) shows the K-map for three variable and it is plotted according to given maxterms.

Step 2 : There are no isolated 0s.

Step 3 : 0 in the cell 4 is adjacent only to 0 in the cell 0 and 0 in the cell 7 is adjacent only to 0 in the cell 3. These two pairs are combined and referred to as group 1 and group 2 respectively.

Step 4 : There are no quads and octets.

Step 5 : The 0 in the cell 1 can be combined with 0 in the cell 3 to form a pair. This pair is referred to as group 3.

Step 6 : In group 1 and in group 2, A is eliminated, whereas in group 3 variable B is eliminated and we get,

$$Y = (B + C)(\bar{B} + \bar{C})(A + \bar{C})$$

	BC	B+C	B+C	$\bar{B} + \bar{C}$	$\bar{B} + \bar{C}$
A	00	01	11	10	
A 0	0	0	1	0	2
\bar{A} 1	0	1	0	0	8

Fig. 4.4.1 (a)

	BC	B+C	B+C	$\bar{B} + \bar{C}$	$\bar{B} + \bar{C}$
A	00	01	11	10	
A 0	0	0	0	0	
\bar{A} 1	0	0	0	0	

Fig. 4.4.1 (b)

	BC	B+C	B+C	$\bar{B} + \bar{C}$	$\bar{B} + \bar{C}$
A	00	01	11	10	
A 0	0	0	0	0	
\bar{A} 1	0	0	0	0	

Group 3 → A + \bar{C}
Group 2 → $\bar{B} + \bar{C}$
Group 1 → B + C

Fig. 4.4.1 (c)

Example 4.4.2 Minimize the following expression in the POS form

$$Y = (\bar{A} + \bar{B} + C + D)(\bar{A} + \bar{B} + \bar{C} + D)(\bar{A} + \bar{B} + C + \bar{D})(\bar{A} + B + C + D)(A + \bar{B} + \bar{C} + D)(A + \bar{B} + \bar{C} + \bar{D})(A + B + C + D)(\bar{A} + \bar{B} + C + \bar{D})$$

Solution :

$$(\bar{A} + \bar{B} + C + D) = M_{12}, (\bar{A} + \bar{B} + \bar{C} + D) = M_{14}, (\bar{A} + \bar{B} + C + \bar{D}) = M_{15}$$

$$(\bar{A} + B + C + D) = M_8, (A + \bar{B} + \bar{C} + D) = M_6, (A + \bar{B} + \bar{C} + \bar{D}) = M_7$$

$$(A + B + C + D) = M_0 \text{ and } (\bar{A} + \bar{B} + C + \bar{D}) = M_{13}$$

Step 1 : Fig. 4.4.2 (a) shows the K-map for four variable and it is plotted according to given maxterms.

Step 2 : There are no isolated 0s.

	CD	C+D	C+ \bar{D}	$\bar{C} + \bar{D}$	$\bar{C} + D$
AB	00	01	11	10	
A+B 00	0	1	3	2	
A+ \bar{B} 01	4	5	7	6	
\bar{A} + \bar{B} 11	0	0	0	0	
\bar{A} +B 10	0	0	0	0	

Fig. 4.4.2 (a)

Step 3 : 0 in the cell 0 is adjacent only to 0 in the cell 8. This pair is combined and referred to as group 1.

Step 4 : There are two quads. Cells 12, 13, 14 and 15 forms a quad 1 and cells 6, 7, 14, 15 forms a quad 2. These two quads are referred to as group 2 and group 3, respectively.

Step 5 : All 0s have already been grouped.

Step 6 : In group 1, variable A is eliminated. In group 2, variable C and D are eliminated and in group 3 variables A and D are eliminated. Therefore we get simplified POS expression as,

$$Y = (B + C + D)(\bar{A} + \bar{B})(\bar{B} + \bar{C})$$

	CD	C+D	C+ \bar{D}	$\bar{C} + \bar{D}$	$\bar{C} + D$
AB	00	01	11	10	
A+B 00	0	1	3	2	
A+ \bar{B} 01	4	5	7	6	
\bar{A} + \bar{B} 11	0	0	0	0	
\bar{A} +B 10	0	0	0	0	

Fig. 4.4.2 (b)

	CD	C+D	C+ \bar{D}	$\bar{C} + \bar{D}$	$\bar{C} + D$
AB	00	01	11	10	
A+B 00	0	1	3	2	
A+ \bar{B} 01	4	5	7	6	
\bar{A} + \bar{B} 11	0	0	0	0	
\bar{A} +B 10	0	0	0	0	

Group 1 → (B + C + D)
Group 2 → ($\bar{A} + \bar{B}$)
Group 3 → ($\bar{B} + \bar{C}$)

Fig. 4.4.2 (c)

Example 4.4.3 Reduce the following function using K-map technique

$$f(A, B, C, D) = \Pi M(0, 2, 3, 8, 9, 12, 13, 15)$$

Solution :

Step 1 : Fig. 4.4.3 (a) shows the K-map for four variables and it is plotted according to given maxterms.

Step 2 : There are no isolated 0s.

Step 3 : The 0 in the cell 15 is adjacent only to 0 in the cell 13 and 0 in the cell 3 is adjacent only to 0 in the cell 2. These two pairs are combined and referred to as group 1 and group 2, respectively.

	CD	C+D	C+ \bar{D}	$\bar{C} + \bar{D}$	$\bar{C} + D$
AB	00	01	11	10	
A+B 00	0	1	3	2	
A+ \bar{B} 01	4	5	7	6	
\bar{A} + \bar{B} 11	0	0	0	0	
\bar{A} +B 10	0	0	0	0	

Fig. 4.4.3 (a)

	CD	C+D	C+ \bar{D}	$\bar{C} + \bar{D}$	$\bar{C} + D$
AB	00	01	11	10	
A+B 00	0	1	3	2	
A+ \bar{B} 01	4	5	7	6	
\bar{A} + \bar{B} 11	0	0	0	0	
\bar{A} +B 10	0	0	0	0	

Fig. 4.4.3 (b)

Step 4 : The cells 8, 9, 12 and 13 form a quad which is referred to as group 3.

Step 5 : The remaining 0 in the cell 0 is combined with the 0 in the cell 2 to form a pair, which is referred to as group 4.

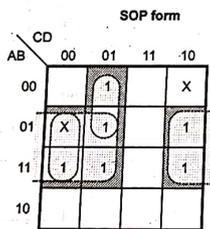
Step 6 : In group 1 and in group 4 variable C is eliminated. In group 2 variable D is eliminated and in group 3 variables B and D are eliminated. Therefore, we get simplified expression in POS form as,
 $f = (\bar{A} + \bar{B} + \bar{D})(A + B + \bar{C})(\bar{A} + C)(A + B + D)$

Example 4.4.4 Reduce the expression in SOP and POS form using K-map.

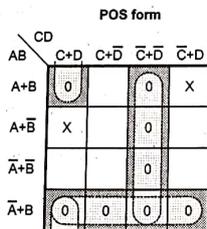
$$F(A, B, C, D) = \sum m(1, 5, 6, 12, 13, 14) + d(2, 4)$$

GTU : Winter-17, Marks 7

Solution :



$$F = B\bar{C} + B\bar{D} + \bar{A}\bar{C}D$$



$$F = (\bar{A} + B)(\bar{C} + \bar{D})(B + C + D)$$

Fig. 4.4.4

Examples for Practice

Example 4.4.5 : Simplify the following Boolean function for minimal POS form
 $F(w, x, y, z) = \pi M(4, 5, 6, 7, 8, 12) + d(1, 2, 3, 9, 11, 14)$

[Ans. : $(w + x)(\bar{w} + y + z)$]

Example 4.4.6 : Reduce the following function using K-map
 $F(A, B, C) = \pi M(0, 1, 2, 3, 4, 7)$

[Ans. : $F = A(\bar{B} + \bar{C}) \cdot (B + C)$]

Example 4.4.7 : Solve the following using minimization technique
 $Z = f(A, B, C, D) = \pi(1, 2, 3, 6, 8, 11, 14, 15)$

[Ans. : $Z = (A + B + \bar{D})(A + B + \bar{C})(\bar{B} + \bar{C} + D)(\bar{A} + \bar{C} + \bar{D})(\bar{A} + B + C + D)$]

Review Question

1. Give the steps for simplification of POS expression.

4.5 Summary of Rules for K-Map Simplification

Rules for simplifying logic function using K-map are :

1. Group should not include any cell containing a zero.
2. The number of cells in a group must be a power of 2, such as 1, 2, 4, 8 or 16.
3. Group may be horizontal, vertical but not diagonal.
4. Cell containing 1 must be included in at least one group.
5. Groups may overlap.
6. Each group should be as large as possible to get maximum simplification.
7. Groups may be wrapped around the map. The leftmost cell in a row may be grouped with the rightmost cell and the top cell in a column may be grouped with the bottom cell.
8. A cell may be grouped more than once. The only condition is that every group must have at least one cell that does not belong to any other group. Otherwise, redundant terms will result.
9. We need not group all don't care cells, only those that actually contribute to a maximum simplification.
10. All above rules are stated considering the SOP simplification. In case of POS simplification all rules are same except 0 (zero) takes place of 1 (one).

Review Question

1. State the rules for K-map simplification.

4.6 Limitation of Karnaugh Map

- The map method of simplification is convenient as long as the number of variables does not exceed five or six. As the number of variables increases it is difficult to make judgements about which combinations form the minimum expression. In case of complex problem with 7, 8 or even 10 variables it is almost an impossible task to simplify expression by the mapping method.
- The K-map simplification is manual technique and simplification process is heavily depends on the human abilities.

To meet this need, W. V. Quine and E. J. McCluskey developed an exact tabular method to simplify the Boolean expression. This method is called the Quine McCluskey or tabular method.

Review Question

1. Explain the limitations of Karnaugh map.

4.7 Realizing Logic Function with Gates

GTU : Dec-11, 12, 13, May-12, 13, Summer-15, 16, 18, Winter-14, 15, 18

- The Boolean algebra is used to express the output of any combinational network. Such a network can be implemented using logic gates.

4.7.1 Implementation of SOP Boolean Expression

- Consider the Boolean expression

$$F = AB + C\bar{D} + \bar{B}C$$

- In this expression, we have three product terms with 2 literals in each product term.
- We can implement these product terms by using three 2-input AND gates, as shown in the Fig. 4.7.1.

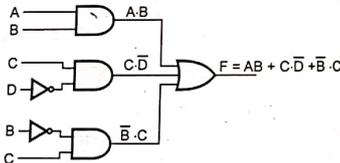


Fig. 4.7.1 Implementation of SOP Boolean expression

- Expression tells that these product terms should be ORed to get the output F.
- We have three product terms so we have to use 3-input OR gate to obtain the sum of products.
- Literals are complemented using NOT gates.

4.7.2 Implementation of POS Boolean Expression

- Consider the Boolean expression

$$F = (A + B)(\bar{B} + C)(\bar{C} + D + E)$$

- In this expression, we have three sum terms with 2 literals in two terms and 3 literals in one term.

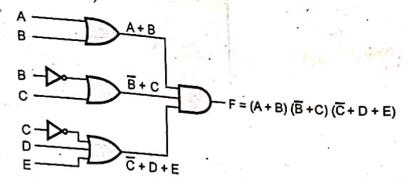


Fig. 4.7.2 Implementation of POS Boolean expression

- We can implement these sum terms by using two 2-input OR gates and one 3-input OR gate, as shown in the Fig. 4.7.2.

- Expression tells that these product terms should be ANDed to get the output F.
- We have three sum terms so we have to use 3-input AND gate to obtain the product of sums.
- Literals are complemented using NOT gates.
- In the previous examples we have seen that simplified SOP Boolean expression can be implemented using AND-OR gates.
- The AND-OR implementation is a two level implementation. In the first level we implement all product terms using AND gates and in the second level all product terms are logically ORed using OR gate.
- In case of POS expression we use OR-AND implementation. Here, we implement all sum terms using OR gates in the first level and all sum terms are logically ANDed using AND gate, to get product of sum, in the second level.
- The logic gates are available in the Integrated Circuit (IC) packages. When we implement logic circuit using basic gates, we require ICs for AND, OR and NOT gates.

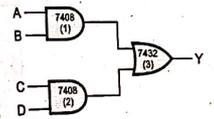


Fig. 4.7.3

- Many times it may happen that all gates from the IC packages are not required to build the circuit and thus remaining gates are unused.
- Consider a combinational circuit which requires two 2-input AND gates and one 2-input OR gate as shown in Fig. 4.7.3.
- To implement such a circuit we require IC 7408 (Four 2-input AND gates) and IC 7432 (Four 2-input OR gate).

- When we use these two ICs we find that two 2-input AND gates are unused and three 2-input OR gates are unused. Thus, the utility factor is very poor.
- The utility factor can be increased by using universal gates to implement logic functions.

Example 4.7.1 For the following function implement the SOP and POS circuit.

$$F(A, B, C, D) = \sum m(2, 3, 5, 7, 12) + \sum d(6, 13, 14, 15)$$

GTU : Dec.-11, Marks 10

Solution :

$$F = AB + BD + \bar{A}C$$

	CD	00	01	11	10	
AB	00			1	1	$\bar{A}C$
	01		1	1	X	BD
	11	1	X	X	X	AB
	10					

Implement using SOP circuit

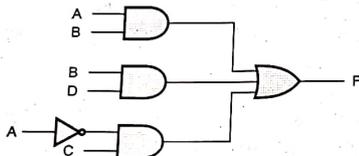


Fig. 4.7.4

Implementation using POS circuit

$$F = \overline{\overline{AB + BD + AC}} = \overline{\overline{AB} \cdot \overline{BD} \cdot \overline{AC}} = (\overline{\overline{AB}}) \cdot (\overline{\overline{BD}}) \cdot (\overline{\overline{AC}})$$

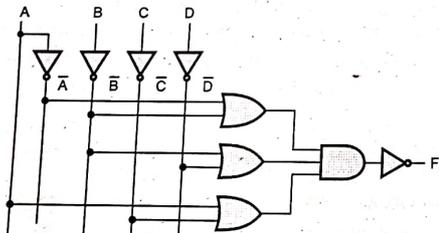


Fig. 4.7.5

Example 4.7.2 Given Boolean function $F = xy + \bar{x}y + \bar{y}z$.

1) Implement it with only OR and NOT gates.

2) Implement it with only AND and NOT gates.

GTU : May-12, Marks 5

Solution : 1) The given Boolean function is

$$\begin{aligned} \bar{F} &= \overline{xy + \bar{x}y + \bar{y}z} \\ &= \overline{(xy) \cdot (\bar{x}y) \cdot (\bar{y}z)} \\ &= \overline{(x + \bar{x}) \cdot (x + y) \cdot (y + \bar{z})} \\ &= \overline{(x + \bar{x})} + \overline{(x + y)} + \overline{(y + \bar{z})} \end{aligned}$$

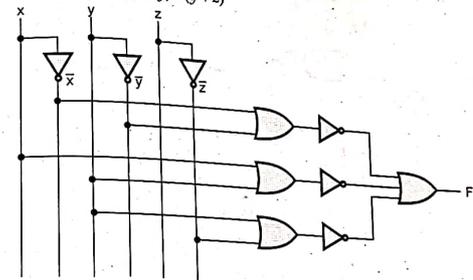


Fig. 4.7.6 Logic diagram using OR and NOT gates

2)

$$\begin{aligned} F &= xy + \bar{x}y + \bar{y}z \\ &= xy + \bar{x}y + \bar{y}z = \overline{(\overline{xy}) \cdot (\overline{\bar{x}y}) \cdot (\overline{\bar{y}z})} \end{aligned}$$

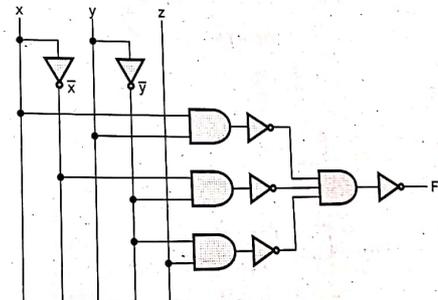


Fig. 4.7.7 Logic diagram using AND and NOT gates

Example 4.7.3 Implement the Boolean functions a) $xyz + \bar{x}y + xy\bar{z}$, b) $(A+B)(\bar{A}+\bar{B})$, c) $F = xy + x\bar{y} + yz$ with logic gates.

GTU : May-13, Marks 7

Solution : a) $xyz + \bar{x}y + xy\bar{z}$

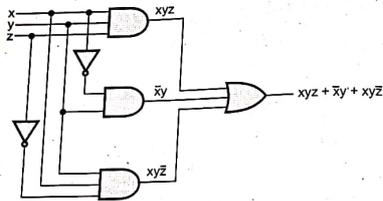


Fig. 4.7.8

b) $(A+B)(\bar{A}+\bar{B})$

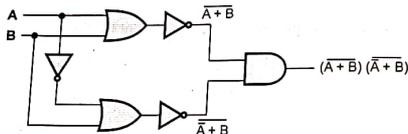


Fig. 4.7.9

c) $F = xy + x\bar{y} + yz$

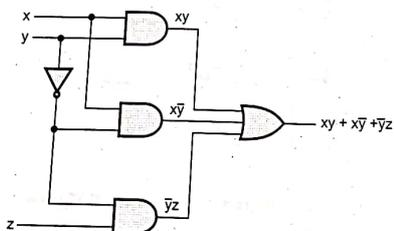


Fig. 4.7.10

Example 4.7.4 Reduce the given function using K-map and implement the same using gates.
 $F(A, B, C, D) = \sum m(0,1,3,7,11,15) + \sum d(2,4)$

GTU : Summer-15, Marks 7

Solution :

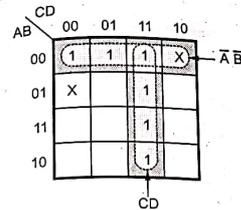


Fig. 4.7.11

Implementation

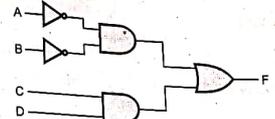
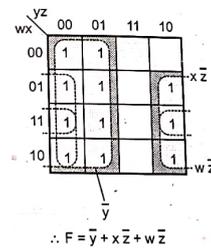


Fig. 4.7.12

Example 4.7.5 Solve the following Boolean by using K-map. Implement the simplified function by using logic gates. $F = (w,x,y,z) = \sum (0,1,4,5,6,8,9,10,12,13,14)$

GTU : Winter-18, Marks 7

Solution :



$\therefore F = \bar{y} + x\bar{z} + w\bar{z}$

Implementation

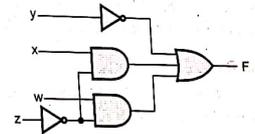


Fig. 4.7.13

Definition : A state machine is a device which can be in one of a set number of stable conditions depending on its previous condition and on the present values of its inputs.

Examples for Practice

Example 4.7.6 : Minimize the following function using K-map and implement using logic gates.

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14).$$

[Ans.: $\overline{A}D + \overline{B}C + \overline{B}D + \overline{A}B + ABCD$]

Example 4.7.7 : Reduce the following function using K-map technique and implement using gates :

$$F(A, B, C, D) = \sum m(0, 1, 4, 8, 9, 10) + d(2, 11).$$

[Ans.: $\overline{B}C + \overline{A}CD + \overline{A}B$]

Example 4.7.8 : Minimize the following expression using K-map and implement it using basic gates.

i) $F(A, B, C, D) = \sum m(1, 4, 8, 12, 13, 15) + d(3, 14)$

ii) $F(A, B, C, D) = \sum m(1, 7, 9, 10, 11, 15) + d(2, 3, 5).$

[Ans.: i) $\overline{A}BD + \overline{B}CD + \overline{A}CD + AB$, ii) $\overline{B}C + \overline{B}D + CD$]

Example 4.7.9 : For the following function implement the SOP and POS circuit.

$$F(A, B, C, D) = \sum m(2, 3, 5, 7) + \sum d(6, 13, 14, 15)$$

GTU : Dec-12, Marks 10

[Ans.: $F = BD + \overline{A}C$ and $\overline{F} = (\overline{A})(C + D)(A + B + C)$]

4.7.3 Universal Gates

- The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND or NOR gates.

4.7.3.1 NAND Gate

- The NAND gate can be used to generate the NOT function, the AND function, the OR function, and the NOR function.

NOT Function :

An inverter can be made from a NAND gate by connecting all of the inputs together and creating, in effect, a single common input, as shown in Fig. 4.7.14, for a two-input gate.

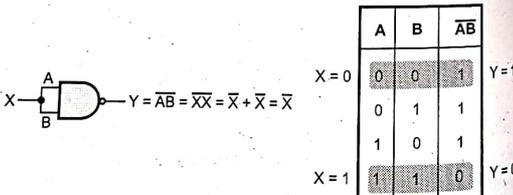


Fig. 4.7.14 NOT function using NAND gate

AND Function :

An AND function can be generated using only NAND gates. It is generated by simply inverting output of NAND gate; i.e. $\overline{\overline{AB}} = AB$. Fig. 4.7.15 shows the two input AND gate using NAND gates.

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

A	B	\overline{AB}	$\overline{\overline{AB}}$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 4.7.1 Truth table

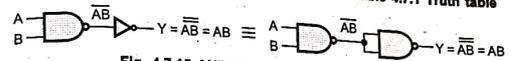


Fig. 4.7.15 AND function using NAND gates

OR Function :

OR function is generated using only NAND gates as follows : We know that Boolean expression for OR gate is

$$Y = A + B$$

$$= \overline{\overline{A} \cdot \overline{B}}$$

$$= \overline{\overline{A} \cdot \overline{B}}$$

[$\overline{\overline{A}} = A$]

DeMorgan's theorem 1

The above equation is implemented using only NAND gates as shown in the Fig. 4.7.16.

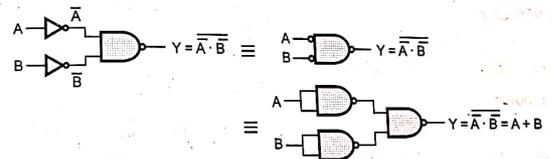


Fig. 4.7.16 OR function using only NAND gates

Note: Bubble at the input of NAND gate indicates inverted input.

A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	1

A	B	$\overline{A} \cdot \overline{B}$	$\overline{A \cdot B}$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Table 4.7.2 Truth table

NOR Function :

NOR function is generated using only NAND gates as follows : We know that Boolean expression for NOR gate is

$$Y = \overline{A+B} = \overline{A} \cdot \overline{B} = \overline{\overline{\overline{A} \cdot \overline{B}}}$$

DeMorgan's theorem 2
[$\overline{\overline{A}} = A$]

The above equation is implemented using only NAND gates, as shown in the Fig. 4.7.17.

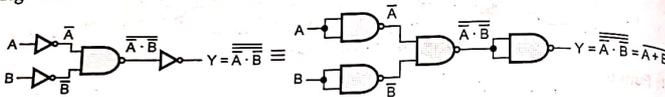


Fig. 4.7.17 NOR function using only NAND gates

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

A	B	$\overline{A \cdot B}$	$\overline{\overline{A \cdot B}}$	$\overline{\overline{\overline{A \cdot B}}}$
0	0	1	0	1
0	1	0	1	0
1	0	0	1	0
1	1	0	1	0

4.7.3.2 NOR Gate

- The NOR gate is also a universal gate, since it can be used to generate the NOT, AND, OR and NAND functions.

NOT Function :

An inverter can be made from a NOR gate by connecting all of the inputs together and creating, in effect, a single common input, as shown in Fig. 4.7.18.

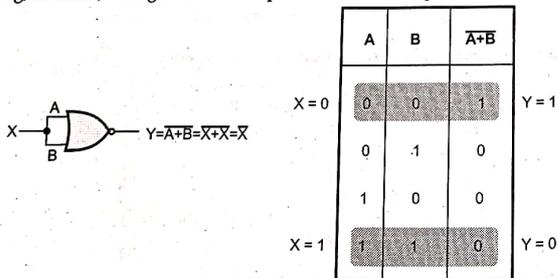


Fig. 4.7.18 NOT function using NOR gate

OR Function :

An OR function can be generated using only NOR gates. It can be generated by simply inverting output of NOR gate; i.e. $\overline{\overline{A+B}} = A+B$. Fig. 4.7.19 shows the two input OR gate using NOR gates.

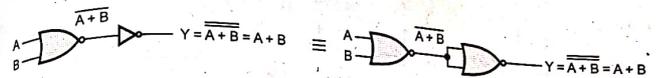


Fig. 4.7.19 OR function using NOR gates

A	B	$\overline{A+B}$	$\overline{\overline{A+B}}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Table 4.7.3 Truth table

AND Function :

AND function is generated using only NOR gates as follows : We know that Boolean expression for AND gate is

$$Y = A \cdot B = \overline{\overline{A \cdot B}} = \overline{\overline{A+B}}$$

DeMorgan's theorem 2
[$\overline{\overline{A}} = A$]

The above equation is implemented using only NOR gates as shown in the Fig. 4.7.20.

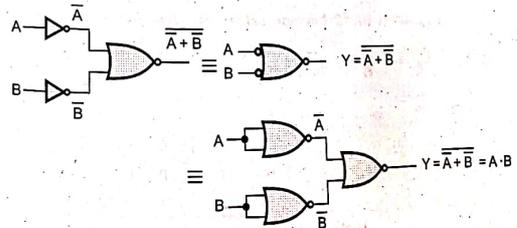


Fig. 4.7.20 AND function using NOR gates

Note Bubble at the input of NOR gate indicates inverted input.

A	B	$A \cdot B$	A	B	$\overline{A+B}$	$\overline{\overline{A+B}}$
0	0	0	0	0	1	0
0	1	0	0	1	1	0
1	0	0	1	0	1	0
1	1	1	1	1	0	1

Table 4.7.4 Truth table

NAND Function :

NAND function is generated using only NOR gates as follows : We know that Boolean expression for NAND gate is

$$\begin{aligned}
 Y &= \overline{A \cdot B} \\
 &= \overline{\overline{\overline{A+B}}} \\
 &= \overline{\overline{A+B}}
 \end{aligned}$$

DeMorgan's theorem 1
 $\overline{\overline{A}} = A$

The above equation is implemented using only NOR gates, as shown in the Fig. 4.7.21.

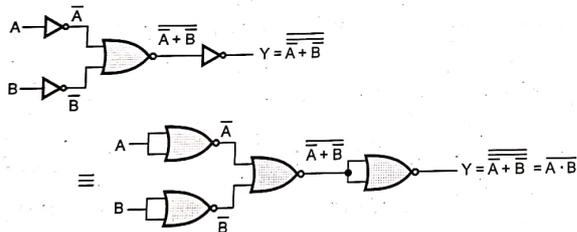


Fig. 4.7.21 NAND function using only NOR gates

A	B	$A \cdot B$	A	B	$\overline{A+B}$	$\overline{\overline{A+B}}$	$\overline{\overline{\overline{A+B}}}$
0	0	1	0	0	1	0	1
0	1	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	1	0	1	1	0	1	0

Table 4.7.5 Truth table

4.7.4 NAND-NAND Implementation

- The implementation of a Boolean function with NAND-NAND logic requires that the function be simplified in the sum of product form.
- The relationship between AND-OR logic and NAND-NAND logic is explained using following example.
- Consider the Boolean function : $Y = ABC + DE + F$.
- This Boolean function can be implemented using AND-OR logic, as shown in Fig. 4.7.22 (a).

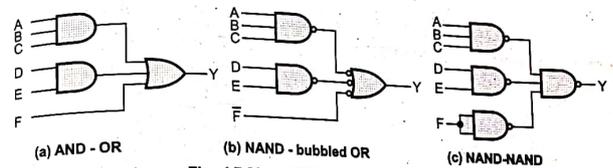


Fig. 4.7.22 NAND-NAND implementation

- Fig. 4.7.22 (b) shows the AND gates are replaced by NAND gates and the OR gate is replaced by a bubbled OR gate. The implementation shown in Fig. 4.7.22 (b) is equivalent to implementation shown in Fig. 4.7.22 (a), because two bubbled on the same line represent double inversion (complementation) which is equivalent to having no bubble on the line.
- In case of single variable, F, the complemented variable is again complemented by bubble to produce the normal value of F.
- In Fig. 4.7.22 (c), the output NAND gate is redrawn with the conventional symbol. The NAND gate with same inputs gives complemented result, therefore \overline{F} is replaced by NAND gate with F input to its both inputs. Thus all the three implementations of Boolean function are equivalent.

Rules for obtaining the NAND-NAND logic diagram

- Simplify the given Boolean function and express it in sum of product form (SOP form).
- Draw a NAND gate for each product term of the function that has two or more literals. The inputs to each NAND gate are the literals of the term. This constitutes a group of first level gates.
- If Boolean function includes any single literal or literals draw NAND gate for each single literal and connect corresponding literal as an input to the NAND gate.

4. Draw a single NAND gate in the second level, with inputs coming from outputs of first level gates.

Illustrative Examples

Example 4.7.10 Implement the following Boolean function with NAND-NAND logic

$$Y = AC + ABC + \bar{A}BC + AB + D$$

Solution : Step 1 : Simplify the given Boolean function.

$$Y = AC + ABC + \bar{A}BC + AB + D$$

$$= AC + BC(A + \bar{A}) + AB + D = AC + BC + AB + D$$

Step 2 : Implement using AND-OR logic.

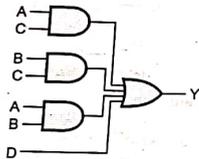


Fig. 4.7.23 (a)

Step 3 : Convert AND-OR logic to NAND-NAND logic.

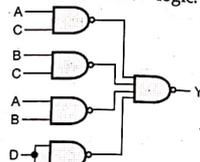


Fig. 4.7.23 (b)

Example 4.7.11 Implement the following Boolean function with NAND-NAND logic

$$F = \bar{A}\bar{B} + \bar{A}C + \bar{B}C$$

Solution :

Step 1 : Implement Boolean function with AND-OR logic.

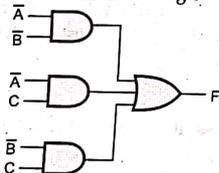


Fig. 4.7.24 (a)

Step 2 : Convert AND-OR logic to NAND-NAND logic.

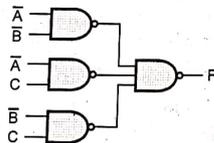


Fig. 4.7.24 (b)

Note It is possible to directly go to step 2 skipping step 1. Here, step 1 is included for clear understanding.

Example 4.7.12 Implement the following Boolean function with NAND-NAND logic.

$$F = (A, B, C) = \sum m(0, 1, 3, 5)$$

Solution : Step 1 : Simplify the given Boolean function.

	BC	00	01	11	10
A	0	1	1	1	0
	1	0	1	0	0

Fig. 4.7.25

$$F = \bar{A}\bar{B} + \bar{A}C + \bar{B}C$$

Step 2 : Implement Boolean function with AND-OR logic.

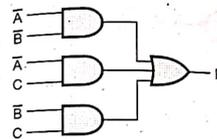


Fig. 4.7.26 (a)

Step 3 : Convert AND-OR logic to NAND-NAND logic.

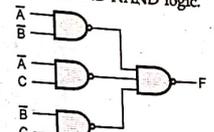


Fig. 4.7.26 (b)

Note It is possible to directly go to step 3 skipping step 2. Here, step 2 is included for clear understanding.

Example 4.7.13 Implement EX-OR gate using only NAND gates.

Solution : The Boolean expression for EX-OR gate is : $Y = \bar{A}\bar{B} + \bar{A}B$

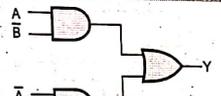


Fig. 4.7.27 (a)

We can implement AND-OR logic by using NAND-NAND logic as shown in Fig. 4.7.27 (b).

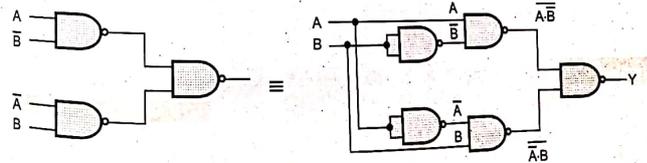


Fig. 4.7.27 (b)

Example 4.7.14 Implement EX-NOR gate using only NAND gates.

Solution : The Boolean expression for EX-NOR gate is $y = AB + \bar{A}\bar{B}$. We can implement AND-OR logic by using NAND-NAND logic as shown in Fig. 4.7.28.

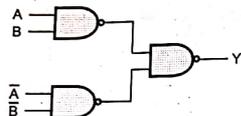


Fig. 4.7.28

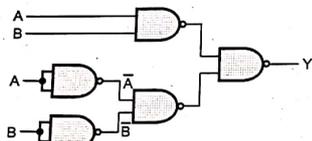
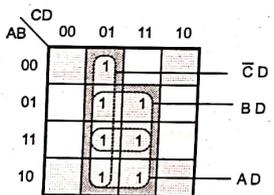


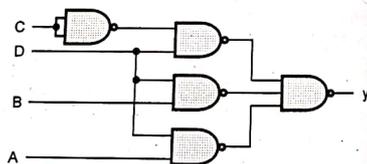
Fig. 4.7.28 (a)

Example 4.7.15 Minimize $y = \sum m(1, 5, 7, 9, 11, 13, 15)$ and realize using universal gates.

Solution :



$y = \bar{C}D + BD + AD$



Example 4.7.16 Draw the logic circuit for following function using only NAND gates :

$F = ABC + \bar{A}B + A\bar{C}D$

GTU : Dec.-13, Marks 3

Solution :

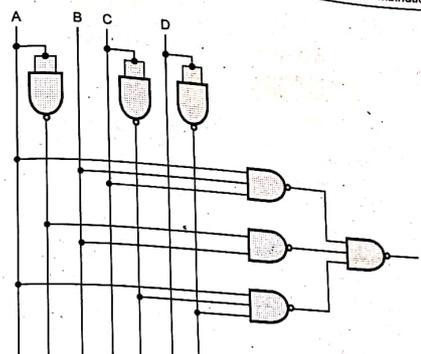
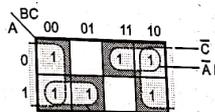


Fig. 4.7.29

Example 4.7.17 Reduce the expression $F = \sum m(0, 2, 3, 4, 5, 6)$ using K-map and implement using NAND gates only.

GTU : Summer-16, Marks 7

Solution :



$\therefore F = \bar{C} + A\bar{B} + \bar{A}B$

Fig. 4.7.30

We can implement AND-OR logic with NAND-NAND logic.

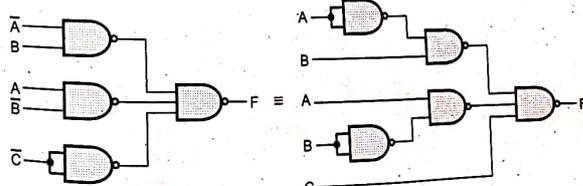


Fig. 4.7.31

Note : For C input two inversions get cancelled.

Examples for Practice

Example 4.7.18 : Simplify the following Boolean function using K-map and implement the same using only NAND gates :

$$F(A, B, C, D) = \overline{D} + \overline{A}BC + ABC + \overline{A}BCD$$

[Ans. : $Y = D \cdot (\overline{B} \cdot C) \cdot (\overline{A} \cdot \overline{C})$]

Example 4.7.19 : Minimize the following equation using K-map and realise it using NAND gates only :

$$Y = \sum m(4, 5, 8, 9, 11, 12, 13, 15)$$

[Ans. : $y = \overline{B}C + \overline{A}B + \overline{A}D$]

Example 4.7.20 : Minimize the given function using K-map and implement using NAND gates only.

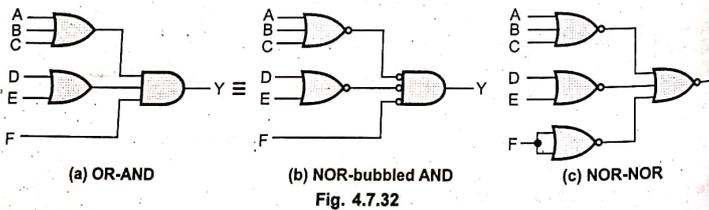
i) $F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5, 8, 14)$

ii) $F(A, B, C, D) = \sum m(0, 1, 2, 3, 6, 7, 13, 15)$

[Ans. : i) $\overline{A}B + CD$, ii) $\overline{A}B + \overline{A}C + ABD$]

4.7.5 NOR-NOR Implementation

- The NOR function is a dual of the NAND function. For this reason, the implementation procedures and rules for NOR-NOR logic are the duals of the corresponding procedures and rules developed for NAND-NAND logic.
- The implementation of a Boolean function with NOR-NOR logic requires that the function be simplified in the product of sum form.
- In product of sum form, we implement all sum terms using OR gates. This constitutes the first level.
- In the second level all sum terms are logically ANDed using AND gate. The relationship between OR-AND logic and NOR-NOR is explained using following example.
- Consider the Boolean function : $Y = (A + B + C)(D + E)F$
- This Boolean function can be implemented using OR-AND logic, as shown in the Fig. 4.7.32 (a).
- Fig. 4.7.32 (b) shows the OR gates are replaced by NOR gates and the AND gate is replaced by a bubbled AND gate. The implementation shown in Fig. 4.7.32 (c)



is equivalent to implementation shown in Fig. 4.7.32 (a), because two bubbled on the same line represent double inversion (complementation) which is equivalent to having no bubble on the line.

- In case of single variable, F, the complemented variable again complemented by bubble to produce the normal value of F.
- In Fig. 4.7.32 (c), the output NOR gate is redrawn with the conventional symbol. The NOR gate with same inputs gives complemented result, therefore, \overline{F} is replaced by NOR gate with F input to its both inputs. Thus all the three implementations of Boolean function are equivalent.

Rules for obtaining the NOR-NOR logic diagram

1. Simplify the given Boolean function and express it in product of sum form (POS form).
2. Draw a NOR gate for each sum term of the function that has two or more literals. The inputs to each NOR gate are the literals of the term. This constitute a group of first level gates.
3. If Boolean function includes any single literal or literals, draw NOR gate for each single literal and connect corresponding literal as an input to the NOR gate.
4. Draw a single NOR gate in the second level, with inputs coming from outputs of first level gates.

Illustrative Examples

Example 4.7.21 Implement the following Boolean function with NOR-NOR logic

$$Y = AC + BC + AB + D$$

Solution : Step 1 : Express Boolean function in POS form.

Using duality theorem we get,

$$\overline{Y} = (\overline{A} + \overline{C})(\overline{B} + \overline{C})(\overline{A} + \overline{B})\overline{D}$$

Step 2 : Implement Boolean function with OR-AND logic.

Step 3 : Convert OR-AND logic to NOR-NOR logic.

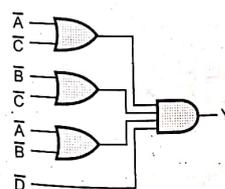


Fig. 4.7.33 (a)

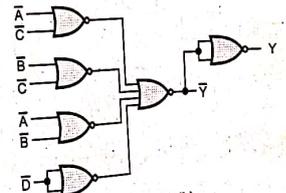


Fig. 4.7.33 (b)

Example 4.7.22 Implement the following Boolean function with NOR-NOR logic.
 $F = (A, B, C) = \Pi M (0, 2, 4, 5, 6)$

Solution : Step 1 : Simplify the given Boolean function:

$$F = (\bar{A} + B) C$$

	BC	00	01	11	10
A	0	0	0	0	0
	1	0	0	0	0

Fig. 4.7.34

Step 2 : Implement Boolean function with OR-AND logic.

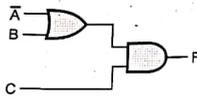


Fig. 4.7.35 (a)

Step 3 : Convert OR-AND logic to NOR-NOR logic.

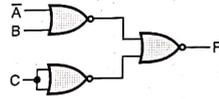


Fig. 4.7.35 (b)

Note It is possible to directly go to step 3 skipping step 2. Here, step 2 is included for clear understanding.

Example 4.7.23 Implement EX-NOR gate using only NOR gates.

Solution : The Boolean expression for EX-NOR gate is :

$$Y = AB + \bar{A}\bar{B} = \overline{AB + \bar{A}\bar{B}}$$

$$= \overline{AB} \cdot \overline{\bar{A}\bar{B}} = (\bar{A} + B) \cdot (A + \bar{B})$$

We can implement OR-AND logic by using NOR-NOR logic, as shown in Fig. 4.7.36 (b).

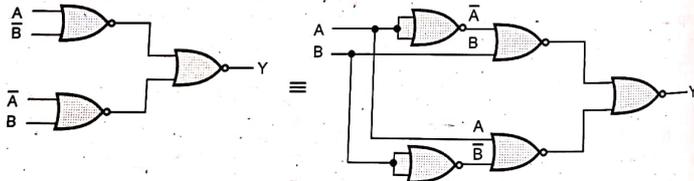


Fig. 4.7.36 (b)

Example 4.7.24 Implement EX-OR gate using only NOR gates.

Solution : Boolean expression of EX-OR gate $Y = A\bar{B} + \bar{A}B = A\bar{B} + \bar{A}B$

$$= \bar{A}\bar{B} \cdot \overline{\bar{A}\bar{B}}$$

$$= (\bar{A} + \bar{B}) (A + B)$$

Note We can implement OR-AND logic by NOR-NOR logic.

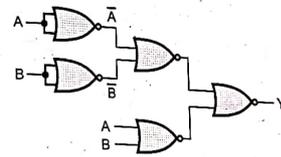
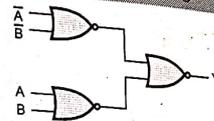


Fig. 4.7.37

Example 4.7.25 For the following function implement the logic circuit using i) Only NAND gates ii) Only NOR gates :

$$F(A, B, C, D) = \Sigma m (1, 3, 4, 6, 9, 11, 12, 14) + \Sigma d (2, 5, 8, 15)$$

Solution : i)

	CD	00	01	11	10	
AB	00		1	1	X	$\bar{B}D$
	01	1	X		1	$B\bar{D}$
	11	1		X	1	
	10	X	1	1		

$\therefore F = B\bar{D} + B\bar{D}$

Implementation using NAND gate

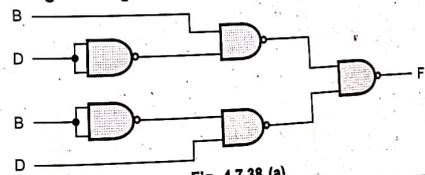


Fig. 4.7.38 (a)

ii) We have,

$$F = \overline{B}D + \overline{B}D$$

$$\overline{F} = \overline{\overline{B}D + \overline{B}D}$$

$$\overline{F} = \overline{\overline{B}D} \cdot \overline{\overline{B}D} = (\overline{B} + D) \cdot (\overline{B} + \overline{D})$$

Implementation using NOR gates

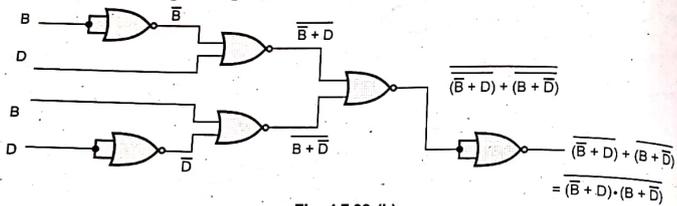


Fig. 4.7.38 (b)

Example 4.7.26 Draw the logic circuit for following function using only NOR gates :

$$F = ABC + AB(C+D)$$

GTU : Dec-13, Marks 4

Solution : $F = ABC + AB(C+D)$
 $= ABC + ABC + ABD$

Express the function F in POS form. Using duality theorem, we get,

$$\overline{F} = (\overline{A} + \overline{B} + C)(\overline{A} + \overline{B} + \overline{C})(\overline{A} + \overline{B} + \overline{D})$$

Logic diagram

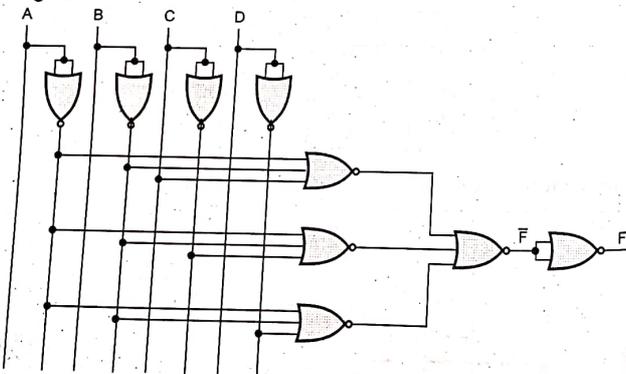


Fig. 4.7.39

Example 4.7.27 Minimize the following logic function

$$F(A, B, C, D) = \pi M(1, 2, 3, 8, 9, 10, 11, 14) d(7, 15)$$

Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only.

GTU : Winter-14, Marks 14

Solution :

K-map Simplification

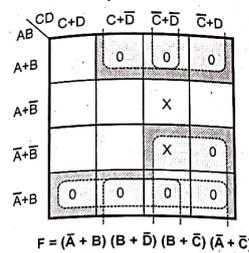


Fig. 4.7.40

Implementation

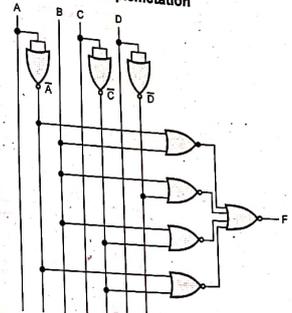
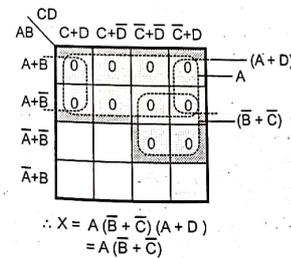


Fig. 4.7.41

Example 4.7.28 Reduce following Boolean function and then realize the reduced one using NOR gate only. $X = A(B' + C')(A + D)$

GTU : Winter-15, Marks 4

Solution : Implementation using NOR gates



Note : POS function can be implemented by NOR-NOR logic

Fig. 4.7.42

Example 4.7.29 Implement the following function with NAND and NOR Gate.

$$F(a, b, c) = \sum(0, 6)$$

GTU : Winter-18, Marks 4

Solution : $F(a,b,c) = \sum(0,6) = \bar{a}\bar{b}\bar{c} + abc$

Implementation using NAND gates

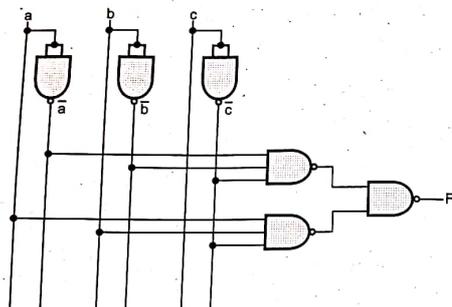


Fig. 4.7.43

Note : AND-OR logic can be directly implemented by NAND-NAND logic.

Implementation using NOR gates

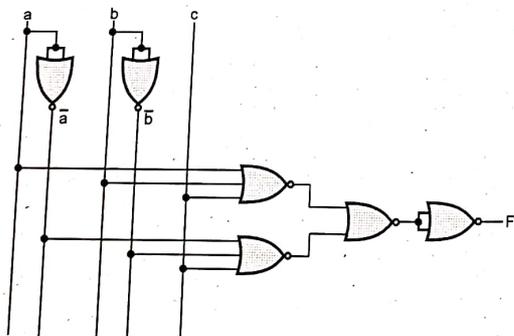


Fig. 4.7.44

$$F = \bar{a}\bar{b}\bar{c} + abc$$

$$= \overline{a\bar{b}c} + \overline{\bar{a}b\bar{c}}$$

$$= \overline{(a\bar{b}c)(\bar{a}b\bar{c})}$$

$$= (a+b+c)(\bar{a}+\bar{b}+\bar{c})$$

Example 4.7.30 Minimize the following logic function using K-maps and realize using NAND and NOR gates.

$$F(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$$

GTU : Winter-14, Marks 7

Solution :

$$F(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$$

$$= \pi M(0, 4, 6, 7, 10, 12, 14) + d(2, 13)$$

		CD	00	01	11	10
AB	00		1	1		X
	01		1			
	11		X	1		
	10		1	1	1	

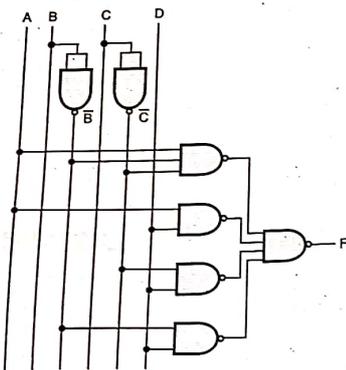
$$F = A\bar{B}\bar{C} + AD + \bar{C}D + \bar{B}D$$

		CD	C+D	C+D	$\bar{C}+\bar{D}$	$\bar{C}+D$
A+B	0					X
A+B	0			0	0	
$\bar{A}+\bar{B}$	0	X			0	
$\bar{A}+B$						0

$$F = (A + D)(\bar{B} + D)(\bar{C} + D)(A + B + \bar{C})$$

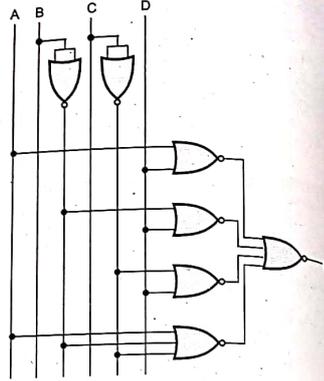
Fig. 4.7.45

Implementation using NAND-Gates



Note : SOP function can be implemented using NAND - NAND logic
Fig. 4.7.46

Implementation using NOR-Gates



Note : POS function can be implemented using NOR - NOR logic
Fig. 4.7.47

4.7.6 The EX-OR Gate in Function Realization

- In Ex-OR gate, the output goes high only if ODD number of inputs are high.
- Ex-OR gate can be used to implement the boolean functions presented by following truth tables and K-maps.
- Two-input Ex-OR gate :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Truth table

A \ B	0	1
0	0	1
1	1	0

K - map

$\therefore y = A\bar{B} + \bar{A}B$
 $y = A \oplus B$



Fig. 4.7.48

$Y = A\bar{B} + \bar{A}B$
 $Y = A \oplus B$

Three input Ex-OR gate :

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth table

$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$
 $= \bar{A}(B \oplus C) + A(B \oplus \bar{C})$
 $Y = A \oplus B \oplus C$

Four input Ex-OR gate :

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Table 4.7.6 Truth table

K-map simplification

$$\begin{aligned}
 Y &= \overline{A}\overline{B}(\overline{C}D + C\overline{D}) + \overline{A}B(\overline{C}D + CD) \\
 &+ AB(\overline{C}D + C\overline{D}) + A\overline{B}(\overline{C}D + CD) \\
 &= \overline{A}\overline{B}(C\oplus D) + \overline{A}B(\overline{C}\oplus D) \\
 &+ AB(C\oplus D) + A\overline{B}(\overline{C}\oplus D) \\
 &= (\overline{A}\overline{B} + A\overline{B})(C\oplus D) + (\overline{A}B + A\overline{B})(\overline{C}\oplus D) \\
 &= (\overline{A}\oplus B)(C\oplus D) + (A\oplus B)(\overline{C}\oplus D) \\
 &= (A\oplus B)\oplus(C\oplus D)
 \end{aligned}$$

		CD			
		00	01	11	10
AB	00	0	1	0	1
	01	1	0	1	0
	11	0	1	0	1
	10	1	0	1	0

$Y = (A\oplus B)\oplus(C\oplus D)$
Fig. 4.7.50 (a)

Logic diagram

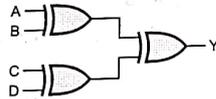


Fig. 4.7.50 (b)

Review Questions

1. Define the following term : Universal gate. **GTU : Dec-13, Mark 1**
2. Why NAND and NOR gates are called universal gates.
3. Using NOR gates draw inverters, AND and OR gates.
4. Discuss NAND gate as universal gate (implement NOT, AND, OR and NOR gate using NAND gate). **Summer-15, Marks 4**
5. Implement NOT, AND and OR gates using NAND gates only. **GTU : Summer-18, Marks 3**

4.8 Combinational Design Examples

GTU : Winter-14, 18

4.8.1 Introduction

- When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called **combinational logic circuit**.
 - In combinational logic circuit, the output variables are at all times dependent on the combination of input variables.
- Fig. 4.8.1 shows the block diagram of a combinational circuit.

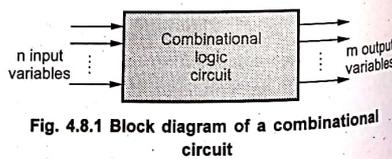


Fig. 4.8.1 Block diagram of a combinational circuit

4.8.2 Design Procedure

The design of combinational circuits starts from the outline of the problem statement and ends in a logic circuit diagram or a set of Boolean functions from which the logic diagram can be easily obtained. The design procedure of the combinational circuit involves following steps :

1. The problem definition.
2. The determination of number of available input variables and required output variables.
3. Assigning letter symbols to input and output variables.
4. The derivation of truth table indicating the relationships between input and output variables.
5. Obtain simplified Boolean expression for each output.
6. Obtain the logic diagram.

4.8.3 A Combinational Function Generator

- Here, the combinational circuit is represented by the relationship between its input and an output variable or variables. The following examples illustrate the procedure to design such combinational circuits.

Example 4.8.1 Design a combination logic circuit with three input variables that will produce a logic 1 output when more than one input variables are logic 1.

Solution :

Step 1 : Derive the truth table for given statement.

Given problem specifies that there are three input variables and one output variable. We assign A, B and C letter symbols to three input variables and assign Y letter symbol to one output variable. The relationship between input variables and output variable can be tabulated as shown in truth Table 4.8.1.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 4.8.1 Truth table

Step 2 : Obtain simplified Boolean expression.

Now we obtain the simplified Boolean expression for output variable Y using K-map simplification.

$Y = AC + BC + AB$

		BC			
		00	01	11	10
A	0	0	0	1	0
	1	0	1	1	1

Fig. 4.8.2 K-map simplification

Step 3 : Draw logic diagram.

In this chapter we are going to study various combinational circuits using above illustrated design method.

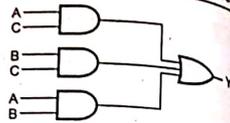


Fig. 4.8.3 Logic diagram

Example 4.8.2 Design a circuit that has one control line C and three data lines D_1, D_2, D_3 . When the control line is high, the circuit is to detect when one of the data lines has a 1 on it. No more than one data line will ever have a 1 on it. When the control line is low, the circuit will output a 0, regardless of what is on the data lines.

Solution : The truth table for the given problem is as shown below.

C	D_3	D_2	D_1	Output
0	x	x	x	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1

Table 4.8.2 Truth Table for given problem

$Y = CD_3 + CD_2 + CD_1$

K-map Simplification

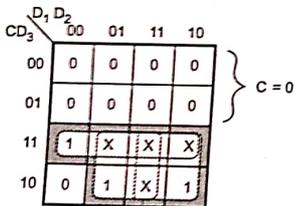


Fig. 4.8.4

Logic diagram

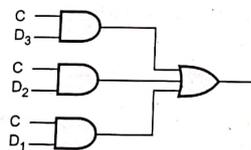


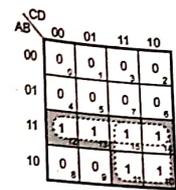
Fig. 4.8.5

Example 4.8.3 Design circuit to detect invalid BCD number and implement using NAND gate only.

Solution : Truth table

Dec	A	B	C	D	Output Y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

K-map Simplification



$Y = AB + AC$

Logic diagram

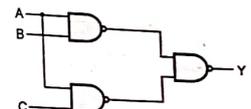


Fig. 4.8.6

AND-OR logic can be directly implemented by NAND-NAND logic.

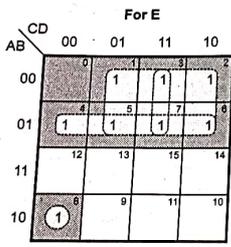
Example 4.8.4 Design a combinational circuit to produce the 2's complement of a 4-bit binary number as a input.

Solution :

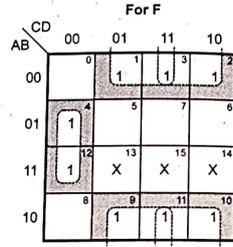
Input				2's complement output			
A	B	C	D	E	F	G	H
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0

0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

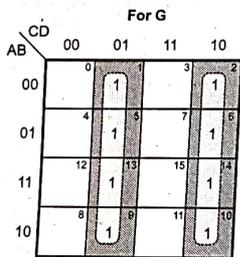
K-map simplification



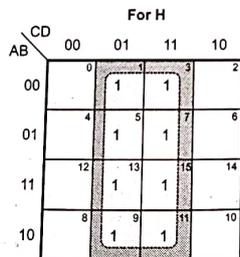
$E = ABC\bar{D} + \bar{A}B + \bar{A}D + \bar{A}C$



$F = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$



$G = \bar{C}D + C\bar{D}$



$H = D$

Logic diagram

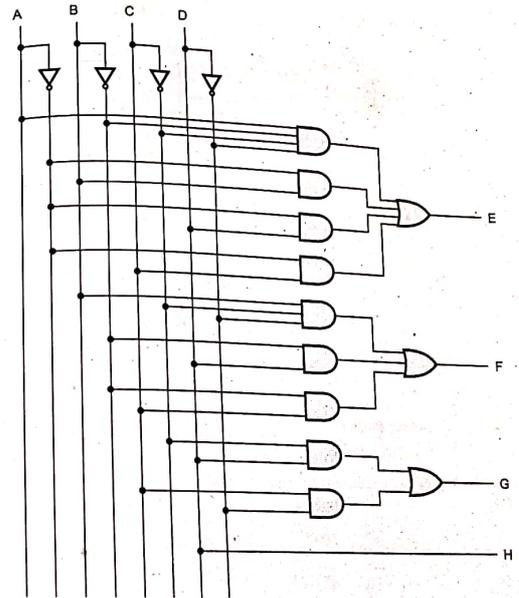


Fig. 4.8.7

Example 4.8.5 A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations
 A is False, B is True
 A is False, C is True
 A, B, C are False
 A, B, C are True
 i) Write the truth table for F. Use the convention True = 1 and False = 0.
 ii) Write the simplified expression for F in SOP form.
 iii) Write the simplified expression for F in POS form.
 iv) Draw logic circuit using minimum number of 2-input NAND gates.

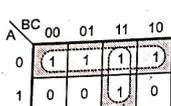
GTU : Winter-14, Marks 7

Solution :

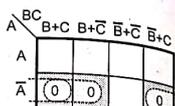
Truth table

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Truth table



$F = \bar{A} + BC$



$F = (\bar{A} + B)(\bar{A} + C)$

Fig. 4.8.8

- ii) Simplified SOP expression : $F = \bar{A} + BC$
- iii) Simplified POS expression : $F = (\bar{A} + B)(\bar{A} + C)$
- iv) Implementation used 2-input NAND gates

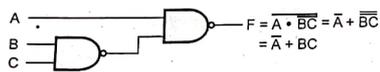


Fig. 4.8.9

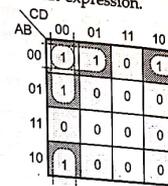
Example 4.8.6 Design a combinational logic circuit output is high only when majority of inputs (A, B, C, D) are low. GTU : Winter-18, Marks

Solution : Step 1 : Derive the truth table for given statement

Input				Output
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0

1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Step 2 : Obtain simplified Boolean expression.



$\therefore Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C}\bar{D}$

Fig. 4.8.10

Step 3 : Draw Logic diagram

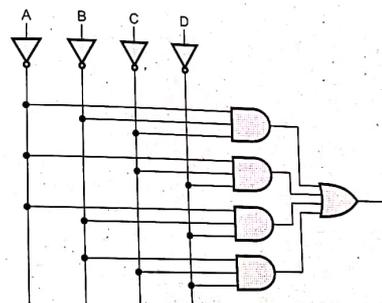


Fig. 4.8.11

Example for Practice

Example 4.8.7 : The inputs to a circuit are the 4 bits of the binary number $D_3D_2D_1D_0$. The circuit produces a 1 if and only if all of the following conditions hold.
 1) MSB is '1' or any of the other bits are a '0'.
 2) D_2 is a 1 or any of the other bits are a '0'.
 3) Any of the 4 bits are a 0.
 Obtain a minimal expression for the output. [Ans. : $Y = \bar{D}_1 + \bar{D}_0 + \bar{D}_3\bar{D}_2$]

Review Question

1. Explain the design procedure of combinational circuits.

4.9 Quine McCluskey Method of Function Realization

In simplification of Boolean expression we observed that the adjacent minterms can be reduced. These minterms are reduced because they differ by only one literal. For example, ABC and $A\bar{B}C$ can be reduced because only the B literal differs. The binary numbers equivalent to these minterms are 110 and 100. Note that the 2's place indicates precisely the same information that the literal represented, namely, that the B is the only literal that differs. Thus we can say that the minterms whose binary equivalent differ only in one place can be combined to reduce the minterms. This is the fundamental principle of the Quine McCluskey method.

Like in other methods, in this method minterms are listed to specify the given function. However, the minterms are written in their binary equivalents. These minterms are grouped according to number of 1s contained and separated by a horizontal line between each number of 1s category, as shown in the Table 4.9.1 (column (b)). This separation of minterms helps in searching the binary minterms that differ only in one place. Once the separation is over, each binary number is compared with every term in the next higher category and if they differ by only one position, a check mark is placed beside each of the two terms and then the term is copied in the second column with a '-' in the position that they differed.

For example, if the terms are 0000 and 0010 then the resultant term will be 00-0. This term, 00-0 is called an **implicant**, it implies the $AB\bar{D}$ could be a term in the final expression, covering minterms $\overline{A}BC\bar{D}$ and $\overline{A}B\bar{C}\bar{D}$. This process of comparison is repeated for every minterm. Once this process is completed the same process is applied to the new resultant terms which are placed in the Table 4.9.2 column (c). These cycles are continued until a single pass through a cycle yields no further elimination of literals. The remaining terms and all the terms that did not match during the process are called the **prime implicants**. Summing one or more prime implicant gives the simplified Boolean expression.

4.9.1 Algorithm for Generating Prime Implicants

1. List all minterms in the binary form.
2. Arrange the minterms according to number of 1s.
3. Compare each binary number with every term in the adjacent next higher category and if they differ only by one position, put a check mark and copy the term in the next column with '-' in the position that they differed.
4. Apply the same process described in step 3 for the resultant column and continue these cycles until a single pass through cycle yields no further elimination of literals.
5. List all prime implicants.

6. Select the minimum number of prime implicants which must cover all the minterms.
- See the following examples to illustrate the algorithm.

Illustrative Examples

Example 4.9.1 Simplify the following Boolean function by using a Quine McCluskey method. $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$.

Solution :

Step 1 : List all minterms in the binary form as shown in Table 4.9.1 (column (a)).

Step 2 : Arrange the minterms according to number of 1s, as shown in the Table 4.9.1 (column (b)).

Minterm	Binary representation	Minterm	Binary representation
m_0	0000	m_9	0000 ✓
m_2	0010	m_2	0010 ✓
m_3	0011	m_8	1000 ✓
m_6	0110	m_3	0011 ✓
m_7	0111	m_6	0110 ✓
m_8	1000	m_{10}	1010 ✓
m_{10}	1010	m_{12}	1100 ✓
m_{12}	1100	m_7	0111 ✓
m_{13}	1101	m_{13}	1101 ✓
	Column (a)		Column (b)

Table 4.9.1

Step 3 : Compare each binary number with every term in the adjacent next higher category and if they differ only by one position, put a check mark and copy the term in the next column with '-' in the position that they differed.

Step 4 : Apply the same process described in step 3 for the resultant column and continue these cycles until a single pass through cycle yields no further elimination of literals.

Minterms	Binary representation	Minterms	Binary representation
0, 2	00-0 ✓	0, 2, 8, 10	-0-0
0, 8	-000 ✓	2, 3, 6, 7	0-1-
2, 3	001- ✓		
2, 6	0-10 ✓		
2, 10	-010 ✓		
8, 10	10-0 ✓		
8, 12	1-00 ✓		
3, 7	0-11 ✓		

6, 7	0 1 1 - ✓
12, 13	1 1 0 -
Column (c)	Column (d)

Table 4.9.2

Step 5 : List the prime implicants.

Prime implicants	Binary representation
$A\bar{C}\bar{D}$	8, 12 1 - 0 0
ABC	12, 13 1 1 0 -
$\bar{B}\bar{D}$	0, 2, 8, 10 - 0 - 0
$\bar{A}C$	2, 3, 6, 7 0 - 1 -

Table 4.9.3

Step 6 : Select the minimum number of prime implicants which must cover all the minterms.

Table 4.9.4 shows prime implicant selection chart. Each prime implicant is represented in a row and each minterm in a column. Dots are placed in each row to show the composition of minterms that make the prime implicants. From this chart we have to select the minimum number of prime implicants which must cover all the minterms. The selection procedure is as follows.

Search for single dot columns and select the prime implicants corresponding to that dot by putting the check mark in front of it.

Prime implicants	m_0 (Col 1)	m_2 (Col 2)	m_3 (Col 3)	m_6 (Col 4)	m_7 (Col 5)	m_8 (Col 6)	m_{10} (Col 7)	m_{12} (Col 8)	m_{13} (Col 9)
$A\bar{C}\bar{D}$	8, 12					•		•	
ABC	12, 13 ✓							⊙	⊙
$\bar{B}\bar{D}$	0, 2, 8, 10 ✓	⊙	⊙			⊙	⊙		
$\bar{A}C$	2, 3, 6, 7 ✓	⊙	⊙	⊙	⊙				

Table 4.9.4 Prime implicant selection chart

Search for multiple dot columns one by one. If the corresponding minterm is already included in the final expression ignore the minterm and go to next multi-dot column ; otherwise include the corresponding prime implicant in the final expression.

In our case, column 1 (m_0) has single dot, so include corresponding prime implicant (0, 2, 8, 10). Column 3 (m_3) has single dot so include corresponding prime implicant (2, 3, 6, 7). Columns 4, 5 and 7 have single dots but the corresponding minterms are already included in the final expression.

Column 9 has single dot so include corresponding prime implicant (12, 13) in the final expression. Now search for multi-dot columns. Columns 2, 6 and 8 have multi-dots but their minterms are already included in the final expression. Therefore, the final expression is

$$F(A, B, C, D) = (110-) + (-0-0) + (0-1-)$$

$$= A\bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}C$$

Example 4.9.2 Minimize the expression using Quine McCluskey method.
 $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D}$

Solution :

Step 1 : List all minterms in the binary form, as shown in Table 4.9.5 (column (a)).

Step 2 : Arrange minterms according to categories of 1s, as shown in the Table 4.9.5 (column (b)).

Minterm	Binary representation	Minterm	Binary representation
m_4	0 1 0 0	m_2	0 0 1 0
m_5	0 1 0 1	m_4	0 1 0 0 ✓
m_{12}	1 1 0 0	m_5	0 1 0 1 ✓
m_{13}	1 1 0 1	m_9	1 0 0 1 ✓
m_9	1 0 0 1	m_{12}	1 1 0 0 ✓
m_2	0 0 1 0	m_{13}	1 1 0 1 ✓
Column (a)		Column (b)	

Table 4.9.5

Step 3 : Compare each binary number with every term in the next higher category and if they differ by only one position put a check mark and copy the term in the next column with '-' in the position that they differed.

Minterms	Binary representation	Minterms	Binary representation
4, 5	0 1 0 - ✓	4, 5, 12, 13	- 1 0 -
4, 12	- 1 0 0 ✓		
5, 13	- 1 0 1 ✓		
9, 13	1 - 0 1		
12, 13	1 1 0 - ✓		

Table 4.9.6

Step 4 : Apply the same process described in step 3 for the resultant column and continue this cycles until a single pass through cycle yields no further elimination of literals.

Step 5 : List the prime implicants.

Prime implicants		Binary representation
$\bar{A} \bar{B} C \bar{D}$	2	0 0 1 0
$A \bar{C} D$	9, 13	1 - 0 1
$B \bar{C}$	4, 5, 12, 13	- 1 0 -

Table 4.9.7

Step 6 : Select the minimum number of prime implicants which must cover all the minterms.

Prime implicants		m_2 (Col 1)	m_4 (Col 2)	m_5 (Col 3)	m_9 (Col 4)	m_{10} (Col 7)	m_{12} (Col 5)	m_{13} (Col 9)
$\bar{A} \bar{B} C \bar{D}$	2 ✓	⊙						
$A \bar{C} D$	9, 13 ✓				⊙		⊙	⊙
$B \bar{C}$	4, 5, 12, 13 ✓		⊙	⊙		⊙	⊙	⊙

Table 4.9.8 Prime implicant selection chart

The final expression is $Y = (0 0 1 0) + (1 - 0 1) + (- 1 0 -) = \bar{A} \bar{B} C \bar{D} + A \bar{C} D + B \bar{C}$

4.9.2 Quine McCluskey using Don't Care Terms

The same rules that applied to using don't care terms with Karnaugh map are appropriate for Quine McCluskey. Here, don't care terms are never included as prime implicants by themselves. Let us consider the following example.

Illustrative Example

Example 4.9.3 Simplify the following using tabulation methods.

$$Y(w, x, y, z) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11).$$

Solution : It is important to note that don't care conditions are used to find the prime implicant but it is not compulsory to include don't care terms in the final expression.

Step 1 : List all minterms in the binary form, as shown in the Table 4.9.9 (Column (a)).

Minterm	Binary representation	Minterm	Binary representation
m_1	0 0 0 1	m_1	0 0 0 1 ✓
m_2	0 0 1 0	m_2	0 0 1 0 ✓
m_3	0 0 1 1	m_4	0 1 0 0 ✓
m_5	0 1 0 1	m_5	0 1 0 1 ✓
m_9	1 0 0 1	m_8	1 0 0 0 ✓
m_{12}	1 1 0 0	m_3	0 0 1 1 ✓
m_{14}	1 1 1 0	m_5	0 1 0 1 ✓
m_{15}	1 1 1 1	m_9	1 0 0 1 ✓
dm_4	0 1 0 0	m_{12}	1 1 0 0 ✓
dm_8	1 0 0 0	m_{11}	1 0 1 1 ✓
dm_{11}	1 0 1 1	m_{14}	1 1 1 0 ✓
		m_{15}	1 1 1 1 ✓

Table 4.9.9

Step 2 : Arrange the minterms according to categories of 1s as shown in the Table 4.9.9 (Column (b)).

Step 3 : Compare each binary number with every term in the adjacent next higher category and if they differ by only one position put a check mark and copy the term in the next column with '-' in the position that they differed.

Step 4 : Apply the same process described in step 3 for the resultant column and continue these cycles until a single pass through cycle yields no further elimination of literals.

Minterms	Binary representation	Minterms	Binary representation
1, 3	0 0 - 1 ✓	1, 3, 9, 11	- 0 - 1
1, 5	0 - 0 1		
1, 9	- 0 0 1 ✓		
2, 3	0 0 1 -		
4, 5	0 1 0 -		

4, 12	-	1	0	0
8, 9	1	0	0	-
8, 12	1	-	0	0
3, 11	-	0	1	1
9, 11	1	0	-	1
12, 14	1	1	-	0
11, 15	1	-	1	1
14, 15	1	1	1	-

Table 4.9.10

Step 5 : List the prime implicants.

Step 6 : Select the minimum number of prime implicants which must cover all the minterms, except don't care minterms.

Only column 2 has single dot i.e. it is essential prime implicant and hence the prime implicant corresponding to it ($m_{2,3}$) is included in the final expression. Now search for multi-dot columns. Column 1 has multi-dot and the corresponding terms are not included in the final expression, so we can include either $m_{1,5}$ or $m_{1,3,9,11}$. Let us include prime implicant which has more minterms. Thus minterm 1, 3, 9, 11 is included. Now minterm for column 3 is already included and minterm for column 4 is don't care. Column 5 has a minterm which is not included yet, therefore prime implicant 1, 5 is included in the final expression. The minterms from column 6 and 8 are don't care and the minterm of column 7 (m_9) is already included in the final expression. Column 9 has minterm 12 which is not included yet.

Prime implicants	Binary representation
$\bar{A}\bar{C}D$	1, 5
$\bar{A}\bar{B}C$	2, 3
$\bar{A}B\bar{C}$	4, 5
$B\bar{C}\bar{D}$	4, 12
$A\bar{B}\bar{C}$	8, 9
$A\bar{C}\bar{D}$	8, 12
$AB\bar{D}$	12, 14
ACD	11, 15
ABC	14, 15
$\bar{B}D$	1, 3, 9, 11

Table 4.9.11

To include this term we have 3 options. We include prime implicant 12, 14 because with this inclusion we can also cover minterm 14 in the final expression. The minterm from the remaining column 11 (m_{15}) can be included in the final expression by including prime implicant 14, 15. Therefore, the final expression is

$$Y = (0 - 0 1) + (0 0 1 -) + (1 1 - 0) + (1 1 1 -) + (- 0 - 1)$$

$$= \bar{A}\bar{C}D + \bar{A}\bar{B}C + AB\bar{D} + ABC + \bar{B}D$$

Prime Implicants	m_1 (Col 1)	m_2 (Col 2)	m_3 (Col 3)	dm_4 (Col 4)	m_5 (Col 5)	dm_6 (Col 6)	m_7 (Col 7)	dm_{11} (Col 8)	m_{12} (Col 9)	m_{14} (Col 10)	m_{15} (Col 11)
$\bar{A}\bar{C}D$	1, 5 ✓	⊙									
$\bar{A}\bar{B}C$	2, 3 ✓	⊙	⊙								
$\bar{A}B\bar{C}$	4, 5			•	•						
$B\bar{C}\bar{D}$	4, 12			•							
$AB\bar{C}$	8, 9							•	•		
$A\bar{C}\bar{D}$	8, 12							•			
$AB\bar{D}$	12, 14 ✓									⊙	⊙
ACD	11, 15								•		•
ABC	14, 15 ✓										⊙
$\bar{B}D$	1, 3, 9, 11 ✓	⊙		⊙				⊙	⊙		

Table 4.9.12 Prime implicant selection table

4.9.3 Prime Implicant Table and Redundant Prime Implicants

We have seen that the prime implicant selection table displays pictorially the covering relationships between the prime implicants and the minterms of the function. It consists of an array of u columns and v rows, where u and v designate the number of minterms for which the function takes on the value 1 and the number of prime implicants, respectively. The entries of the i^{th} row in the chart consists of dots placed at its intersections with the columns, corresponding to minterms covered by the i^{th} prime implicant. For example, the prime implicant chart of $f(ABC) = \sum m(0, 1, 2, 5, 6, 7)$ is shown in Table 4.9.13 (b). It consists of 6 columns corresponding to the minterms of f and six rows which correspond to the prime implicant generated in Table 4.9.13 (a).

Minterm	Binary representation	Minterms	Binary representation
0	0 0 0	0, 1	0 0 -
1	0 0 1	0, 2	0 - 0
2	0 1 0	1, 5	- 0 1
5	1 0 1	2, 6	- 1 0
6	1 1 0	5, 7	1 - 1
7	1 1 1	6, 7	1 1 -

Table 4.9.13 (a)

The problem now is to select a minimal subset of prime implicants such that column contains at least one dot in the rows corresponding to the selected subset and the total number of literals in the prime implicants selected as small as possible. In our example, each column has two dots. It is a special case. When each column in the prime implicant selection chart has two or more dots, the chart is known as cyclic prime implicant table.

Since all columns have two dots, we have to proceed by trial and error. Both (0, 1) and (0, 2) cover column 0, so we will try (0, 1). After selecting row (0, 1) and columns 0, and 1 we examine column 2, which is covered by (0, 2) and (2, 6). The best choice is (2, 6) because it covers two of the remaining columns while (0, 2) covers only one of the remaining columns. After selecting row (2, 6) and columns 2 and 6, we see that (5, 7) covers the remaining columns and completes the solution. Therefore, one of the solution is $f = \bar{A}\bar{B} + B\bar{C} + AC$. The prime implicants which are not selected to get the solution [(0, 2), (1, 5), (6, 7)] are called redundant prime implicants.

Prime implicants		m ₀	m ₁	m ₂	m ₅	m ₆	m ₇
$\bar{A}\bar{B}$	0, 1 ✓	⊙	⊙				
$\bar{A}\bar{C}$	0, 2	•		•			
$\bar{B}C$	1, 5		•		•		
$B\bar{C}$	2, 6 ✓			⊙		⊙	
AC	5, 7 ✓				⊙		⊙
AB	6, 7					•	•

Table 4.9.13 (b) Prime implicant selection table

Example 4.9.4 Minimize the following function by tabular method.

$$f(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 9, 10, 13)$$

Solution :

Minterms	Binary representation	Minterm	Binary representation	Minterm	Binary representation
m ₀	0000	m ₀ ✓	0000	0, 2 ✓	00-0
m ₂	0010	m ₂ ✓	0010	0, 8 ✓	-000
m ₃	0011	m ₃ ✓	1000	2, 3 ✓	001-
m ₆	0110	m ₃ ✓	0011	2, 6 ✓	0-10
m ₇	0111	m ₆ ✓	0110	2, 10 ✓	-010
m ₈	1000	m ₆ ✓	1001	8, 9	100-

m ₉	1001	m ₁₀ ✓	1010	8, 10 ✓	10-0
m ₁₀	1010	m ₇ ✓	0111	3, 7 ✓	0-11
m ₁₃	1101	m ₁₃ ✓	1101	6, 7 ✓	011-
				9, 13	1-01

Minterm	Binary representation
0, 2, 8, 10	-0-0
2, 3, 6, 7	0-1-

Prime implicant selection chart

Prime implicants	m ₀	m ₂	m ₃	m ₆	m ₇	m ₈	m ₉	m ₁₀	m ₁₃
$\bar{B}\bar{D}$	0, 2, 8, 10 ✓	⊙	⊙			⊙		⊙	
$\bar{A}\bar{C}$	2, 3, 6, 7 ✓		⊙	⊙	⊙				
$A\bar{B}\bar{C}$	8, 9					•	•		
$A\bar{C}D$	9, 13 ✓							⊙	⊙

$$\therefore f(A, B, C, D) = \bar{B}\bar{D} + \bar{A}\bar{C} + A\bar{C}D$$

Example 4.9.5 Minimize the following function by tabular method :

$$f(w, x, y, z) = \sum m(1, 4, 8, 9, 13, 14, 15) + d(2, 3, 11, 12)$$

Solution :

Minterms	Binary representation	Minterms	Binary representation	Minterms	Binary representation
m ₁	0001	m ₁	0001	1, 5 ✓	00-1
dm ₂	0010	dm ₂	0010	1, 9 ✓	-001
dm ₃	0011	m ₄	0100	2, 3	001-
m ₄	0100	m ₈	1000	4, 12	-100
m ₈	1000	dm ₃	0011	8, 9 ✓	100-
m ₉	1001	m ₉	1001	8, 12 ✓	1-00
dm ₁₁	1011	dm ₁₂	1100	3, 11 ✓	-011
dm ₁₂	1100	dm ₁₁	1011	9, 11 ✓	10-1
m ₁₃	1101	m ₁₃	1101	9, 13 ✓	1-01
m ₁₄	1110	m ₁₄	1110	12, 13 ✓	110-
m ₁₅	1111	m ₁₅	1111	12, 14 ✓	11-0
				11, 15 ✓	1-11
				13, 15 ✓	11-1
				14, 15 ✓	111-

Minterms	Binary representation
1, 3, 9, 11	- 0 - 1
8, 9, 12, 13	1 - 0 -
9, 11, 13, 15	1 - - 1
12, 13, 14, 15	1 1 - -

Prime implicant selection chart

Prime implicants	m ₁	dm ₂	dm ₃	m ₄	m ₈	m ₉	dm ₁₁	dm ₁₂	m ₁₃	m ₁₄	m ₁₅
$\bar{x}z$	1, 3, 9, 11 ✓	⊙	⊙			⊙	⊙				
$w\bar{y}$	8, 9, 12, 13 ✓				⊙	⊙		⊙	⊙		
wz	9, 11, 13, 15					•	•		•		
wx	12, 13, 14, 15 ✓							⊙	⊙	⊙	⊙
$x\bar{y}\bar{z}$	4, 12 ✓			⊙				⊙			

$f(w, x, y, z) = \bar{B}D + A\bar{C} + AB + B\bar{C}\bar{D}$

4.9.4 Advantages and Disadvantages of Quine McCluskey Method

The Quine McCluskey method of simplification can be applied to any number of variables and is algorithmic in nature. The simplification process of Quine-McCluskey becomes lengthy and time consuming as number of variables increase; however the algorithm can be easily programmed to run on a computer to identify prime implicants and implicates of any function.

Examples for Practice

Example 4.9.6 : Find prime implicants for the Boolean expression by using Quine McCluskey method. $f(A,B,C,D) = \sum (1, 3, 6, 7, 8, 9, 10, 12, 14, 15) + d(11, 13)$
 Ans. : $F(A, B, C, D) = \bar{B}D + A + BC$

Example 4.9.7 : Give simplified logic equation using Quine-McCluskey method for the following Boolean function $f(A, B, C, D) = \sum m (0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$
 Ans. : $F(A, B, C, D) = \bar{A}\bar{B} + AC + AB$

Example 4.9.8 : Minimize the following using Quine-McCluskey method.
 $\sum m (0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$
 Ans. : $\bar{A}\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{E} + A\bar{B}\bar{C}\bar{E} + BCDE + A\bar{B}\bar{D}\bar{E}$

Example 4.9.9 : Minimize the given terms $\pi M (0, 1, 4, 11, 13, 15) + \pi d (5, 7, 8)$ using Quine-McCluskey methods and verify the results using K-map methods.
 Ans. : $f(A, B, C, D) = \bar{A}C + A\bar{D} + A\bar{B}\bar{C}$

Example 4.9.10 : Using QM method simplify the Boolean expression $f(x_1, x_2, x_3, x_4, x_5) = \sum (0, 1, 4, 5, 16, 17, 21, 25, 29)$
 Ans. : $f = \bar{x}_1\bar{x}_2\bar{x}_4 + \bar{x}_2x_3\bar{x}_4 + x_1\bar{x}_4x_5$

Example 4.9.11 : Minimize the following function using Quine Mc Cluskey method : $f(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 9, 10, 13)$

Example 4.9.12 : Minimize the following function by tabular method and implement the result using NAND gate only : $f(w, x, y, z) = \sum m (1, 4, 8, 9, 13, 14, 15) + d(2, 3, 11, 12)$

4.10 Multiplexers

GTU : Dec-13, Winter-14, 15, 18, Summer-15, 17, 18

In digital systems, many times it is necessary to select single data line from several data-input lines, and the data from the selected data line should be available on the output. The digital circuit which does this task is a multiplexer.

It is a digital switch. It allows digital information from several sources to be routed onto a single output line, as shown in the Fig. 4.10.1. The basic multiplexer has several data-input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Since multiplexer selects one of the input and routes it to output, it is also known as data selector. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

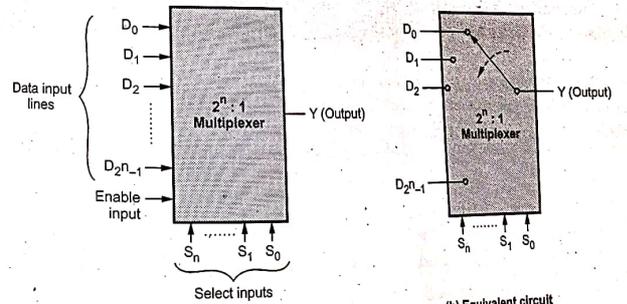


Fig. 4.10.1

4.10.1 2 : 1 Multiplexer

Fig. 4.10.2 (a) shows 2 : 1 multiplexer. D_0 is applied as an input to one AND gate and D_1 is applied as an input to another AND gate. Enable input is applied to both gates as one input. Selection line S is connected as second input to second AND gate. An inverted S is applied as second input to first AND gate. Outputs of both AND gates are applied as inputs to OR gate.

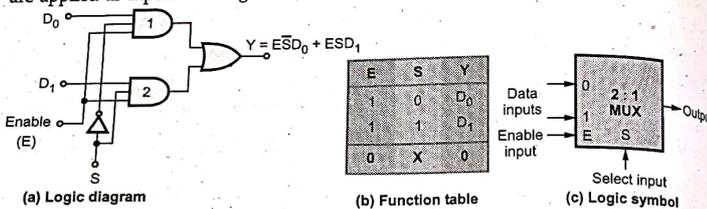


Fig. 4.10.2

Working

When $E = 0$, output is 0, i.e. $Y = 0$ irrespective of any input condition. When $E = 1$ the circuit works as follows :

When $S = 0$, the inverted S , that is 1 gets applied as second input to first AND gate. Since S is applied directly as input to second AND gate; its output goes zero irrespective of first input. Since the second input of first AND gate is 1, its output is equal to its first input, that is D_0 . Hence $Y = D_0$. Hence $Y = D_0$.

Exactly opposite is the case when $S = 1$. In this case, second AND gate output is equal to its first input D_1 and first AND gate output is 0. Hence $Y = D_1$. Both these cases are summarized in truth table shown in Fig. 4.10.2 (b).

Deriving realization expression

The Table 4.10.1 shows the truth table for 2 : 1 multiplexer. From the truth table it is clear that $Y = 1$ when $E\bar{S}D_0 = 1$ or $ES D_1 = 1$ as indicated by shaded rows.

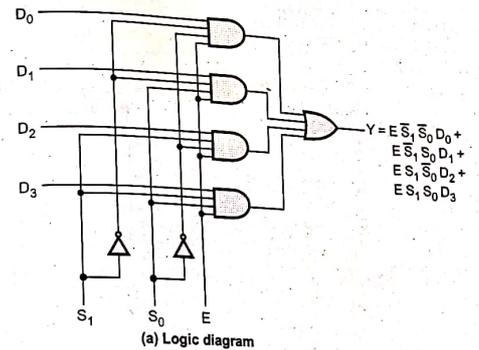
Enable (E)	Select (S)	D_1	D_0	Output Y
1	0	X	0	0
1	0	X	1	1
1	1	0	X	0
1	1	1	X	1
0	X	X	X	0

Table 4.10.1 Truth table for 2 : 1 multiplexer

$Y = E\bar{S}D_0 + ES D_1$

4.10.2 4 : 1 Multiplexer

Fig. 4.10.3 (a) shows 4-to-1 line multiplexer. Each of the four lines, D_0 to D_3 , is applied to one input of an AND gate. Selection lines are decoded to select a particular AND gate.



(a) Logic diagram

E	S_1	S_0	Y
1	0	0	D_0
1	0	1	D_1
1	1	0	D_2
1	1	1	D_3
0	X	X	0

(b) Function table

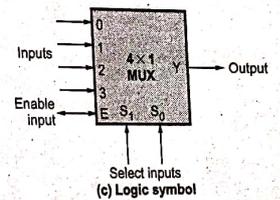


Fig. 4.10.3 4 to 1 line multiplexer

For example, when $S_1S_0 = 01$, the AND gate associated with data input D_1 has two of its inputs equal to 1 and the third input connected to D_1 . The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0. The OR gate output is now equal to the value of D_1 , thus we can say data bit D_1 is routed to the output when $S_1S_0 = 01$.

4.10.3 8 : 1 Multiplexer

Fig. 4.10.4 shows 8 : 1 multiplexer.

There are eight input lines one output line and three select lines. As shown in the function table, the selection of a particular input line is controlled by three selection lines.

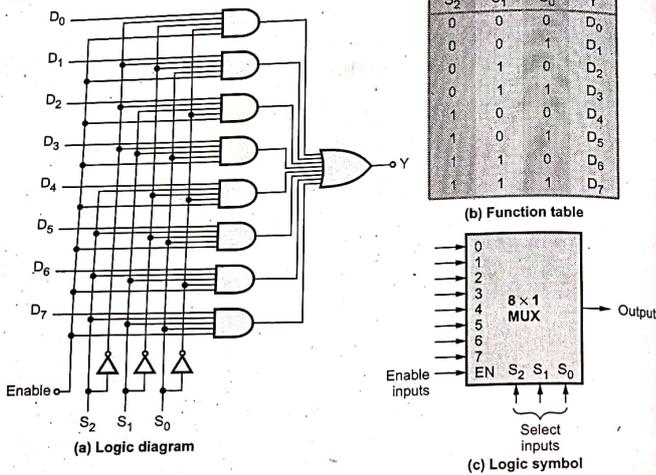


Fig. 4.10.4 8 : 1 Multiplexer

4.10.4 Quadruple 2 to 1 Multiplexer

In some cases, two or more multiplexers are enclosed within one IC package, as shown in the Fig. 4.10.5. The Fig. 4.10.5 shows quadruple 2-to-1 line multiplexer, i.e. four multiplexers, each capable of selecting one of two input lines. Output Y_1 can be selected to be equal to either A_1 or B_1 . Similarly output Y_2 may have the value of A_2 or B_2 , and so on. The selection line S selects one of two lines in all four multiplexers.

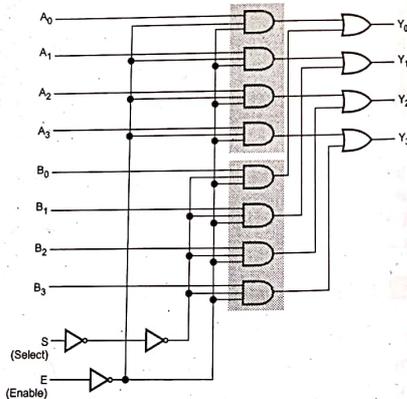


Fig. 4.10.5 Quadruple 2-to-1 line multiplexer

The control input E enables the multiplexers in the 0 state and disables them in the 1 state. When $E = 1$, outputs have all 0's, regardless of the value of S.

Function Table

E	S	Output Y
1	X	All 0s
0	0	Select A
0	1	Select B

4.10.5 The 74XX151 Multiplexer

The 74XX151 is a 8-to-1 multiplexer. It has eight inputs. It provides two outputs, one is active high, the other is active low. The Fig. 4.10.6 shows the logic symbol for 74XX151. As shown in the logic symbol, there are three select inputs C, B and A which select one of the eight inputs. The 74XX151 is provided with active low enable input.

The Table 4.10.2 shows the truth table for 74XX151. In this truth table for each input combinations output is not specified in 1s and 0s. Because, we know that, multiplexer is a data switch, it does not generate any data of its own, but it simply passes external input data from the selected input to the output. Therefore, the two output column represent data by D_n and \overline{D}_n .

Input			Outputs		
Select	Enable		Y	\overline{Y}	
C	B	A	EN		
x	x	x	1	0	1
0	0	0	0	D_0	\overline{D}_0
0	0	1	0	D_1	\overline{D}_1
0	1	0	0	D_2	\overline{D}_2
0	1	1	0	D_3	\overline{D}_3
1	0	0	0	D_4	\overline{D}_4
1	0	1	0	D_5	\overline{D}_5
1	1	0	0	D_6	\overline{D}_6
1	1	1	0	D_7	\overline{D}_7

Table 4.10.2 Truth table for 74XX151, 8 to 1 multiplexer

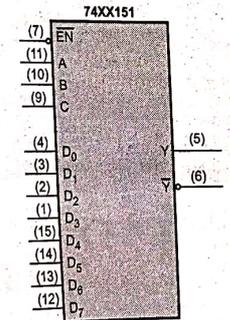


Fig. 4.10.6 Logic symbol for 74XX151, 8 to 1 multiplexer

4.10.6 The 74XX153 Dual 4 to 1 Multiplexer

The 74XX153 is a dual 4-to-1 multiplexer. Fig. 4.10.7 shows the logic symbol for 74XX153. It contains two identical and independent 4-to-1 multiplexers. Each multiplexer has separate enable inputs. The Table 4.10.3 shows the truth table for 74XX153.

Inputs				Outputs	
1EN	2EN	B	A	1Y	2Y
0	0	0	0	1D ₀	2D ₀
0	0	0	1	1D ₁	2D ₁
0	0	1	0	1D ₂	2D ₂
0	0	1	1	1D ₃	2D ₃
0	1	0	0	1D ₀	0
0	1	0	1	1D ₁	0
0	1	1	0	1D ₂	0
0	1	1	1	1D ₃	0
1	0	0	0	0	2D ₀
1	0	0	1	0	2D ₁
1	0	1	0	0	2D ₂
1	0	1	1	0	2D ₃
1	1	x	x	0	0

Table 4.10.3 Truth table for 74XX153, dual 4-to-1 multiplexer

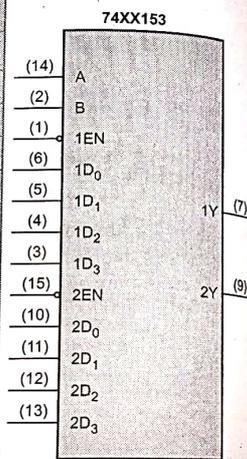


Fig. 4.10.7 Logic symbol for 74XX153

4.10.7 Expanding Multiplexers

It is possible to expand range of inputs for multiplexer beyond the available range by interconnecting several multiplexers in cascade. The circuit with two or more multiplexers connected to obtain the multiplexer with more number of inputs is known as multiplexer tree.

Illustrative Examples

Example 4.10.1 Design 16 : 1 multiplexer using 8 : 1 multiplexer.

Solution :

- Step 1 : Connect the select lines (S_2, S_1 and S_0) of two multiplexers in parallel.
- Step 2 : Connect most significant select line (S_3) such that when $S_3 = 0$, MUX 1 is enabled and when $S_3 = 1$, MUX 2 is enabled.
- Step 3 : Logically OR the outputs of two multiplexers to obtain the final output Y.

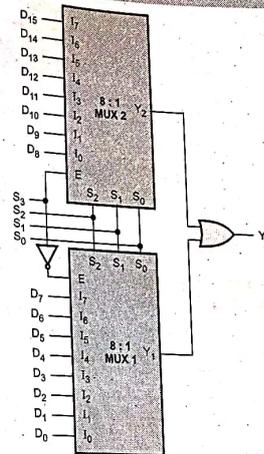


Fig. 4.10.8 16 : 1 multiplexer using two 8 : 1 multiplexers

Example 4.10.2 Design 16 : 1 multiplexer using 4 : 1 multiplexers.

Solution : Since there are 16-inputs for the multiplexers we require four 4 : 1 multiplexers to satisfy input needs. The four outputs of 4 : 1 multiplexers are again multiplexed by 4 : 1 multiplexer to generate final output.

- Step 1 : Connect the select lines (S_1 and S_0) of four multiplexers in parallel.
- Step 2 : Connect the most significant select lines (S_3 and S_2) to the MUX 5.
- Step 3 : Connect the outputs Y_0, Y_1, Y_2 and Y_4 of four multiplexers as data inputs for the MUX 5, as shown in the Fig. 4.10.2.

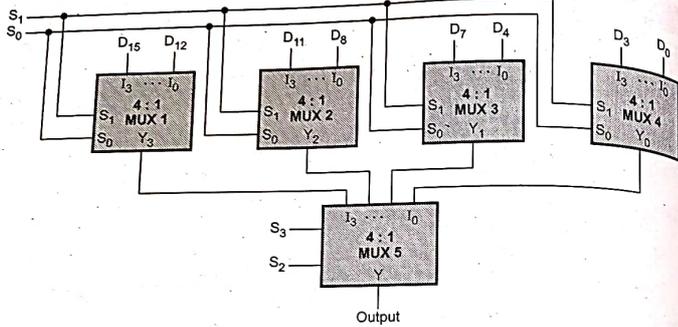


Fig. 4.10.9

Examples for Practice

Example 4.10.3 Draw the block diagram of a 4 : 1 multiplexer using 2 : 1 MUX.

Example 4.10.4 Design 32 : 1 MUX using 8 : 1 MUX.

Example 4.10.5 Design 14 : 1 mux using 4 : 1 mux (with enable inputs). Explain the truth table of your circuit in short.

Example 4.10.6 Design 28 : 1 mux using 8 : 1 mux (with enable inputs). Explain truth table of your design in short. [Hint : You can use separate mux for enable of respective IC's]

4.10.8 Implementation of Combinational Logic using MUX

A multiplexer consists of a set of AND gates whose outputs are connected to single OR gate. Because of this construction any Boolean function in a SOP form can be easily realized using multiplexer. Each AND gate in the multiplexer represents a minterm. In 8 to 1 multiplexer, there are 3 select inputs and 23 minterms. By connecting the function variables directly to the select inputs, a multiplexer can be made to select the AND gate that corresponds to the minterm in the function. If a minterm exists in a function, we have to connect the AND gate data input to logic 1; otherwise we have to connect it to logic 0. This is illustrated in the following example.

Illustrative Examples

Example 4.10.7 Implement the given function using multiplexer.

$$F(x, y, z) = \sum(0, 2, 6, 7).$$

Solution :

- Step 1 :** Select the multiplexer. Here, Boolean expression has 3 variables, thus we require $2^3 = 8 : 1$ multiplexer.
- Step 2 :** Connect inputs corresponds to the present minterms to logic 1.
- Step 3 :** Connect remaining inputs to logic 0.
- Step 4 :** Connect input variables to select lines of MUX.

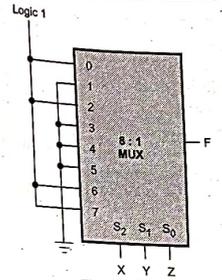


Fig. 4.10.10

Example 4.10.8 Implement the Boolean function represented by the given truth table using multiplexer.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Solution :

- Step 1 :** Select the multiplexer. Here, there are three input variables, thus we require $2^3 = 8 : 1$ multiplexer.
- Step 2 :** Find the minterm expression.
Minterm expression for given truth table is $\sum m(1, 2, 5, 7)$.
- Step 3 :** Connect inputs corresponds to the present minterms to logic 1.

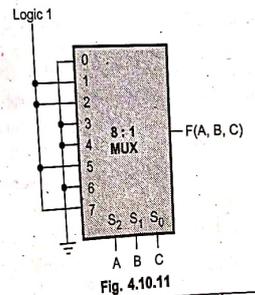


Fig. 4.10.11

Step 4 : Connect remaining inputs to logic 0.

Step 5 : Connect input variables to select lines of MUX.

In the above example, we have seen the method for implementing Boolean function of 3 variables with $2^3(8)$ -to-1 multiplexer. Similarly, we can implement any Boolean function of n variables with 2^n -to-1 multiplexer. However, it is possible to do better than this. If we have Boolean function of $n + 1$ variables, we take n of these variables and connect them to the selection lines of a multiplexer. The remaining single variable of the function is used for the inputs of the multiplexer. In this way we can implement any Boolean function of n variables with 2^{n-1} -to-1 multiplexer. Let us see some examples.

Example 4.10.9 Implement the following Boolean function using 4 : 1 multiplexer.

$$F(A, B, C) = \sum m(1, 3, 5, 6)$$

Solution :

Step 1 : Connect least significant variables as a select inputs of multiplexer. Here, connect C to S_0 and B to S_1 .

Step 2 : Derive inputs for multiplexer using implementation table.

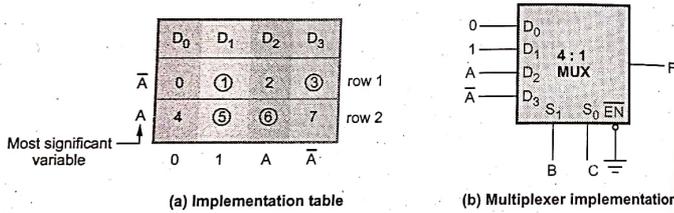


Fig. 4.10.12

As shown in the Fig. 4.10.12 (a) the implementation table is nothing but the list of the inputs of the multiplexer and under them list of all the minterms in two rows. The first row lists all those minterms where A is complemented, and the second row lists all the minterms with A uncomplemented. The minterms given in the function are circled and then each column is inspected separately as follows :

- If the two minterms in a column are not circled, 0 is applied to the corresponding multiplexer input (see column 0).
- If the two minterms in a column are circled, 1 is applied to the corresponding multiplexer input (see column 1).
- If the minterm in the second row is circled and minterm in the first row is not circled, A is applied to the corresponding multiplexer input (see column 2).

• If the minterm in the first row is circled and minterm in the second row is not circled, A is applied to the corresponding multiplexer input (see column 3).

Example 4.10.10 Implement the following Boolean function using 8 : 1 multiplexer

$$F(A, B, C, D) = A \bar{B} \bar{D} + A C D + \bar{B} C D + \bar{A} \bar{C} D$$

Solution :

Step 1 : Express Boolean function in the minterm form.

The given Boolean expression is not in standard SOP form. Let us first convert this in standard SOP form

$$\begin{aligned} F(A, B, C, D) &= \bar{A} \bar{B} \bar{D} (C + \bar{C}) + A C D (B + \bar{B}) + \bar{B} C D (A + \bar{A}) + \bar{A} \bar{C} D (B + \bar{B}) \\ &= \bar{A} \bar{B} \bar{C} \bar{D} + \bar{A} \bar{B} C \bar{D} + A B C D + A \bar{B} C D \\ &\quad + A \bar{B} \bar{C} D + \bar{A} B C D + \bar{A} B \bar{C} D + \bar{A} \bar{B} \bar{C} D \\ &= \bar{A} \bar{B} \bar{C} \bar{D} + \bar{A} \bar{B} C \bar{D} + A B C D + A \bar{B} C D + \bar{A} B C D + \bar{A} \bar{B} \bar{C} D \\ &= \sum m(6, 4, 15, 11, 3, 5, 1) \\ &= \sum m(1, 3, 4, 5, 6, 11, 15) \end{aligned}$$

Step 2 : Implement it using implementation table.

From the Boolean function in the minterm form can be implemented using 8 : 1 multiplexer as follows :

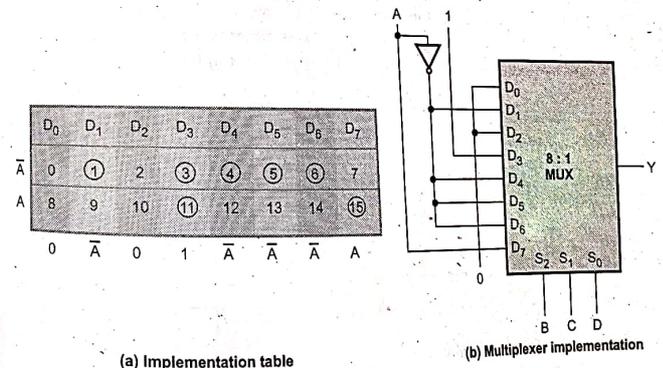
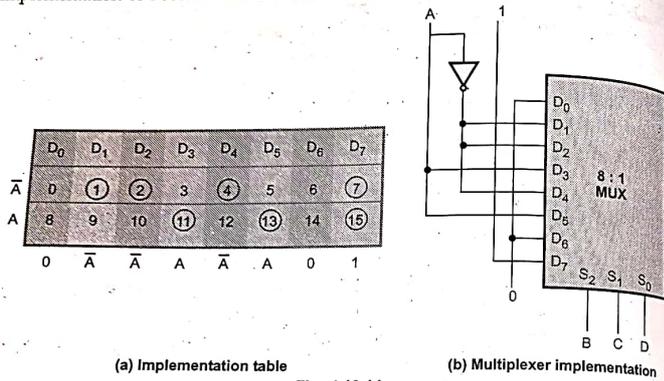


Fig. 4.10.13

Example 4.10.11 Implement the following Boolean function with 8 : 1 multiplexer

$$F(A, B, C, D) = \pi M(0, 3, 5, 6, 8, 9, 10, 12, 14)$$

Solution : Here, instead of minterms, maxterms are specified. Thus, we have to circle maxterms which are not included in the Boolean function. Fig. 4.10.14 shows the implementation of Boolean function with 8 : 1 multiplexer.



(a) Implementation table

(b) Multiplexer implementation

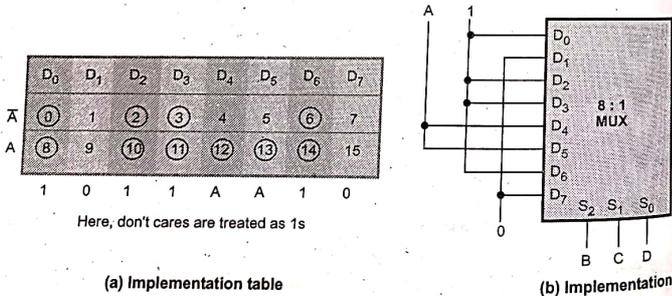
Fig. 4.10.14

Example 4.10.12 Implement the following Boolean function with 8 : 1 multiplexer.

$$F(A, B, C, D) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$$

Solution : In the given Boolean function three don't care conditions are also specified. We know that don't care conditions can be treated as either 0s or 1s. Fig. 4.10.15 shows the implementation of given Boolean function using 8 : 1 multiplexer.

In this example, by taking don't care conditions 8 and 14 as 1s we have eliminated \bar{A} term and hence the inverter.



Here, don't cares are treated as 1s

(a) Implementation table

(b) Implementation

Fig. 4.10.15

Examples for Practice

Example 4.10.13 Implement the following expression using 8 : 1 multiplexer :
 $f(A, B, C, D) = \sum m(2, 4, 6, 7, 9, 10, 11, 12, 15)$

Example 4.10.14 Implement Boolean function $f = AB + \bar{C}D + \bar{A}BC$ using 8 : 1 multiplexer.

4.10.9 Implementation of Logic Function using IC 74153

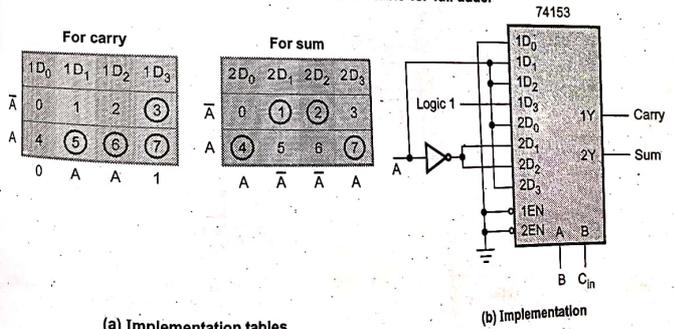
The 74XX153 is a dual 4 to 1 multiplexer. We have already seen how to implement combinational circuits using multiplexers in section 4.10.8. Let us see some examples of logic function implementation using IC 74153.

Example 4.10.15 Implement full adder using IC 74153.

Solution : The Table 4.10.4 shows the truth table for full adder.

Inputs			Outputs	
A	B	C _{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 4.10.4 Truth table for full-adder



(a) Implementation tables

(b) Implementation

Fig. 4.10.16

Since 74153 is a dual 4 : 1 multiplexer, we can use one 4 : 1 multiplexer to implement carry function and other 4 : 1 multiplexer to implement sum function.

Example 4.10.16 Implement full subtractor using IC 74153.

Solution : The Table 4.10.5 shows the truth table for full subtractor.

Inputs				Outputs	
A	B	B _{in}	D	B _{out}	
0	0	0	0	0	
0	0	1	1	1	
0	1	0	1	1	
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	1	1	

Table 4.10.5 Truth table for full-subtractor

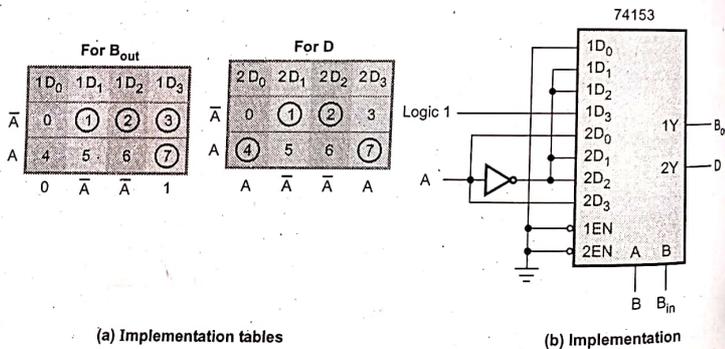


Fig. 4.10.17

Since 74153 is a dual 4 : 1 multiplexer, we can use one 4 : 1 multiplexer to implement D and other 4 : 1 multiplexer to implement B_{out}.

Example 4.10.17 Design a 8 to 1 multiplexer by using the four variable function given by $F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$

Solution :

Implementation table

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	1	2	3	4	5	6	7
\bar{A}	A	10	11	12	13	14	15
1	1	0	\bar{A}	\bar{A}	0	0	A

Fig. 4.10.18

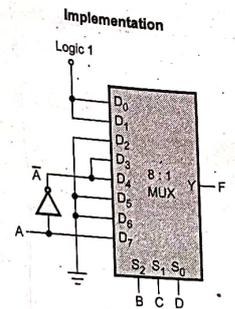


Fig. 4.10.19

Example 4.10.18 Implement the given function using 8 × 1 Multiplexer

$$F(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 8, 9, 11, 14)$$

GTU : Summer-15, Marks 7

Solution : Implementation Table

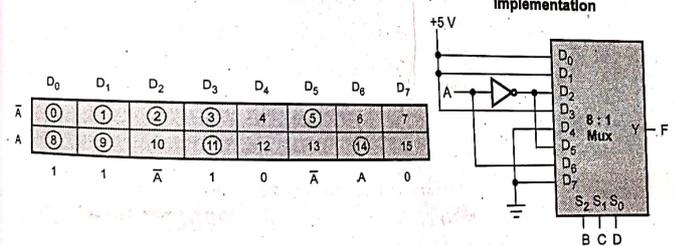


Fig. 4.10.20

Fig. 4.10.21

Example 4.10.19 Implement following logic function using 8 × 1 MUX.

$$F = \sum m(0, 1, 3, 5, 7, 11, 13, 14, 15)$$

GTU : Winter-15, Marks 7

Solution : Implementation table

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
\bar{A}	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	\bar{A}	\bar{A}	0	1	0	1	A	1

Fig. 4.10.22

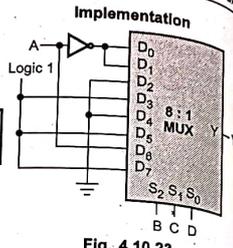


Fig. 4.10.23

Example 4.10.20 Implement following Boolean function using 8 : 1 multiplexer.

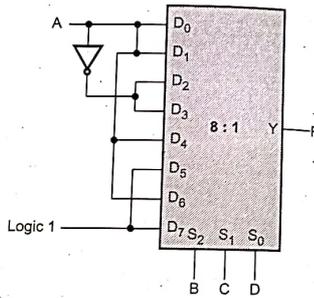
$$F(A, B, C, D) = \sum(2, 3, 5, 7, 8, 9, 12, 13, 14, 15)$$

GTU : Summer-17, Marks 7

Solution : Implementation Table

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
\bar{A}	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	A	A	\bar{A}	\bar{A}	A	1	A	1

(a) Implementation table



(b) Implementation

Fig. 4.10.24

Example 4.10.21 Implement the following Boolean functions with a multiplexer.

$$F(w, x, y, z) = \sum(1, 3, 5, 6, 11, 14, 15)$$

GTU : Winter-18, Marks 7

Solution : Implementation using Multiplexer

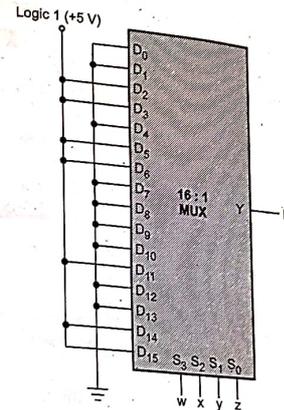


Fig. 4.10.25

4.10.10 Applications of Multiplexer

1. They are used as a data selector to select one out of many data inputs.
2. They can be used to implement combinational logic circuit.
3. They are used in time multiplexing systems.
4. They are used in frequency multiplexing systems.
5. They are used in A/D and D/A converter.
6. They are used in data acquisition systems.

4.10.11 Multiplexer ICs

IC number	Function
74150	16 : 1 multiplexer
74151	8 : 1 multiplexer
74153	Dual 4 : 1 multiplexer
74157	Quad 2-input multiplexer

Table 4.10.6 Multiplexer ICs

Review Questions

1. Draw logic circuit of 4 : 1 MUX. GTU : Summer-18, Marks 3
2. What is multiplexer ? GTU : Dec.-13, Marks 2
3. Explain the working of 8 : 1 multiplexer.
4. Obtain an 8 : 1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines.
5. Design an 8 : 1 multiplexer using two 4 : 1 multiplexers. Explain with the help of the truth table. Implement the function $f(A, B, C) = \sum m(1, 3, 7)$ using the same.
6. Realize the expression $Y(A, B, C, D) = \sum (15, 7, 4, 6, 8, 9, 12, 14)$ using an 8:1 MUX. GTU : Summer-18, Marks 7

4.11 Demultiplexers

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

The Fig. 4.11.1 shows the block diagram of a demultiplexer. It has one input data line, 2^n output lines, n select lines and one enable input.

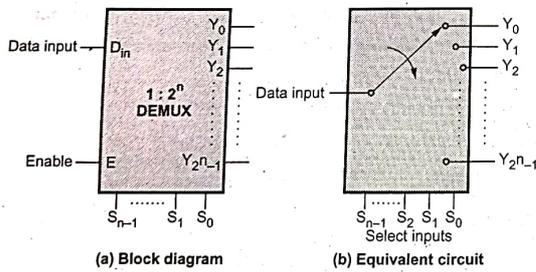


Fig. 4.11.1

Differentiate between Multiplexer and Demultiplexer

Parameter	Multiplexer	Demultiplexer
Definition	Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line.	Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines
Number of data inputs	2^n	1
Number of data outputs	1	2^n
Relationship of input and output	Many to one	One to many
Applications	<ul style="list-style-type: none"> • Used as a data selector • In time division multiplexing at the transmitting end 	<ul style="list-style-type: none"> • Used as a data distributor • In time division multiplexing at the receiving end

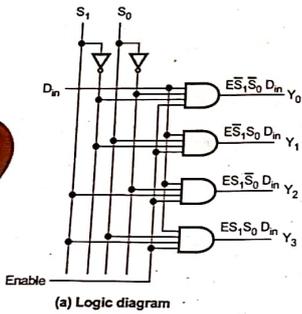
4.11.1 Types of Demultiplexers

4.11.1.1 1 : 4 Demultiplexer

Fig. 4.11.2 shows 1 : 4 demultiplexer. The single input variable D_m has a path to all four outputs, but the input information is directed to only one of the output lines depending on the select inputs. Enable input should be high to enable demultiplexer.

4.11.1.2 1 : 8 Demultiplexer

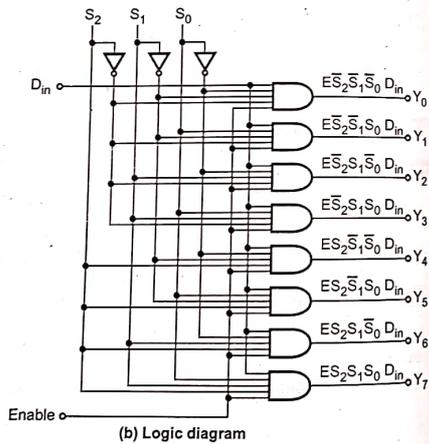
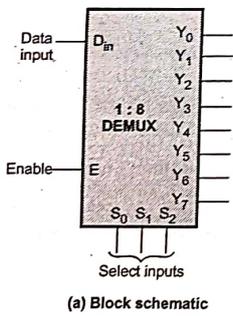
The Fig. 4.11.3 shows 1 : 8 demultiplexer. The single input data D_{in} has a path to all eight outputs, but the input information is directed to only one of the output lines depending on the select inputs.



Enable (E)	S ₁	S ₀	D _{in}	Y ₀	Y ₁	Y ₂	Y ₃
0	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

(b) Function table for 1 : 4 demultiplexer

Fig. 4.11.2



(a) Block schematic

(b) Logic diagram

Enable	Select inputs			Outputs							
	S ₂	S ₁	S ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	D _{in}	0	0	0	0	0	0	0
1	0	0	1	0	D _{in}	0	0	0	0	0	0
1	0	1	0	0	0	D _{in}	0	0	0	0	0
1	0	1	1	0	0	0	D _{in}	0	0	0	0
1	1	0	0	0	0	0	0	D _{in}	0	0	0
1	1	0	1	0	0	0	0	0	D _{in}	0	0
1	1	1	0	0	0	0	0	0	0	D _{in}	0
1	1	1	1	0	0	0	0	0	0	0	D _{in}

(c) Function table

Fig. 4.11.3 1 : 8 demultiplexer

4.11.2 Expanding Demultiplexers

To provide larger output needs we can cascade two or more demultiplexer to get demultiplexer with more number of output lines. Such a connection is known as demultiplexer tree.

Example 4.11.1 Design 1 : 8 demultiplexer using two 1 : 4 demultiplexers.

Solution :

- Step 1 : Connect D_{in} signal to D_{in} input of both the demultiplexers.
- Step 2 : Connect select lines B and C to select lines S₁ and S₀ of the both demultiplexers, respectively.

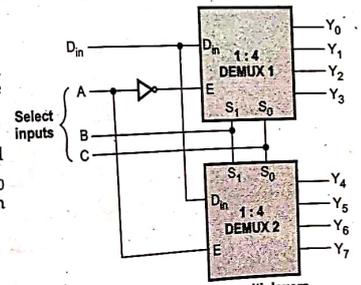


Fig. 4.11.4 Cascading of demultiplexers

Step 3 : Connect most significant select line (A) such that when A = 0 DEMUX 1 is enabled and when A = 1 DEMUX 2 is enabled.

Example 4.11.2 Implement 1 : 16 demultiplexer using 1 : 4 demultiplexers.

Solution : The 1 : 16 demultiplexer has 16 outputs. To select one of the 16 output, the circuit needs 4 ($\because 2^4 = 16$) select lines. Each 1 : 4 demultiplexer requires 2 select lines.

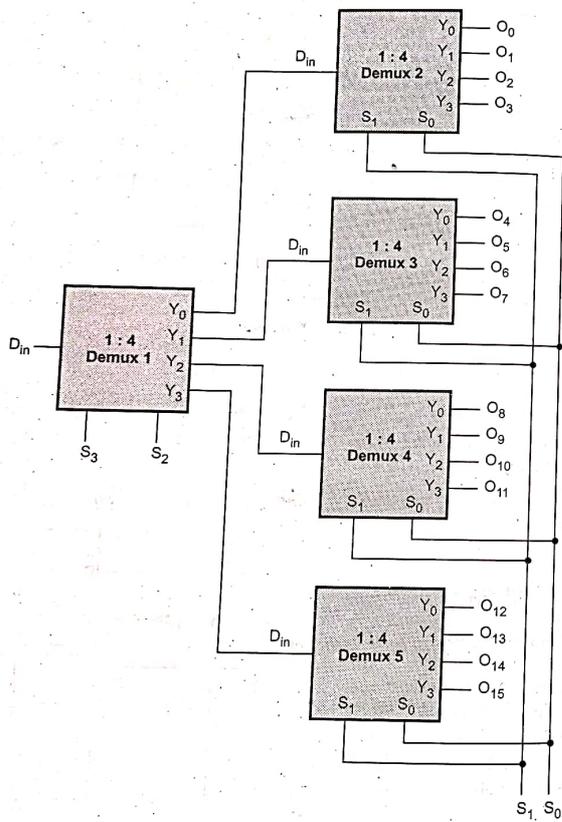


Fig. 4.11.5 1 : 16 Demux using 1 : 4 Demux

Step 1 : Connect two least significant select lines (S_1, S_0) to select lines of four 4 : 1 demultiplexer.

Step 2 : Connect one more 4 : 1 demultiplexer such that its four outputs are routed to the data inputs of the four demultiplexers. Connect higher select lines (S_3, S_2) to the select lines of this demultiplexer. (See Fig. 4.12.5 on previous page).

Examples for Practice

Example 4.11.3 Draw 1 : 64 demultiplexer tree using 1 : 16 demultiplexer.

Example 4.11.4 Draw 1 : 64 demultiplexer tree using 1 : 8 demultiplexer.

4.11.3 Implementation of Combinational Logic using Demultiplexer

Example 4.11.5 Implement full subtractor using demultiplexer.

Solution :

Step 1 : Write the truth table of full subtractor.

Step 2 : Represent output of full-subtractors in minterm form.

For full subtractor difference D function can be written as $D = f(A, B, C) = \sum m(1, 2, 4, 7)$ and B_{out} function can be written as,

$$B_{out} = F(A, B, C) = \sum m(1, 2, 3, 7)$$

Step 3 : Logically OR the outputs corresponding to minterms.

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 4.11.1 Truth table of full subtractor

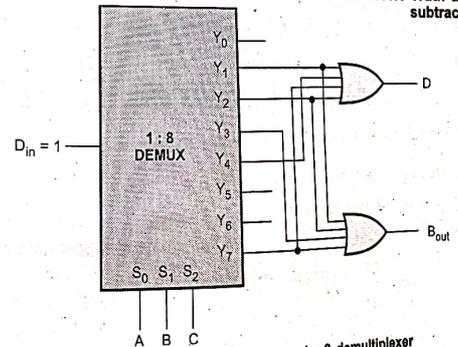


Fig. 4.11.6 Full subtractor using 1 : 8 demultiplexer

With D_{in} input 1, demultiplexer gives minterms at the output so by logically ORing required minterms we can implement Boolean functions for full subtractor. Fig. 4.11.6 shows the implementation of full subtractor using demultiplexer.

Example 4.11.6 Implement the following functions using demultiplexer :

$$f_1(A, B, C) = \sum m(0, 3, 7)$$

$$f_2(A, B, C) = \sum m(1, 2, 5)$$

Solution :

$$f_1(A, B, C) = \sum m(0, 3, 7)$$

$$f_2(A, B, C) = \sum m(1, 2, 5)$$

Implementation using 1 : 8 demultiplexer.

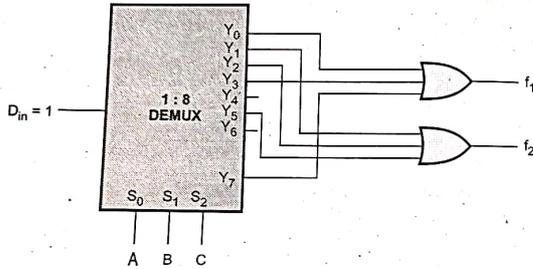


Fig. 4.11.7

Examples for Practice

Example 4.11.7 Implement full adder using demultiplexer.

Example 4.11.8 Implement the following functions using demultiplexer

$$f_1(A, B, C) = \sum m(1, 5, 7), \quad f_2(A, B, C) = \sum m(3, 6, 7)$$

4.11.4 Applications of Demultiplexer

1. It can be used as a decoder.
2. It can be used as a data distributor.
3. It is used in time division multiplexing at the receiving end as a data separator.
4. It can be used to implement Boolean expressions.

4.11.5 Demultiplexer ICs

IC Number	Function
74154	1 : 16 Demultiplexer
74155	Dual 1 : 4 Demultiplexer
Refer Appendix A for details	

Table 4.11.2 Demultiplexer ICs

Review Questions

1. Define demultiplexer.
2. Differentiate between multiplexer and demultiplexer.
3. State the applications of demultiplexer.

4.12 Decoders

GTU : May-12, 14, Dec.-13, Winter-15, 18, Summer-15, 18

A decoder is a multiple-input, multiple-output logic circuit which converts coded inputs into coded outputs, where the input and output codes are different.

The Fig. 4.12.1 shows the general structure of the decoder circuit. As shown in the Fig. 4.12.1, the encoded information is presented as n inputs producing 2^n possible outputs. The 2^n output values are from 0 through $2^n - 1$.

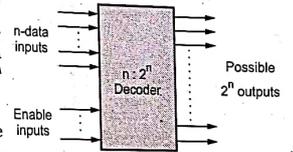


Fig. 4.12.1 General structure of decoder

Usually, a decoder is provided with enable inputs to activate decoded output based on data inputs. When any one enable input is unasserted, all outputs of decoder are disabled.

4.12.1 Binary Decoder

A decoder which has an n -bit binary input code and a one activated output out of 2^n output code is called **binary decoder**. A binary decoder is used when it is necessary to activate exactly one of 2^n outputs based on an n -bit input value.

Fig. 4.12.2 shows 2-to-4 decoder. Here, 2 inputs are decoded into four outputs, each output representing one of the

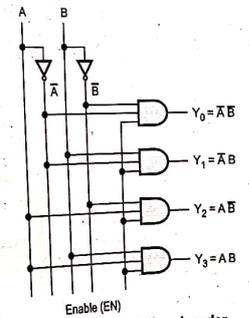


Fig. 4.12.2 2 to 4 line decoder

minterms of the 2 input variables. The two inverters provide the complement of the inputs, and each one of four AND gates generates one of the minterms.

The Table 4.12.1 shows the truth table for a 2-to-4 decoder. As shown in the truth table, if enable input is 1 (EN = 1), one, and only one, of the outputs Y_0 to Y_3 , is active for a given input. The output Y_0 is active, i.e. $Y_0 = 1$ when inputs $A = B = 0$, the output Y_1 is active when inputs $A = 0$ and $B = 1$. If enable input is 0, i.e. $EN = 0$, then all the outputs are 0.

Inputs			Outputs			
EN	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Table 4.12.1 Truth table for a 2 to 4 decoder

Example 4.12.1 With logic circuit and truth table explain the working of 3 : 8 line decoder.

GTU: Dec-13, Marks 7

Solution : Fig. 4.12.3 shows 3-to-8 line decoder. Here, 3 inputs are decoded into eight outputs, each output represent one of the minterms of the 3 input variables. The three inverters provide the complement of the inputs, and each one of the eight AND gates generates one of the minterms. Enable input is provided to activate decoded output based on data inputs A, B, and C. The table shows the truth table for 3-to-8 decoder.

Inputs				Outputs							
EN	A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Table 4.12.2 Truth table for a 3 to 8 decoder

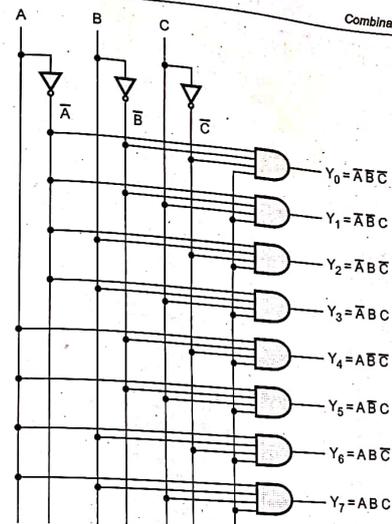


Fig. 4.12.3 3 : 8 line decoder

4.12.2 The 74X138 3-to-8 Decoder

The 74X138 is a commercially available 3-to-8 decoder. It accepts three binary inputs (A, B, C) and when enabled, provides eight individual active low outputs ($Y_0 - Y_7$). The device has three enable inputs : Two active low ($\overline{G}_A, \overline{G}_B$) and one active high (G_C). Fig. 4.12.4 and Table 4.12.3 show logic symbol and function table respectively.

Inputs						Outputs							
G_{2B}	G_{2A}	G_1	C	B	A	\overline{Y}_7	\overline{Y}_6	\overline{Y}_5	\overline{Y}_4	\overline{Y}_3	\overline{Y}_2	\overline{Y}_1	\overline{Y}_0
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1

0	0	1	0	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	0	1	1	1	0	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1	1
0	0	1	1	1	0	1	0	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1

Table 4.12.3 Function table

4.12.3 Expanding Cascading Decoders

Binary decoder circuits can be connected together to form a larger decoder circuit. Fig. 4.12.5 shows the 4 × 16 decoder using two 3 × 8 decoders.

Here, one input line (D) is used to enable/disable the decoders. When D = 0, the top decoder is enabled and the other is disabled. Thus the bottom decoder outputs are all 1s, and the top eight outputs generate minterms 0 0 0 0 0 1 1 1.

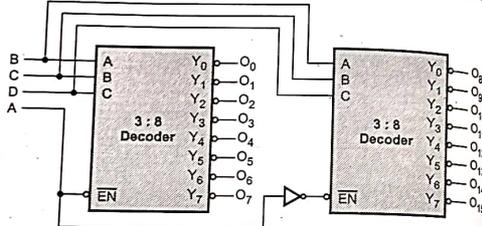


Fig. 4.12.5

When D=1, the enable conditions are reversed and thus bottom decoder outputs generate minterms 1000 to 1111, while the outputs of the top decoder are all 1s.

Example 4.12.2 Design 5-to-32 decoder using one 2-to-4 and four 3-to-8 decoder ICs.

Solution : The Fig. 4.12.6 shows the construction of 5-to-32 decoder using four 74LS138s and half 74LS139. The half section of 74LS139 IC is used as a 2-to-4 decoder to decode the two higher order inputs, D and E. The four outputs of this decoder are used to enable one of the four 3-to-8 decoders. The three lower order inputs A, B and C are connected in parallel to four 3-to-8 decoders. This means that the same output pin of each of the four 3-to-8 decoders is selected but only one is enabled. The remaining enable signals of four 3-to-8 decoder ICs are connected in parallel to construct enable signals for 5-to-32 decoder.

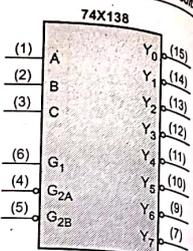


Fig. 4.12.4 Logic symbol

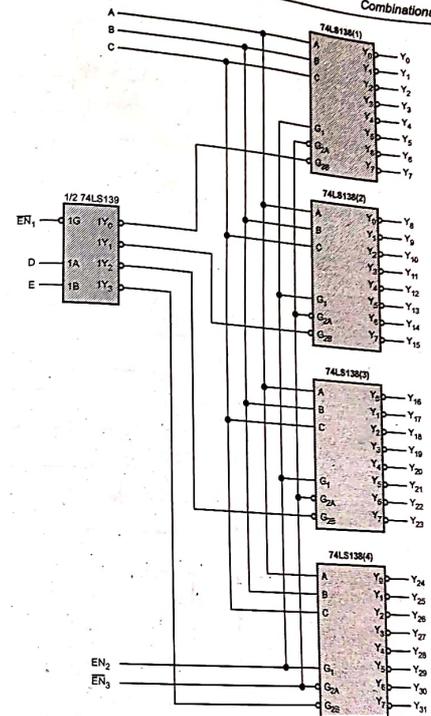


Fig. 4.12.6 5-to-32 decoder using 74LS138 and 74LS139

Example 4.12.3 Design 4 line to 16 line decoder using 2 line to 4 line decoders.

GTU : May-12, 14, Marks 7

Solution : 4 line to 16 line decoder using 1 line to 4 line decoder.

As shown in Fig. 4.12.7 five 2 : 4 decoders are required to design 4 : 16 decoder. Decoder 1 is used to enable one of the decoder 2, 3, 4 and 5. Inputs of first decoder are the A and B, MSB inputs of 4 :16 decoder. The inputs of decoder 2, 3, 4 and 5 are connected together forming C and D LSB inputs of 4 : 16 decoder.

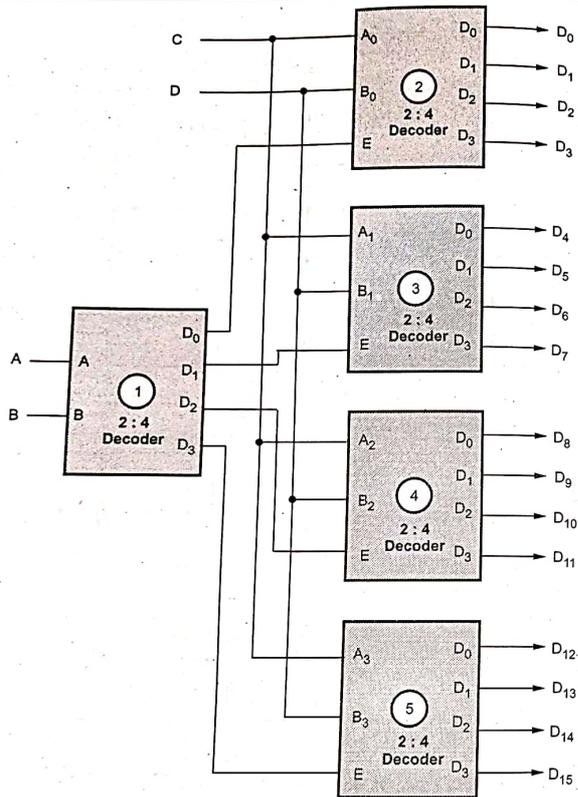


Fig. 4.12.7

When A and B are 0 0, decoder 1 is enabled, for AB = 0 1 decoder 2 is enabled, for AB = 1 0 decoder 3 is enabled and for A = B = 1, decoder 4 is enabled.

4.12.4 Realization of Boolean Function using Decoder

The combination of decoder and external logic gates can be used to implement single or multiple output functions. We know that decoder can have one of the two output

states; either active low or active high. Let us see the significance of these output states in the implementation of binary function.

When decoder output is active high, it generates minterms (product terms) for input variables; i.e. it makes selected output logic 1. In such case to implement SOP function we have to take sum of selected product terms generated by decoder.

Illustrative Examples

Example 4.12.4 Implement Boolean function $F = \sum m(1, 2, 3, 7)$ using 3 : 8 decoder.

Solution :

Step 1 : Connect function variables as inputs to the decoder.

Step 2 : Logically OR the outputs correspond to present minterms to obtain the output.

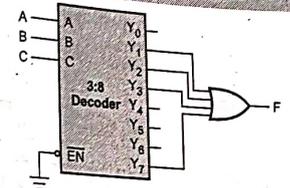


Fig. 4.12.8

Example 4.12.5 Design and implement a full adder circuit using a 3 : 8 decoder.

GTU - Winter-15, Marks 7

Solution : Truth table for full adder is as shown in the Table 4.12.4.

Inputs			Outputs	
A	B	C _{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

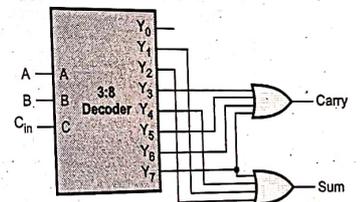


Fig. 4.12.9

Table 4.12.4 Truth table for full-adder

Example 4.12.6 Implement the following Boolean functions with a decoder

GTU - Winter-18, Marks 7

$$F(w, x, y, z) = \sum (1, 3, 5, 6, 11, 14, 15)$$

Solution :

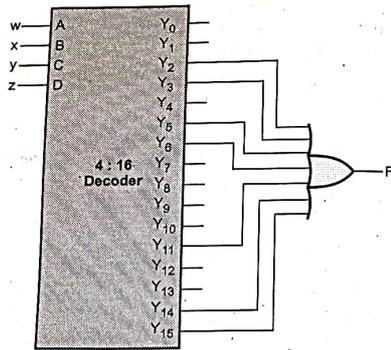


Fig. 4.12.10

Example 4.12.7 Using suitable decoder and OR gates, design 4-bit binary to gray code convertor. **GTU : Summer-18, Marks 7**

Solution :

Step 1 : Form the Truth table relating 8421 binary code and Gray code

Input code : Binary code : $B_3 B_2 B_1 B_0$

Output code : Gray code : $G_3 G_2 G_1 G_0$

Decimal	Binary code				Gray code			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1

10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	0
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Table 4.12.5

Step 2 : Implement Truth Table using decoder

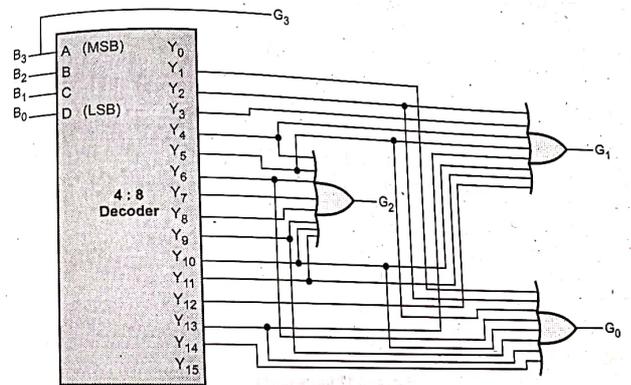


Fig. 4.12.11

Examples for Practice

Example 4.12.8 : Implement the following Boolean functions using decoder and OR gates :

$$F_1(A, B, C, D) = \sum (2, 4, 7, 9)$$

$$F_2(A, B, C, D) = \sum (10, 13, 14, 15)$$

Example 4.12.9 : Implement the logic circuit for full subtractor using decoder.

Example 4.12.10 : Explain decoder (1 : 8) as a binary to gray code converter. Show your design.

4.12.5 Implementation of Logic Function using IC 74138

IC 74138 is a 3:8 decoder with active-low outputs. In section 4.12.4 we have seen how to implement combinational logic function using decoder with active-high outputs. For active-high outputs, we use OR gate to implement the function. We know that bubbled-NAND is OR. Thus, for active-low outputs we have to use NAND gate to implement the function.

Example 4.12.11 Implement full subtractor using a decoder (IC 74138) and write a truth table.

Solution : The truth table for full subtractor is as shown in Table 4.12.6.

Inputs			Outputs	
A	B	B _{in}	D	B _{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 4.12.6 Truth table for full subtractor

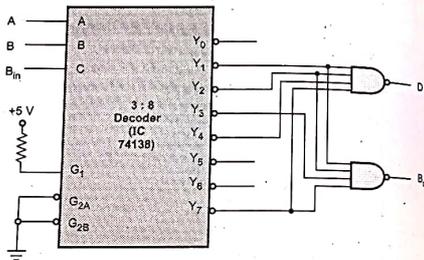


Fig. 4.12.12 Implementation of full subtractor using 3:8 decoder (IC 74138)

4.12.6 Applications of Decoder

The uses of decoders are :

- Code converters
- Implementation of combinational circuits
- Address decoding
- BCD to 7-segment decoder

4.12.7 Decoder ICs

IC Number	Function
74138	3:8 Decoder
74139	Dual 2:4 Decoder
7442	BCD to decimal decoder
7447	BCD to 7-segment decoder

Table 4.12.7 Decoder ICs

4.12.8 Seven Segment Decoder

In most practical applications, seven segment displays are used to give a visual indication of the output states of digital ICs such as decade counters, latches etc. These outputs are usually in four bit BCD (binary coded decimal) form, and are thus not suitable for directly driving seven segment displays. The special BCD to seven segment decoder/driver ICs are used to convert the BCD signal into a form suitable for driving these displays. In this sections, we are going to study LED and LCD decoders/drivers for seven segment displays. Let us tabulate the segments activated during each digit display.

Digit	Segments Activated	Display
0	a, b, c, d, e, f	
1	b, c	
2	a, b, d, e, g	
3	a, b, c, d, g	
4	b, c, f, g	

5	a, c, d, f, g	
6	a, c, d, e, f, g	
7	a, b, c	
8	a, b, c, d, e, f, g	
9	a, b, c, d, f, g	

Table 4.12.8

From the above Table 4.12.8 we can determine the truth table for BCD-to-7 segment decoder/driver. This truth table also depends on the construction of 7-segment display. If 7-segment display is common anode, the segment driver output must be active low to glow the segment. In case of common cathode type 7-segment display, the segment driver output must be active high to glow the segment. Table 4.12.9 and 4.12.10 show the truth tables for both BCD to 7 segment decoder/driver with common cathode display and with common anode display respectively.

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 4.12.9 Truth table for BCD-to-common cathode 7-segment decoder/driver

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	1	1	1	1
3	0	0	1	1	0	0	0	1	0	0	1
4	0	1	0	0	0	0	0	0	1	1	0
5	0	1	0	1	0	0	0	1	1	0	0
6	0	1	1	0	0	1	0	0	0	1	0
7	0	1	1	1	0	0	0	0	0	0	0
8	1	0	0	0	0	0	0	0	1	1	1
9	1	0	0	1	0	0	0	0	1	0	0

Table 4.12.10 Truth table for BCD-to-common anode 7-segment decoder/driver. Let us design the combinational circuit for common cathode 7-segment display/driver.

K-map simplification

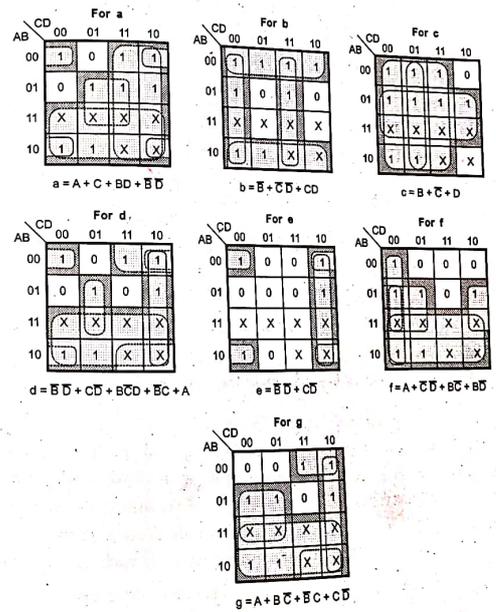


Fig. 4.12.13

Logic diagram

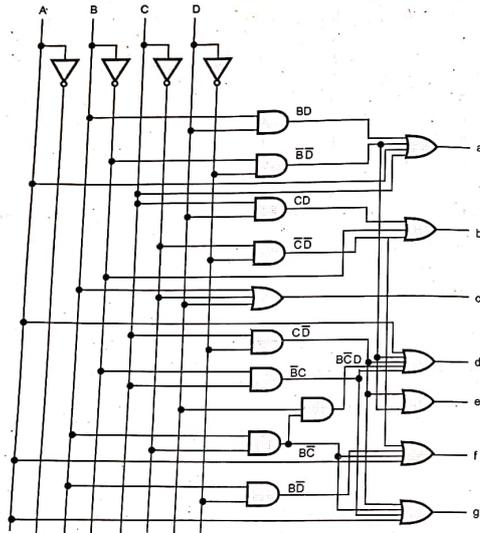


Fig. 4.12.14

Example 4.12.12 Implement BCD-to-7 segment decoder for common anode using 4 : 16 decoder.

Solution : Referring the truth table from Table. 4.12.9 we can implement BCD-to-7 segment decoder for common anode as shown in the Fig. 4.12.15.

4.12.8.1 Basic Connection for Driving 7-Segment Displays

Fig. 4.12.16 and 4.12.17 show the basic connections of BCD to seven segment decoder/driver for common-anode and common-cathode displays, respectively. In both the circuits, current limiting resistors are placed in series with each display segment. Looking at the figures, we can observe that common anode decoder/driver sinks current whereas common-cathode decoder/driver source the current to each display segment.

Now we will see the practical decoder/driver ICs, their pin connections, functional description and features.

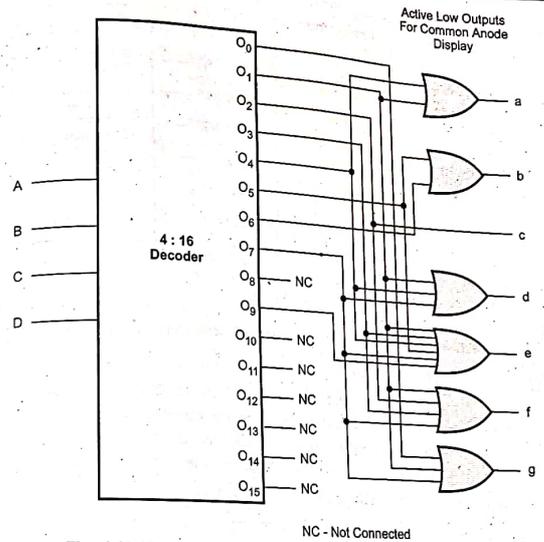


Fig. 4.12.15 BCD-to-7 segment decoder using 4 : 16 decoder

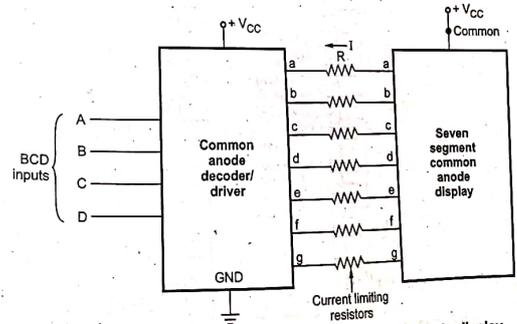


Fig. 4.12.16 Basic connections for driving common anode display

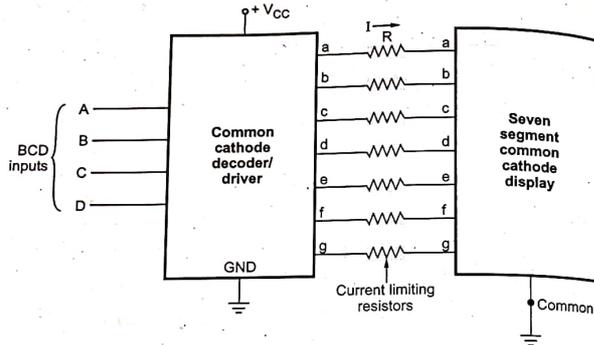


Fig. 4.12.17 Basic connections for driving common cathode display

4.12.8.2 IC 7446A, 7447A and 74LS47

The 7446A, 7447A and 74LS47 ICs accept four lines of BCD input data and gives open collector outputs to drive the individual segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for 74LS47) in the 'ON' (LOW) state. As the outputs of these ICs sink the current, it is suitable to drive common anode seven segment displays.

Fig. 4.12.18 shows the pin diagram for 7446A, 7447A and 74LS47.

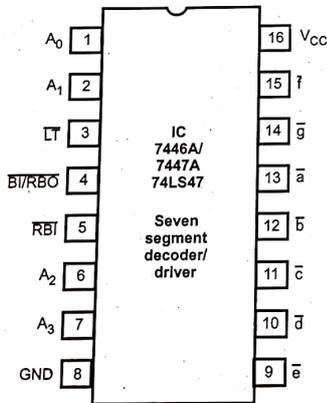


Fig. 4.12.18 Pin diagram for 7446A, 7447A and 74LS47

Pins A_0, A_1, A_2 and A_3 represent BCD inputs with A_0 as a least significant bit (LSB) and A_3 as a most significant bit (MSB). Pins \bar{a} through \bar{g} are the seven segment outputs. These are active low outputs, i.e. when segment output goes low (active state), segment is made 'ON'. The test lamp pin (\bar{LT}) is provided to test whether all segments are working properly or not. When \bar{LT} pin is held low with \bar{RBO} pin open or at logic high, IC drives all display terminals ON (active low). When the \bar{BI}/\bar{RBO} pin is pulled low, all outputs are blanked; this pin also functions as a ripple-blanking output terminal. \bar{BI}/\bar{RBO} along with RBI can be used to provide ripple blanking feature discussed later.

Fig. 4.12.19 shows a circuit to drive a single, seven segment, common anode LED display. For common anode, when anode is connected to positive supply, a low voltage is applied to a cathode to turn it on. Here, BCD to seven segment decoder, IC 7447 is used to apply low voltages at cathodes according to BCD input applied to 7447. To limit the current through LED segments, resistors are connected in series with the segments. This circuit connection is referred to as a static or non-multiplex display because current is being passed through the display at all times.

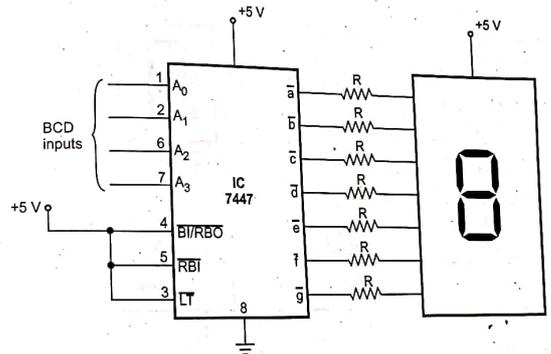


Fig. 4.12.19 Circuit for driving single seven segment display using 7446/7447

The value of the resistor in series with the segment can be calculated as follows :

We know, $V_{CC} - \text{drop across LED segment} - IR = 0$

Drop across LED segment is nearly 1.5 V.

$$\begin{aligned} IR &= V_{CC} - 1.5 \text{ V} \\ &= 5 - 1.5 \text{ V} \\ &= 3.5 \text{ V} \end{aligned}$$

Each LED segment requires a current of between 5 and 30 mA to light. Let us assume that current through LED segment is 15 mA

$$R = \frac{3.5 \text{ V}}{1.5 \text{ mA}} = 233 \Omega$$

In practice, the voltage drop across the LED and the output of 7447 are not exactly predictable and the exact current through the LED is not critical as long as we do not exceed its maximum current rating. Therefore, a standard value 220 Ω can be used.

(a) Cascaded Non Multiplexed Displays

Several sets of seven segment displays and associated decoder/drivers ICs can be cascaded to make multi-digit display system. Fig. 4.12.20 shows the connection for cascaded multi-digit display system.

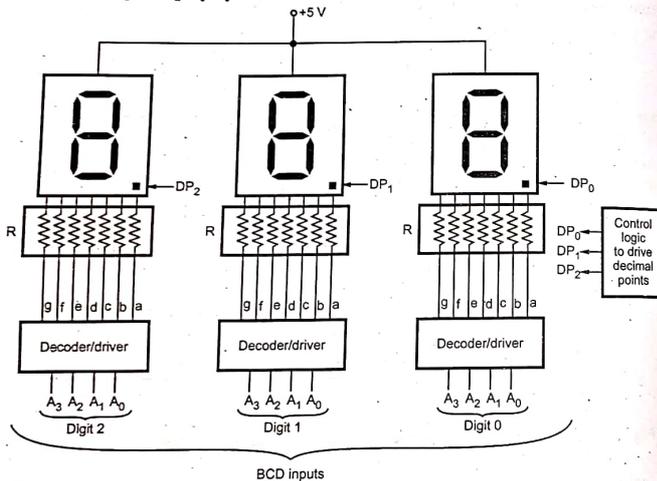


Fig. 4.12.20 Cascaded multi-digit non multiplexed display system

(b) Ripple Blanking in Multi-digit Displays

If the display system shown in Fig. 4.12.20 is used to display count of 8, then it actually gives the reading 008. Similarly, if it is used to display 0.2, it actually gives reading 0.20. These leading and trailing zeroes can be automatically blanking using RBI and RBO signals of the IC 7447 decoder/driver. The technique of blanking leading and trailing zeroes is called ripple blanking.

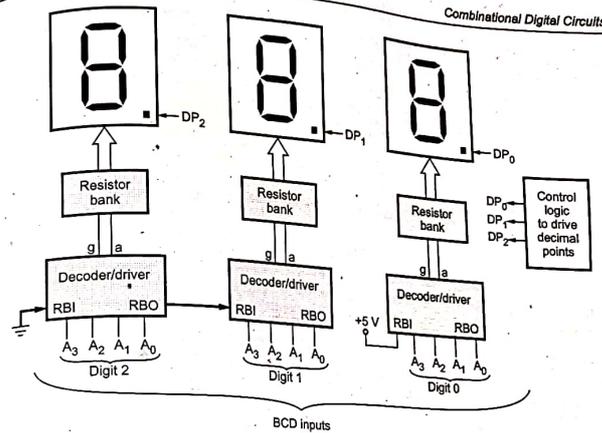


Fig. 4.12.21 Circuit for blanking leading zeroes

Fig. 4.12.21 and 4.12.22 show circuits to provide ripple blanking for leading zeroes and trailing zeroes.

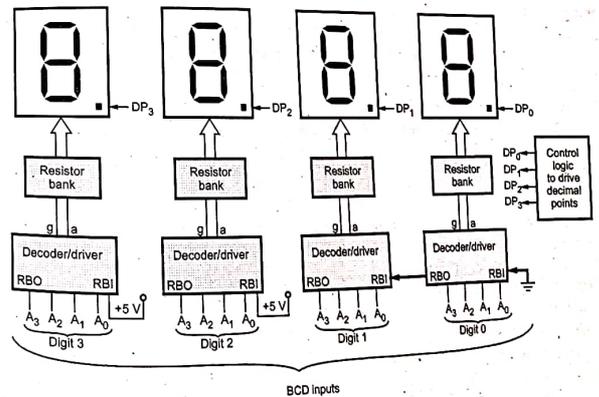


Fig. 4.12.22 Circuit for blanking trailing zeroes

To understand the working of signals RBI and RBO we will see the internal circuit for these two signals, as shown in Fig. 4.12.23.

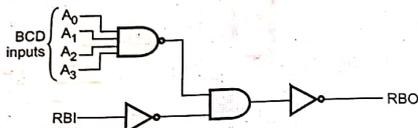


Fig. 4.12.23 Internal circuit for RBI and RBO signals

When RBI is low (activated) and all the BCD inputs are zero, then RBO goes low. Looking at Fig. 4.12.21 we can observe that when there is leading zero, digit 2 is blanked and it sets RBI zero for adjacent digit (digit 1), so that if BCD inputs for adjacent digit (digit 1) are zero, the digit is blanked.

In case of trailing zero the process of blanking starts from the right most digit. Here, digit 0 is blanked if all BCD inputs to the digit 0 are zero. If so, RBO for digit 0 goes low and therefore RBI input for digit 1 is low. Now if all BCD inputs of the digit 1 are zero then digit 1 is blanked.

(c) Multiplexed Displays

Untill now we have seen static or non-multiplexed display circuits. These circuits work well for driving up to four LED digits. However, these circuits are not suitable for driving more LED digits, say 8 digits. When there are more number of digits, the first problem is a power consumption. For worst-case calculations, assume that all eight digits with all segments are lit. Therefore, worst case current required is

$$I = 8 \text{ (digits)} \times 7 \text{ (segments)} \times 15 \text{ mA (current per segment)} = 840 \text{ mA}$$

A second problem of the static approach is that each display digit requires a separate BCD to 7 segment decoder. To solve the problems of the static non-multiplexed display approach multiplexed display method is used. Fig. 4.12.24 shows the 4 seven segment displays connected using multiplexed method. Here, common anode seven segment LEDs are used.

Anodes are connected to + 5 V through transistors. Cathodes of all seven segments are connected in parallel and then to the output of 7447 IC through resistors. Looking at the Fig. 4.46, the question may occur in our mind that, "Aren't all of the digits going to display the same number ?" The answer is that they would show the same number only if all the digits are turned-on at the same time. However, in multiplexed display the segment information is sent for all digits on the common lines (output lines of 7447), but only one display digit is turned on at a time. The PNP transistors connected in series with the common anode of each digit acts as an ON and OFF switch for that digit. Here is how the multiplexing process works.

The BCD code for digit 0 is first applied to the 7447. The 7447, BCD to seven segment decoder outputs the corresponding seven segment code on the segment bus lines. The transistor Q₀ connected to digit 0 is then turned on by corresponding control signals. All of the rest of the control lines are made high to ensure no other digits are turned on. After 2 ms, digit 0 is turned-off by making all control inputs high. The BCD code for digit 1 is then applied and the control input for digit 1 is made low to turn it ON. After next 2 ms, digit 1 is turned-off and the process is repeated for digit 2 and digit 4. After completion of turn for each digit, all the digits are lit again in turn.

With 4 digits and 2 ms per digit we get back to digit 1 every 8 ms or about 125 times a second. This refresh rate is fast enough that, to our eye and due to persistence of all digits will appear to be lit all the time.

In multiplexed display, the segment current is kept in between 40 mA to 60 mA so that they will appear as bright as they would, if not multiplexed. Even with this increased segment current, multiplexing gives a large saving in power and hardware components.

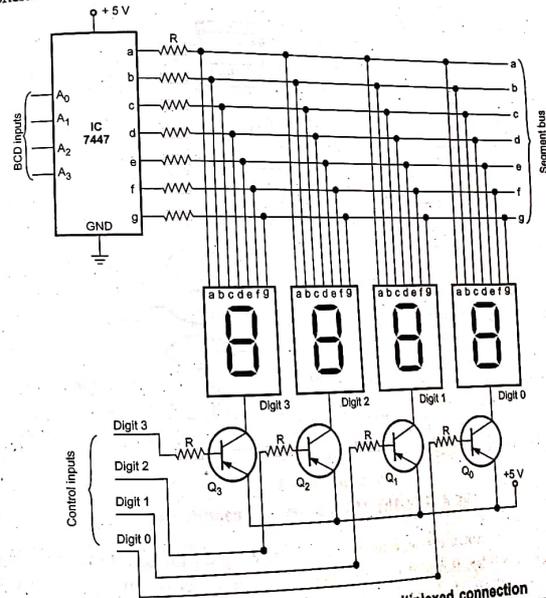


Fig. 4.12.24 Seven segment display in multiplexed connection

4.12.8.3 IC 74X49 Seven Segment Decoder

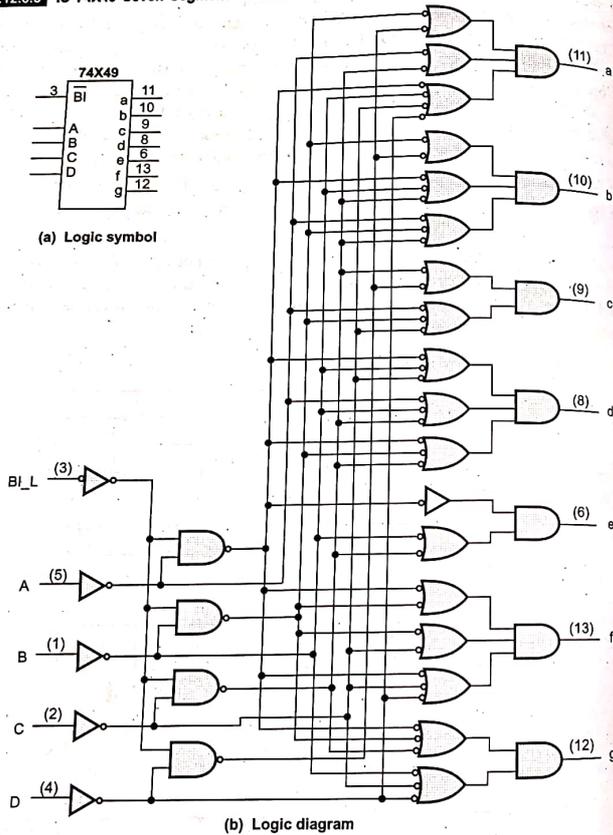


Fig. 4.12.25 The 74X49 seven segment decoder

The Fig. 4.12.25 shows the pinouts and the logic diagram for IC 74X49, 4-bit BCD to seven segment decoder. It has active-low blanking \overline{BL} input. When \overline{BL} input is activated the outputs are logic 0. The Table 4.12.11 shows the truth table for IC 74X49.

Inputs					Outputs						
\overline{BI}	D	C	B	A	a	b	c	d	e	f	g
0	X	X	X	X	0	0	0	0	0	0	0
1	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
1	0	0	1	0	1	1	0	1	1	0	1
1	0	0	1	1	1	1	1	1	0	0	1
1	0	1	0	0	0	1	1	0	0	1	1
1	0	1	0	1	1	0	1	1	0	1	1
1	0	1	1	0	0	0	1	1	1	1	1
1	0	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	0	0	1	1
1	1	0	1	0	0	0	0	1	1	0	1
1	1	0	1	1	0	0	1	1	0	0	1
1	1	1	0	0	0	1	0	0	0	1	1
1	1	1	0	1	1	0	0	1	0	1	1
1	1	1	1	0	0	0	0	1	1	1	1
1	1	1	1	1	0	0	0	0	0	0	0

Table 4.12.11 Truth table for IC 74X49

Review Questions

1. What is decoder ?
2. Draw logic diagram of 3-line to 8-line decoder.
3. What is difference between demultiplexer and decoder ?
4. Compare and contrast : Multiplexer and decoder.
5. Give applications of decoder.
6. Design full adder using suitable decoder.
7. Design 4x16 decoder using two 3x8 decoder.

GTU : Summer-18, Marks 4

GTU : Summer-15, Marks 7

4.13 Encoders

- An encoder is a digital circuit that performs the inverse operation of a decoder.
- An encoder has 2^n (or fewer) input lines and n output lines.
- In encoder the output lines generate the binary code corresponding to the input value.

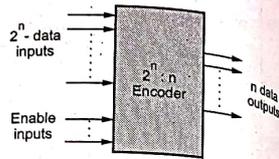


Fig. 4.13.1 General structure of encoder

The Fig. 4.13.1 shows the general structure of the encoder circuit. As shown in the Fig. 4.13.1 the decoded information is presented as 2^n inputs producing n possible outputs.

4.13.1 Decimal to BCD Encoder

- The decimal to BCD encoder, usually has ten input lines and four output lines.
- The decoded decimal data acts as an input for encoder and encoded BCD output is available on the four output lines.
- The Fig. 4.13.2 shows the logic symbol for decimal to BCD encoder IC, IC 74XX147.

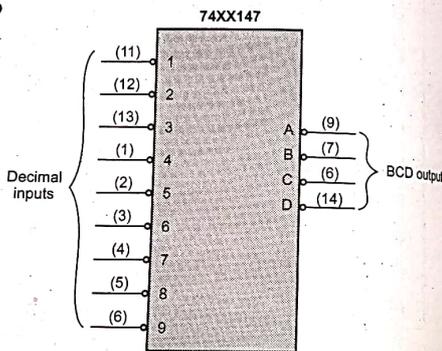


Fig. 4.13.2 Logic symbol for 74XX147 (Decimal to BCD encoder)

- It has nine input lines and four output lines.
- Both input and output lines are asserted active low.
- It is important to note that there is no input line for decimal zero. When this condition occurs, all output lines are 1.
- The function table for the 74XX147 is shown in Table 4.13.1.

Decimal value	Inputs									Outputs			
	1	2	3	4	5	6	7	8	9	D	C	B	A
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	x	0	1	1	1	1	1	1	1	1	1	0	1
3	x	x	0	1	1	1	1	1	1	1	0	1	1
4	x	x	x	0	1	1	1	1	1	0	1	1	1
5	x	x	x	x	0	1	1	1	1	0	1	0	1
6	x	x	x	x	x	0	1	1	1	0	0	1	1
7	x	x	x	x	x	x	0	1	1	0	0	0	1
8	x	x	x	x	x	x	x	0	1	0	1	1	1
9	x	x	x	x	x	x	x	x	0	0	1	1	0

x indicates don't care condition

Table 4.13.1 Truth table for decimal to BCD encoder

Example 4.13.1 Draw the interfacing diagram of ten key keypad interface to a digital system using decimal to BCD encoder.

Solution :

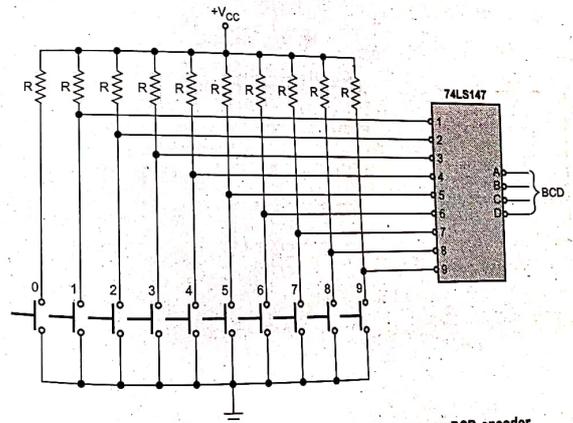


Fig. 4.13.3 Ten key keypad interface using decimal to BCD encoder

4.13.2 Priority Encoder

- A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.
- Table 4.13.2 shows truth table of 4-bit priority encoder.
- Table 4.13.2 shows D_3 input with highest priority and D_0 input with lowest priority.
- When D_3 input is high, regardless of other inputs output is ($Y_1 Y_0 = 11$) 11.
- The D_2 has the next priority. Thus, when $D_3 = 0$ and $D_2 = 1$, regardless of other two lower priority input, output is 10.
- The output for D_1 is generated only if higher priority inputs are 0, and so on.
- The output V (a valid output indicator) indicates, one or more of the inputs are equal to 1. If all inputs are 0, V is equal to 0, and the other two outputs (Y_1 and Y_0) of the circuit are not used.

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_0	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Table 4.13.2 Truth table of 4-bit priority encoder

Example 4.13.2 Design a priority encoder circuit for 4-bit input.

Solution : Refer Table 4.13.2.

K-map simplification

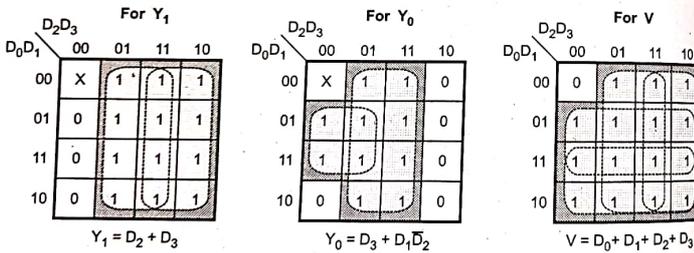


Fig. 4.13.4

Logic diagram

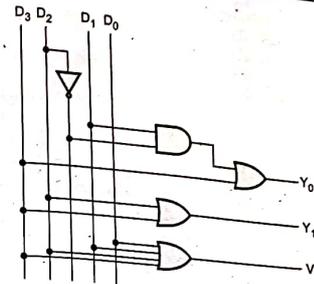
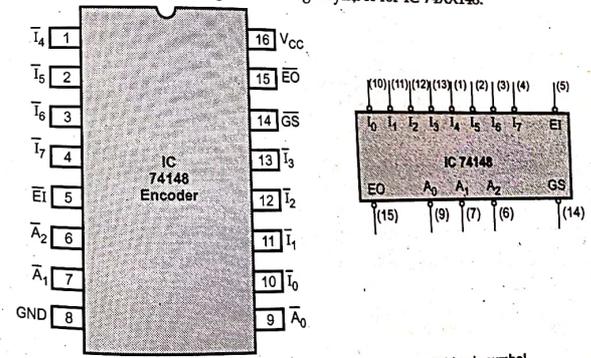


Fig. 4.13.5

4.13.3 Priority Encoder IC (74XX148)

- The IC 74XX148 is an 8-input priority encoder. It accepts data from eight active low inputs and provides a binary representation on the three active-low outputs.
- A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output.
- Input I_0 has least priority and input I_7 has highest priority.
- Fig. 4.13.6 shows pin diagram and logic symbol for IC 74XX148.



(a) Pin diagram

(b) Logic symbol

Fig. 4.13.6

- \overline{EI} is the active low Enable Input. A high on the \overline{EI} will force all outputs to the inactive (high) state and allow new data to settle without producing erroneous information at the outputs.
- A Group Signal (\overline{GS}) is asserted when the device is enabled and one or more of the inputs to the encoder are active.
- Enable Output (\overline{EO}) is an active low signal that can be used to cascade several priority encoder devices to form a larger priority encoding system.
- When all inputs are high, i.e., none of the input is active, the \overline{EO} goes low indicating that no priority event connected to the IC is present.
- In cascaded priority encoders, \overline{EO} is connected to the \overline{EI} input of the next lower priority encoder.
- The Table 4.13.3 shows the truth table for 74XX148 priority encoder.

EI	Inputs								Outputs				
	0	1	2	3	4	5	6	7	A_2	A_1	A_0	GS	EO
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	x	0	1	1	1	1	1	1	1	0	0	0	1
0	x	x	0	1	1	1	1	1	0	1	0	0	1
0	x	x	x	0	1	1	1	1	0	0	0	0	1
0	x	x	x	x	0	1	1	0	1	1	0	0	1
0	x	x	x	x	x	0	1	0	0	1	0	0	1
0	x	x	x	x	x	x	0	0	0	0	0	0	1

Table 4.13.3 Truth table for the 74XX148 priority encoder

4.13.4 Octal to Binary Encoder

- Fig. 4.13.7 shows octal to binary encoder. It has eight inputs, one for each octal digit, and three outputs that generate the corresponding binary code.
- In encoders it is assumed that only one input has a value of 1 at any given time; otherwise the circuit is meaningless.
- Table 4.13.4 shows the truth table of octal to binary converter.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Outputs		
								A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Table 4.13.4 Truth table of octal-to-binary encoder

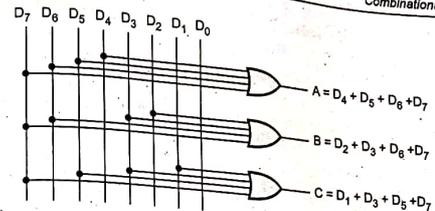


Fig. 4.13.7 Octal to binary encoder

- The above circuit has one more ambiguity that when all inputs are 0s the outputs are 0s. The zero output can also be generated when $D_0 = 1$. This ambiguity can be resolved by providing an additional output that specifies the valid condition.

4.13.5 Encoder ICs

IC Number	Function
74147	Decimal to BCD encoder
74148	8-input priority Encoder

Table 4.13.5 Encoder ICs

Review Questions

1. What is encoder ?
2. Define priority encoder.

4.14 Adders

GTU : May-13, Dec-13

Digital computers perform various arithmetic operations. The most basic operation, no doubt, is the addition of two binary digits. This simple addition consists of four possible elementary operations, namely,

$$\begin{aligned}
 0 + 0 &= 0 \\
 0 + 1 &= 1 \\
 1 + 0 &= 1 \\
 1 + 1 &= 10_2
 \end{aligned}$$

The first three operations produce a sum whose length is one digit, but when the last operation is performed sum is two digits. The higher significant bit of this result is called a carry, and lower significant bit is called sum. The logic circuit which performs

this operation is called a half-adder. The circuit which performs addition of three bits (two significant bits and a previous carry) is a full-adder.

4.14.1 Half Adder

The half-adder operation needs two binary inputs : augend and addend bits; and two binary outputs : sum and carry. The truth table shown in Table 4.14.1 gives the relation between input and output variables for half-adder operation.

Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 4.14.1 Truth table for half-adder

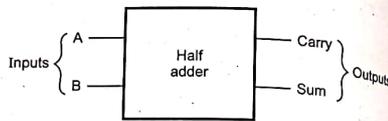
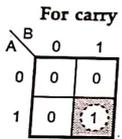
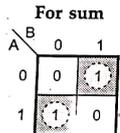


Fig. 4.14.1 Block schematic of half-adder

K-map simplification for carry and sum



Carry = AB



Sum = $\overline{A}B + A\overline{B}$
= $A \oplus B$

Logic diagram

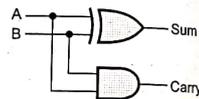


Fig. 4.14.3 Logic diagram for half-adder

Fig. 4.14.2 Maps for half-adder

Limitations of Half-Adder :

In multidigit addition we have to add two bits along with the carry of previous digit addition. Effectively such addition requires addition of three bits. This is not possible with half-adder. Hence half-adders are not used in practice.

Example 4.14.1 Draw half adder using NAND gates.

Solution : For half adder :

$$\begin{aligned} \text{Sum} &= \overline{A}B + A\overline{B} & C_{out} &= AB \\ &= \overline{\overline{\overline{\overline{A}B + A\overline{B}}}} & &= \overline{\overline{AB}} \\ &= \overline{A \cdot B} & &= \overline{A \cdot B} \end{aligned}$$

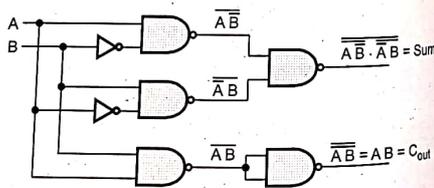


Fig. 4.14.4

4.14.2 Full Adder

A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by A and B, represent the two significant bits to be added. The third input C_{in} represents the carry from the previous lower significant position. The truth table for full-adder is shown in Table 4.14.2.

Inputs			Outputs	
A	B	C_{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 4.14.2 Truth table for full-adder

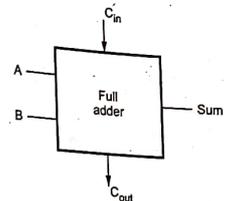
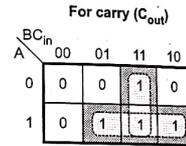
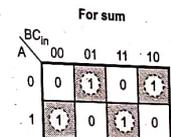


Fig. 4.14.5 Block schematic of full-adder

K-map simplification for carry and sum



$C_{out} = AB + AC_{in} + BC_{in}$



Sum = $\overline{A}BC_{in} + \overline{A}B\overline{C}_{in} + A\overline{B}C_{in} + ABC_{in}$

Fig. 4.14.6 Maps for full-adder

Logic diagram

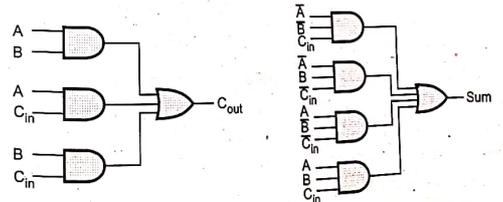


Fig. 4.14.7 Sum of product implementation of full-adder

The Boolean function for sum can be further simplified as follows :

$$\begin{aligned} \text{Sum} &= \bar{A} \bar{B} C_{in} + \bar{A} B \bar{C}_{in} + A \bar{B} \bar{C}_{in} + A B C_{in} \\ &= C_{in} (\bar{A} \bar{B} + AB) + \bar{C}_{in} (\bar{A} B + A \bar{B}) \\ &= C_{in} (A \odot B) + \bar{C}_{in} (A \oplus B) \\ &= C_{in} (\overline{A \oplus B}) + \bar{C}_{in} (A \oplus B) \\ &= C_{in} \oplus (A \oplus B) \end{aligned}$$

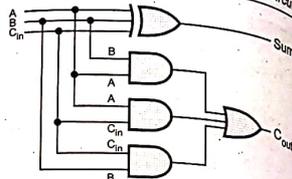


Fig. 4.14.8 Implementation of full-adder

With this simplified Boolean function circuit for full-adder can be implemented as shown in the Fig. 4.14.8.

Full adder using two half adders

A full-adder can also be implemented with two half-adders and one OR gate, as shown in the Fig. 4.14.9. The sum output from the second half-adder is the exclusive-OR of C_{in} and the output of the first half-adder, giving

$$\begin{aligned} C_{out} &= AB + A C_{in} + B C_{in} = AB + A C_{in} (B + \bar{B}) + B C_{in} (A + \bar{A}) \\ &= AB + ABC_{in} + A \bar{B} C_{in} + ABC_{in} + \bar{A} B C_{in} = AB (1 + C_{in} + C_{in}) + A \bar{B} C_{in} + \bar{A} B C_{in} \\ &= AB + A \bar{B} C_{in} + \bar{A} B C_{in} = AB + C_{in} (A \bar{B} + \bar{A} B) = AB + C_{in} (A \oplus B) \end{aligned}$$

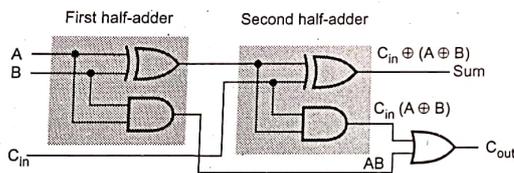


Fig. 4.14.9 Implementation of a full-adder with two half-adders and an OR gate

Review Questions

1. Design a full adder
2. Define half adder and full adder.
3. Draw a block diagram of half adder. Write truth table. Draw logic diagram.
4. Write a truth table for half adder, reduce the equation using K-map and design half adder using logic gates.
5. Define full adder. Draw logic circuit and truth table of full adder.
6. Implement full adder using two half adders.
7. Explain half and full adders in detail.

GTU : May-13, Dec.-13, Marks 7

4.15 Subtractors

The subtraction consists of four possible elementary operations, namely,
 0 - 0 = 0
 0 - 1 = 1 with 1 borrow
 1 - 0 = 1
 1 - 1 = 0

In all operations, each subtrahend bit is subtracted from the minuend bit. In case of second operation the minuend bit is smaller than the subtrahend bit, hence 1 is borrowed. Just as there are half and full-adders, there are half and full-subtractors.

4.15.1 Half Subtractor

A half-subtractor is a combinational circuit that subtracts two-bits and produces their difference. It also has an output to specify if a 1 has been borrowed. Let us designate minuend bit as A and the subtrahend bit as B. The result of operation A - B for all possible values of A and B is tabulated in Table 4.15.1.

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 4.15.1 Truth table for half-subtractor

As shown in the Table 4.15.1, half-subtractor has two input variables and two output variables. The Boolean expression for the outputs of half-subtractor can be determined as follows.

K-map simplification for half-subtractor

For difference

	B	0	1
A	0	0	1
	1	1	0

$$\begin{aligned} \text{Difference} &= A\bar{B} + \bar{A}B \\ &= A \oplus B \end{aligned}$$

For borrow

	B	0	1
A	0	0	1
	1	0	0

$$\text{Borrow} = \bar{A}B$$

Fig. 4.15.1

Limitations of half-subtractor :

In multidigit subtraction, we have to subtract two bits along with the borrow of the previous digit subtraction. Effectively such subtraction requires subtraction of three bits. This is not possible with half-subtractor.

Logic diagram

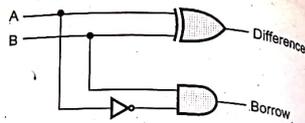


Fig. 4.15.2 Implementation of half-subtractor

Example 4.15.1 Draw half subtractor using NAND gates.

Solution : For half subtractor :

$$\begin{aligned} \text{Difference} &= A\bar{B} + \bar{A}B \\ &= \overline{A\bar{B}\bar{A}B} \\ &= \overline{A\bar{B} \cdot \bar{A}B} \\ \text{Borrow} &= \bar{A}B \\ &= \overline{A\bar{B}} \end{aligned}$$

Implementation :

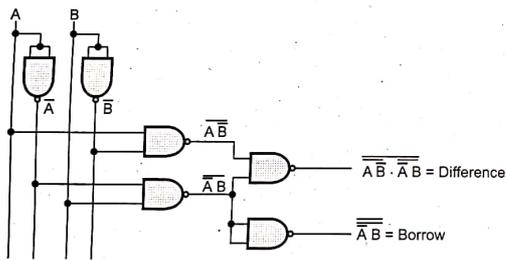


Fig. 4.15.3

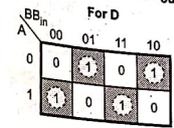
4.15.2 Full-Subtractor

A full-subtractor is a combinational circuit that performs a subtraction between two bits, taking into account borrow of the lower significant stage. This circuit has three inputs and two outputs. The three inputs are A, B and B_{in} , denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, D and B_{out} represent the difference and output borrow, respectively. The Table 4.15.2 shows the truth table for full-subtractor.

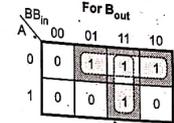
Inputs			Outputs	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 4.15.2 Truth table for full-subtractor

K-map simplification of D and B_{out}



$$D = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + AB B_{in}$$



$$B_{out} = \bar{A}B_{in} + \bar{A}B + BB_{in}$$

Fig. 4.15.4 Maps for full-subtractor

Logic diagram

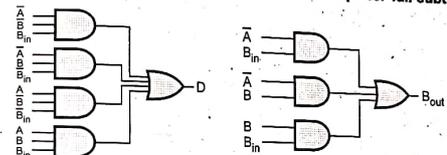
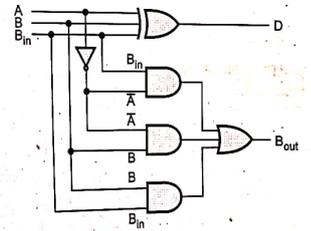


Fig. 4.15.5 Sum of product implementation of full-subtractor

The Boolean function for D (difference) can be further simplified as follows :

$$\begin{aligned} D &= \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + AB B_{in} \\ &= B_{in}(\bar{A}\bar{B} + AB) + \bar{B}_{in}(\bar{A}B + A\bar{B}) \\ &= B_{in}(A \odot B) + \bar{B}_{in}(A \oplus B) \\ &= B_{in}(\bar{A} \oplus \bar{B}) + \bar{B}_{in}(A \oplus B) \\ &= B_{in} \oplus (A \oplus B) \end{aligned}$$



With this simplified Boolean function Fig. 4.15.6 Implementation of full-subtractor circuit for full-subtractor can be implemented as shown in the Fig. 4.15.6.

A full subtractor can also be implemented with two half-subtractors and one OR gate, as shown in the Fig. 4.15.7. The difference output from the second half-subtractor is the exclusive-OR of B_{in} and the output of the first half-subtractor, which is same as difference output of full-subtractor.

The borrow output for circuit shown in Fig. 4.15.6 can be given as,

$$\begin{aligned} B_{out} &= \bar{A} B_{in} + \bar{A} B + B B_{in} \\ &= \bar{A} B_{in} (B + \bar{B}) + \bar{A} B + B B_{in} (A + \bar{A}) \\ &= \bar{A} B_{in} + \bar{A} \bar{B} B_{in} + \bar{A} B + AB B_{in} + \bar{A} \bar{B} B_{in} \\ &= \bar{A} B (B_{in} + 1 + B_{in}) + \bar{A} \bar{B} B_{in} + AB B_{in} \\ &= \bar{A} B + \bar{A} \bar{B} B_{in} + AB B_{in} \\ &= \bar{A} B + B_{in} (\bar{A} \bar{B} + AB) \\ &= \bar{A} B + B_{in} (A \oplus B) \end{aligned}$$

This Boolean function is same as borrow out of the full-subtractor. Therefore, we can implement full-subtractor using two half-subtractors and OR gate.

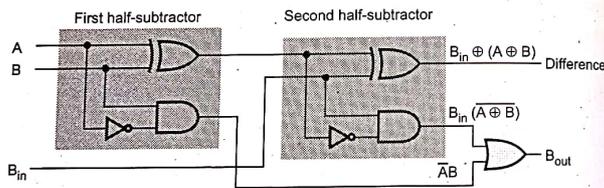


Fig. 4.15.7 Implementation of a full-subtractor with two half-subtractors and an OR gate

Review Questions

1. Define half subtractor and full subtractor.
2. Design a half-subtractor combinational circuit to produce the outputs. Difference and borrow.
3. Explain the operation of a half subtractor with the help of logic diagram and truth table.
4. Write the logic expressions for the difference and borrow of a half subtractor.
5. Realize full-subtractor using K-map.
6. Write an expression for borrow and difference in a full subtractor circuit.
7. Design full-subtractor circuit and draw necessary truth tables.
8. Explain how full subtractor can be designed by using two half subtractor circuits. Draw the circuit diagram.

4.16 BCD Arithmetic

The digital systems handle the decimal number in the form of Binary Coded Decimal numbers (BCD). A BCD adder is a circuit that adds two BCD digits and produces a sum digit also in BCD. Here, we will see the implementation of addition of BCD numbers.

To implement BCD adder we require :

- 4-bit binary adder for initial addition
- Logic circuit to detect sum greater than 9 and
- One more 4-bit adder to add 0110_2 in the sum if sum is greater than 9 or carry is 1.

The logic circuit to detect sum greater than 9 can be determined by simplifying the boolean expression of given truth table.

Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 4.16.1

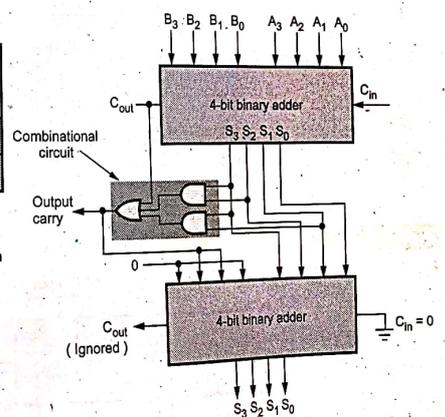
$Y = 1$ indicates sum is greater than 9. We can put one more term, C_{out} in the above expression to check whether carry is one. If any one condition is satisfied we add 6 (0110) in the sum.

With this design information we can draw the block diagram of BCD adder, as shown in the Fig. 4.16.1 (b).

$S_3 S_2 S_1 S_0$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

$Y = S_3 S_2 + S_3 S_1$

(a) K-map simplification



(b) Block diagram of BCD adder

Fig. 4.16.1

As shown in the Fig. 4.16.1 (b), the two BCD numbers, together with input carry, are first added in the top 4-bit binary adder to produce a binary sum.

When the output carry is equal to zero (i.e. when $\text{sum} \leq 9$ and $C_{\text{out}} = 0$) nothing (zero) is added to the binary sum. When it is equal to one (i.e. when $\text{sum} > 9$ or $C_{\text{out}} = 1$), binary 0110 is added to the binary sum through the bottom 4-bit binary adder.

The output carry generated from the bottom binary adder can be ignored, since it supplies information already available at the output-carry terminal.

Example 4.16.1 Design an 8-bit BCD adder using 4-bit binary adder.

Solution : To implement 8-bit BCD adder we have to cascade two 4-bit BCD adders. In cascade connection carry output of the lower position (digit) is connected as a carry input of the higher position (digit). Fig. 4.16.2 shows the block diagram of 8-bit BCD adder.

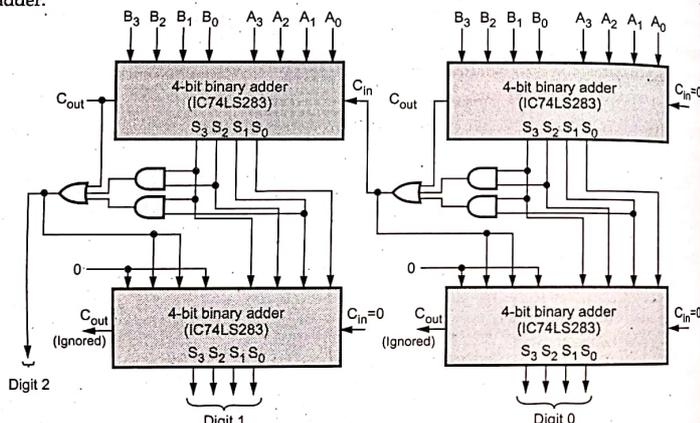


Fig. 4.16.2 8-bit BCD adder using IC 74283

Example 4.16.2 Design a BCD to Ex-3 code converter using binary parallel adder.

Solution :

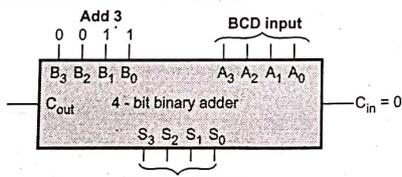


Fig. 4.16.3

Review Question

1. With a suitable block diagram explain the operation of BCD adder.

4.17 Carry Look Ahead Adder

GTU : Summer-15

One method of speeding up parallel addition process by eliminating inter stage carry delay is called look ahead-carry addition. This method utilizes logic gates to look at the lower-order bits of the augend and addend to see if a higher-order carry is to be generated. It uses two functions : carry generate and carry propagate.

Consider the circuit of the full-adder shown in Fig. 4.17.1. Here, we define two functions : carry generate and carry propagate.

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

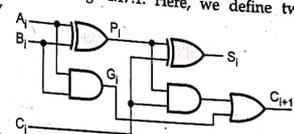


Fig. 4.17.1 Full-adder circuit

The output sum and carry can be expressed as

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

G_i is called a carry generate and it produces on carry when both A_i and B_i are one, regardless of the input carry. P_i is called a carry propagate because it is term associated with the propagation of the carry from C_i to C_{i+1} .

Now the Boolean function for the carry output of each stage can be written as follows.

$$C_2 = G_1 + P_1 C_1$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 (G_1 + P_1 C_1) = G_2 + P_2 G_1 + P_2 P_1 C_1$$

$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 (G_2 + P_2 G_1 + P_2 P_1 C_1)$$

$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_1$$

From the above Boolean function it can be seen that C_4 does not have to wait for C_3 and C_2 to propagate; in fact C_4 is propagated at the same time as C_2 and C_3 .

Review Question

1. Describe the working of look-ahead-carry adder.

GTU : Summer-15, Marks 7

4.18 Digital Comparator

GTU : Dec.-13, Summer-15, 18, Winter-15, 16

• Here, the combinational circuit compares numerical values of two binary numbers and result is presented by the outputs of combinational circuits.

Example 4.18.1 Design 2-bit comparator using gates.

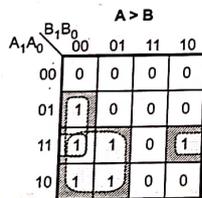
GTU : Summer-15, Marks 7

Solution : The truth table for 2-bit is given in Table 4.18.1.

Inputs				Outputs		
A ₁	A ₀	B ₁	B ₀	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table 4.18.1

K-map simplification



$A > B = A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{B}_1 + A_1 A_0 \bar{B}_0$

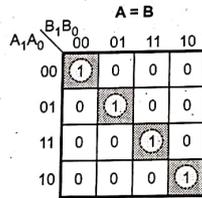
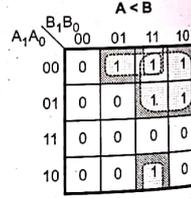


Fig. 4.18.1



$$\begin{aligned}
 (A = B) &= \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0 \\
 &= \bar{A}_1 \bar{B}_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0) + A_1 B_1 (A_0 B_0 + \bar{A}_0 \bar{B}_0) \\
 &= (A_0 \odot B_0) (A_1 \odot B_1) \\
 (A < B) &= \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 B_1 B_0 + \bar{A}_1 B_1
 \end{aligned}$$

Logic diagram

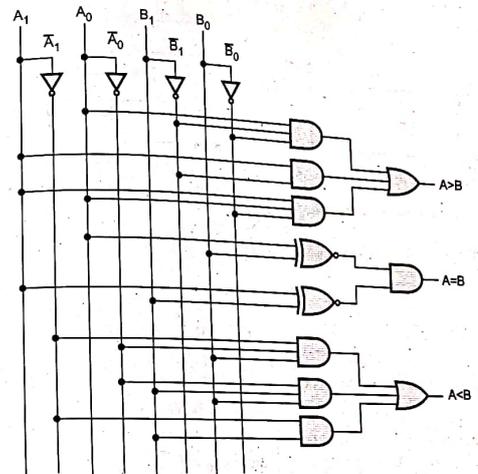


Fig. 4.18.2

Note We can also use outputs $A = B$ and $A < B$ to generate the third output $A > B$. This is illustrated in Fig. 4.18.3.



Fig. 4.18.3

Example 4.18.2 Design a 1-bit comparator using basic gates.

GTU : Winter-16, Summer-18, Marks 3

Solution : Consider two one bit number A and B. The truth table is as shown.

Inputs		Outputs		
A	B	$Y_{A=B}$	$Y_{A>B}$	$Y_{A<B}$
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

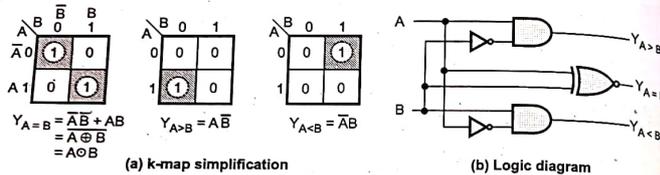


Fig. 4.18.4

Example 4.18.3 Design a 4-bit magnitude comparator.

Solution :

Comparison Algorithm

(A = B)

- Consider two 4-bit binary numbers A and B such that $A = A_3 A_2 A_1 A_0$ and $B = B_3 B_2 B_1 B_0$
- Two numbers are said to be equal when $A_3 = B_3, A_2 = B_2, A_1 = B_1$ and $A_0 = B_0$
- In binary, the equality of each pair of bits can be expressed logically with an exclusive-NOR function as $x_i = A_i B_i + \bar{A}_i \bar{B}_i$ for $i = 0, 1, 2, 3$

where $x_i = 1$ only if the pair of bits in position i are equal (i.e. if both are 1 or both are 0).

- Therefore, we can say that $A = B$, if $x_0 \cdot x_1 \cdot x_2 \cdot x_3 = 1$

(A > B) or (A < B)

- To determine whether A is greater or less than B, it is necessary to inspect the relative magnitudes of pairs of significant digits, starting from the most significant position.

- If the two digits of a pair are equal, we compare the next lower significant pair of digits. The comparison continues until a pair of unequal digits is reached.
- If corresponding digits of A is 1 and that of B is 0, we say that $A > B$.
- If corresponding digits of A is 0 and that of B is 1, we say that $A < B$.
- The sequential expression to determine whether $A > B$ or $A < B$ are as given below :

$$(A > B) = A_3 \bar{B}_3 + x_3 A_2 \bar{B}_2 + x_3 x_2 A_1 \bar{B}_1 + x_3 x_2 x_1 A_0 \bar{B}_0$$

$$(A < B) = \bar{A}_3 B_3 + x_3 \bar{A}_2 B_2 + x_3 x_2 \bar{A}_1 B_1 + x_3 x_2 x_1 \bar{A}_0 B_0$$

Logic diagram

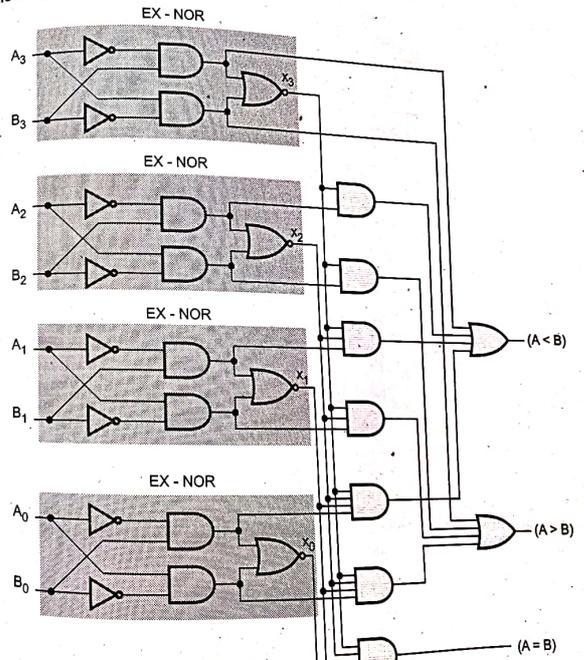


Fig. 4.18.5 Four-bit magnitude comparator

Fig. 4.18.6 shows the block diagram of an n-bit comparator. It receives two n-bit numbers A and B as inputs and the outputs are A > B, A = B and A < B. Depending upon the relative magnitudes of the two number, one of the outputs will be high.

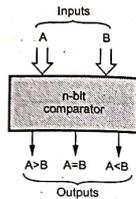
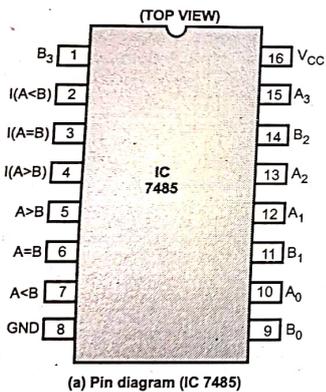
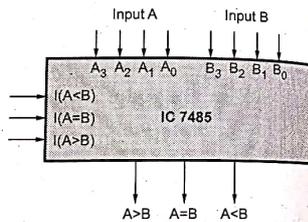


Fig. 4.18.6 Block diagram of n-bit comparator

IC 7485 is a 4-bit comparator. It can be used to compare two 4-bit binary words by grounding I (A < B), and I (A > B), and connector input I (A = B) to V_{CC}. These ICs, can be cascaded to compare words of almost any length. Its 4-bit inputs are weighted (A₀ - A₃) and (B₀ - B₃), where A₃ and B₃ are the most significant bits.



(a) Pin diagram (IC 7485)



(b) Block diagram (IC 7485)

Fig. 4.18.7

Fig. 4.18.7 shows the logic symbol and pin diagram of IC 7485. The operation of IC 7485 is described in the function table, showing all possible logic conditions.

Comparing Inputs A B	Cascading Inputs			Outputs		
	I(A > B)	I(A = B)	I(A < B)	A > B	A = B	A < B
A > B	X	X	X	1	0	0
A = B	1	0	0	1	0	0
	X	1	X	0	1	0
	0	0	1	0	0	1
	0	0	0	1	0	0
A < B	X	X	X	0	0	1

Table 4.18.2 Function table for IC 7485

Example 4.18.4 Design an 8-bit comparator using two 7485 ICs.

Solution : Fig. 4.18.8 shows an 8-bit comparator using two 7485 ICs.

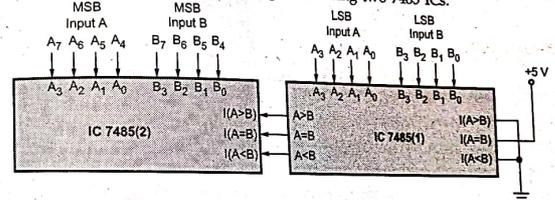


Fig. 4.18.8 8-bit comparator

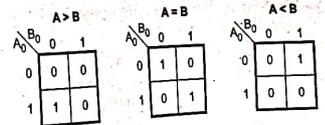
Example 4.18.5 Design a 5-bit magnitude comparator using comparator IC 7485.

Solution :

Truth Table

A ₀	B ₀	I(A > B)	I(A = B)	I(A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

K-map simplification



$$(A > B) = A_0 \bar{B}_0$$

$$(A = B) = \bar{A}_0 \bar{B}_0 + A_0 B_0 = A_0 \oplus B_0$$

$$(A < B) = \bar{A}_0 B_0$$

Implementation

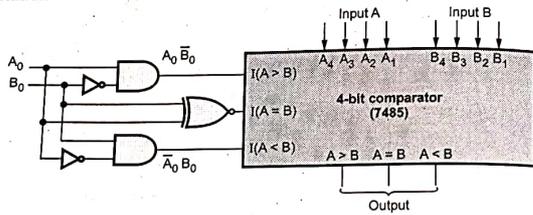


Fig. 4.18.9

Example 4.18.6 Explain how you will build a 24-bit magnitude comparator using 7485s.

Solution : By cascading six 4-bit comparator ICs as shown in Fig. 4.18.10 we can build a 24-bit magnitude comparator. (Refer Fig. 4.18.10 on next page).

Review Questions

1. What is magnitude comparator ?
2. Explain a 2-bit magnitude comparator with gate level circuit and truth table.
3. Draw the schematic of a magnitude comparator and give its truth table.
4. Write a note on IC 7485.
5. With logic circuit explain the working of 4-bit magnitude comparator. **GTU : Dec-13, Marks 7**
6. Draw and explain in brief pin diagram of 7485 four-bit magnitude comparator. **GTU : Winter-15, Marks 3**

4.19 Parity Generator / Checker

GTU : May-14, Summer-15, 18

- A parity bit is used for the purpose of detecting errors during transmission of binary information.
- A parity bit is an extra bit included with a binary message to make the number of 1s either odd or even.
- The message, including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted.

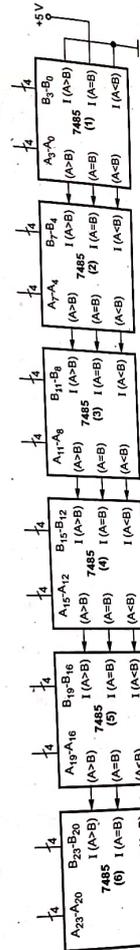


Fig. 4.18.10 - 24-bit comparator

- The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.
- In even parity, the added parity bit will make the total number of 1s an even amount.
- In odd parity, the added parity bit will make the total number of 1s an odd amount.
- Table 4.19.1 shows the 3-bit message with even parity and odd parity.

3-bit message			Odd parity bit	Even parity bit
A	B	C		
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Table 4.19.1 Parity generator truth table for even and odd parity

Example 4.19.1 Design an even parity generator with 3 message bits.

GTU: Summer-15, 18, Marks 7

Solution : Refer Table 4.19.1.

$$\begin{aligned}
 P &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC) \\
 &= \bar{A}(B \oplus C) + A(B \odot C) \\
 &= \bar{A}(B \oplus C) + A(\overline{B \oplus C}) = A \oplus (B \oplus C)
 \end{aligned}$$

K-map simplification

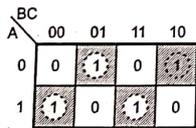


Fig. 4.19.1 (a) Simplification of even parity bit

Logic diagram

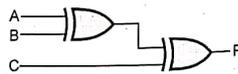


Fig. 4.19.1 (b)

Parity checker

- The three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit.
- The parity checker circuit checks for possible errors in the transmission.
- Since the information was transmitted with even parity, the four bits received must have an even number of 1s. An error occurs during the transmission if the four bits received have an odd number of 1s, indicating that one bit has changed in value during transmission.

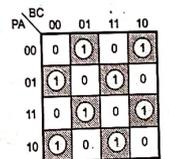
Decimal equivalent	Four bits received			Parity error check	
	P	A	B		C
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

Table 4.19.2 Truth table for even parity checker

- The output of the parity checker, is denoted by PEC (Parity Error Check). It will be equal to 1, if an error occurs, that is, if the four bits received have an odd number of 1s. The Table 4.19.2 shows the truth table for the even parity checker.

$$\begin{aligned}
 PEC &= \bar{P}\bar{A}(\bar{B}C + B\bar{C}) + \bar{P}A(\bar{B}\bar{C} + BC) \\
 &+ P\bar{A}(\bar{B}C + B\bar{C}) + PA(\bar{B}\bar{C} + BC) \\
 &= \bar{P}\bar{A}(B \oplus C) + \bar{P}A(\overline{B \oplus C}) + P\bar{A}(B \oplus C) + PA(\overline{B \oplus C}) \\
 &= (\bar{P}\bar{A} + PA)(B \oplus C) \\
 &+ (\bar{P}A + P\bar{A})(\overline{B \oplus C}) \\
 &= (\bar{P} \oplus A)(B \oplus C) + (P \oplus A)(\overline{B \oplus C}) = (P \oplus A) \oplus (B \oplus C)
 \end{aligned}$$

K-map simplification



PEC = (P⊕A)⊕(B⊕C)
Fig. 4.19.2 (a)

Logic diagram

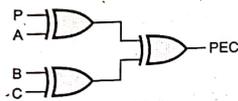


Fig. 4.19.2 (b)

Example 4.19.2 Implement an even parity checker for a 4-bit data, using 8 : 1 mux and inverters.

Solution : Refer Table 4.19.2 for the truth table of 4-bit even parity checker.

Implementation Table

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
\bar{P}	0	1	2	3	4	5	6	7
P	8	9	10	11	12	13	14	15
	P	\bar{P}	\bar{P}	P	\bar{P}	P	P	\bar{P}

Implementation

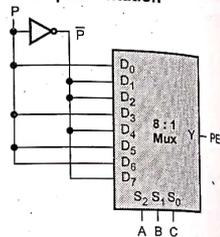


Fig. 4.19.3

IC 74180 : Parity Generator/Checker

The 74180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both even and odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

The Fig. 4.19.4 (a, b) shows pin diagram and logic diagram for 74180.

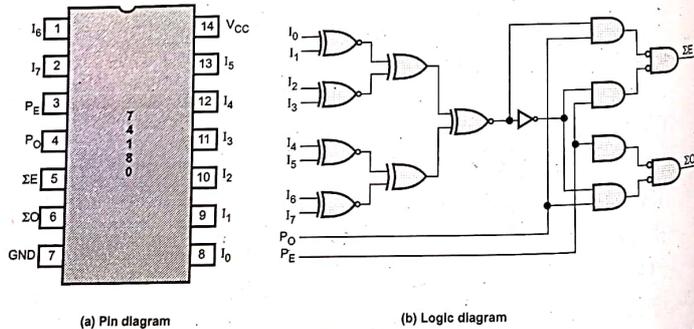


Fig. 4.19.4

Table 4.19.3 shows the function table for 74180

Number of HIGH data Inputs (I ₀ - I ₇)	Inputs		Outputs	
	P _E	P _O	ΣE	ΣO
Even	1	0	1	0
Odd	1	0	0	1
Even	0	1	0	1
Odd	0	1	1	0
X	1	1	0	0
X	0	0	1	1

Table 4.19.3 Function table for 74180

As shown in the Table 4.19.3, true active-HIGH or true active-LOW parity can be generated at both the even or odd outputs. True active-HIGH parity is established with Even parity enable input (P_E) set HIGH and the Odd parity enable input (P_O) set LOW. True active LOW parity is established when P_E is LOW and P_O is HIGH. When both are enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8-bits plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active-HIGH parity, the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs as shown in the Fig. 4.19.5 (a). To check for true active-LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs, as shown in the Fig. 4.19.5 (b).

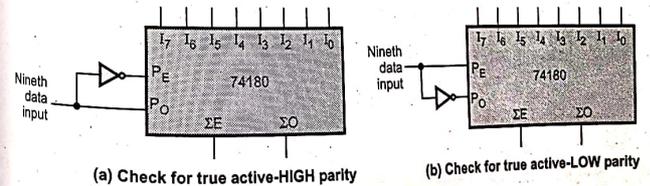


Fig. 4.19.5

Expansion to larger word sizes is accomplished by serially cascading the 74180 in 8-bit increments. The even and odd parity outputs of the first stages are connected to the corresponding P_E and P_O inputs, respectively, of the succeeding stage, as shown in the Fig. 4.19.6.

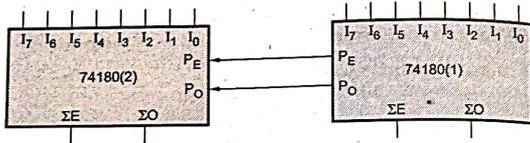


Fig. 4.19.6 Expansion to the larger word

Review Questions

1. Write a note on parity generator / parity checker. GTU : May-14, Marks 5
2. Implement an odd parity checker for a 4-bit data, using 8 : 1 mux and inverters.
3. Design 16-bit odd parity checker using 74180 ICs.
4. Design 3-bit even parity generator circuit. GTU : Summer-15, 18, Marks 7

4.20 Code Converters

GTU : May-12, 13

There is a wide variety of binary codes used in digital systems. Some of these codes are Binary-Coded-Decimal (BCD), Excess-3, Gray and so on. Many times it is required to convert one code to another.

Let us see the procedure to design code converters :

- Step 1 :** Write the truth table showing the relationship between input code and output code.
- Step 2 :** For each output code bit determine the simplified Boolean expression using K-map.
- Step 3 :** Realize the code converter using logic gates.

Illustrative Examples

Example 4.20.1 Design a 4-bit binary to BCD converter.

Step 1 : Form the truth table relating binary and BCD code.

Input code : Binary code : $B_3 B_2 B_1 B_0$ (B_0 LSB)

Output code : BCD (Decimal) code : $D_4 D_3 D_2 D_1 D_0$ (D_0 LSB)

Binary code				BCD code				
B_3	B_2	B_1	B_0	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0
0	1	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	1
1	0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	0	1
1	1	0	0	1	0	0	1	0
1	1	0	1	1	0	0	1	1
1	1	1	0	1	0	1	0	0
1	1	1	1	1	0	1	0	1

Table 4.20.1 Truth table for binary to BCD conversion

Step 2 : K-map simplification for each BCD output

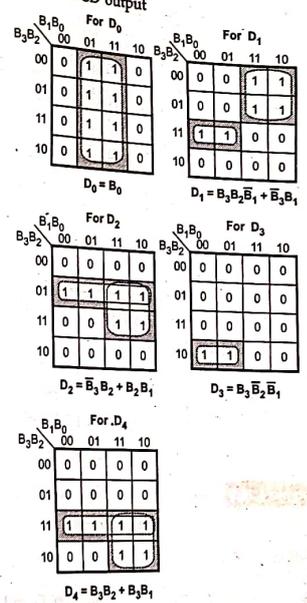


Fig. 4.20.1

Step 3 : Realization of code converter

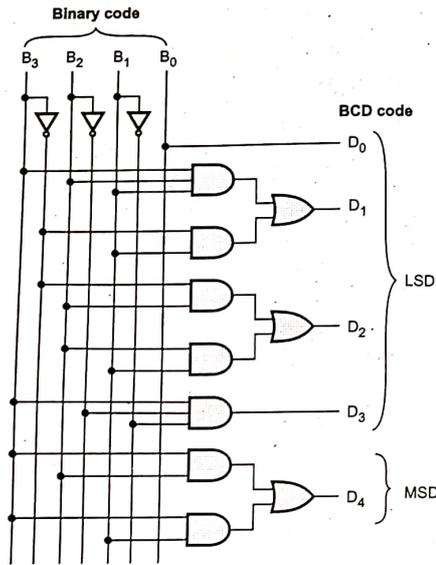


Fig. 4.20.2 Binary to BCD converter

Example 4.20.2 Design a logic circuit to convert the 8421 BCD to Excess-3 code.

GTU : May-13, Marks 7

Solution :

Step 1 : Form the truth table relating BCD and Excess-3 code

Excess-3 code is a modified form of a BCD number. The Excess-3 code can be derived from the natural BCD code by adding 3 to each coded number. For example, decimal 12 can be represented in BCD as 0001 0010. Now adding 3 to each digit we get Excess-3 code as 0100 0101 (12 in decimal). With this information the truth table for BCD to Excess-3 code converter can be determined as shown in Table 4.20.2.

Input code : BCD code : $D_3 D_2 D_1 D_0$ (D_0 LSB)

Output code : Excess-3 code : $E_3 E_2 E_1 E_0$ (E_0 LSB)

Decimal	D_3	D_2	D_1	D_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 4.20.2

Step 2 : K-map simplification for each Excess-3 code output.

For E_3

D_3D_2	D_1D_0 00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$\therefore E_3 = D_3 + D_2(D_0 + D_1)$

For E_2

D_3D_2	D_1D_0 00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	X	X	X	X
10	0	1	X	X

$\therefore E_2 = D_2\bar{D}_1\bar{D}_0 + \bar{D}_2(D_0 + D_1)$

For E_1

D_3D_2	D_1D_0 00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	X	X	X	X
10	1	0	X	X

$E_1 = \bar{D}_1\bar{D}_0 + D_1D_0 = D_1 \odot D_0$

For E_0

D_3D_2	D_1D_0 00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$E_0 = \bar{D}_0$

Fig. 4.20.3

Step 3 : Realization of code converter.

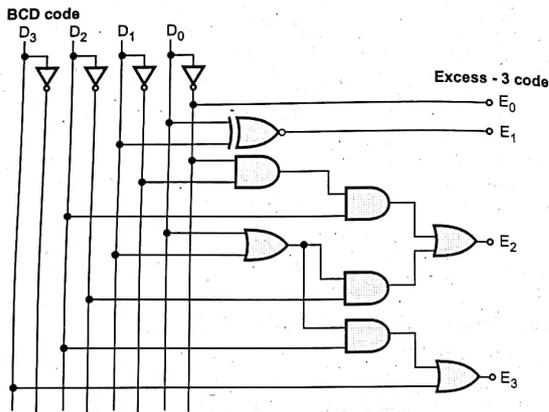


Fig. 4.20.4 BCD to excess-3 code converter

Example 4.20.3 Design a logic circuit to convert BCD to gray code.

Solution :

Step 1 : Form the truth table relating BCD and gray code.

Input code : BCD code : $D_3 D_2 D_1 D_0$ (D_0 LSB)

Output code : Gray code : $G_3 G_2 G_1 G_0$ (G_0 LSB)

Table 4.20.3 shows truth table for BCD to gray code converter.

BCD code				Gray code			
D_3	D_2	D_1	D_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0

Table 4.20.3 Truth table for BCD to gray code converter

Step 2 : K-map simplification

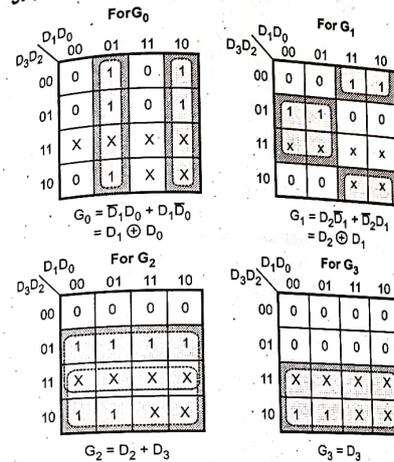


Fig. 4.20.5

Step 3 : Realization of code converter

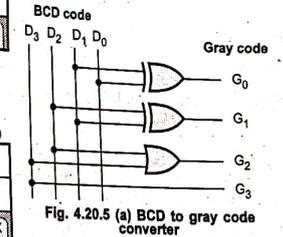


Fig. 4.20.5 (a) BCD to gray code converter

Example 4.20.4 Design and implement a 8421 to Gray code converter. Realize the converter using only NAND gates. GTU : May-12, Marks 5

Solution :

Step 1 : Form the Truth table relating 8421 binary code and Gray code

Input code : Binary code : $B_3 B_2 B_1 B_0$

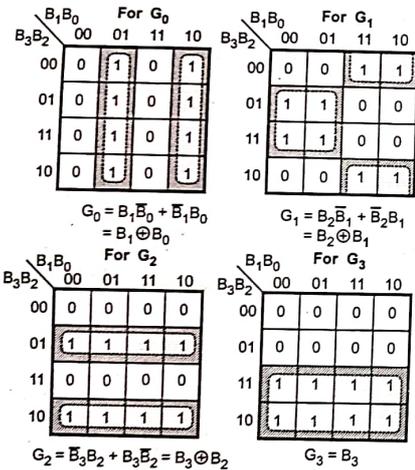
Output code : Gray code : $G_3 G_2 G_1 G_0$

Decimal	Binary code				Gray code			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1

7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Table 4.20.4

Step 2 : K-map simplification for each gray code output



$G_0 = B_1\bar{B}_0 + \bar{B}_1B_0 = B_1 \oplus B_0$

$G_1 = B_2\bar{B}_1 + \bar{B}_2B_1 = B_2 \oplus B_1$

$G_2 = \bar{B}_3B_2 + B_3\bar{B}_2 = B_3 \oplus B_2$

$G_3 = B_3$

Fig. 4.20.6

Step 3 : Realization of code converter using XOR-gates

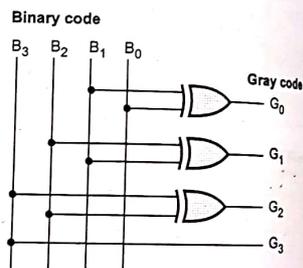


Fig. 4.20.7 Binary to gray code converter

Step 4 : Realization of code converter using NAND gates

For this converter we have derived the Boolean expressions for each gray code output in the Sum Of Product (SOP) form. We can implement SOP expression using AND-OR logic or NAND-NAND logic. Let us see the implementation of code converter using NAND-NAND logic.

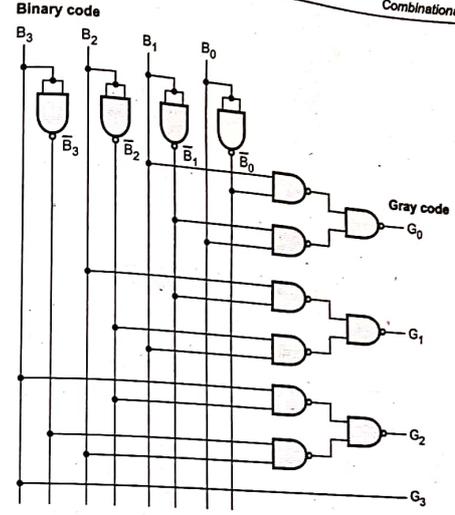


Fig. 4.20.8 Binary to Gray code converter

Example 4.20.5 Design a Gray to BCD code converter.

Solution : The Table 4.20.5 shows truth table for gray to BCD code converter.

Gray code				BCD code				
G ₃	G ₂	G ₁	G ₀	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	1	0	0	0	1	0
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	0	0
0	1	1	1	0	0	1	0	1
0	1	0	1	0	0	1	1	0
0	1	0	0	0	0	1	1	1

1	1	0	0	0	1	0	0	0
1	1	0	1	0	1	0	0	1
1	1	1	1	1	0	0	0	0
1	1	1	0	1	0	0	0	1
1	0	1	0	1	0	0	1	0
1	0	1	1	1	0	0	1	1
1	0	0	1	1	0	1	0	0
1	0	0	0	1	0	1	0	1

Table 4.20.5 Gray to BCD code converter

Kmap-simplification

For D ₀				For D ₁				For D ₂									
G ₃ G ₂	G ₁ G ₀	00	01	11	10	G ₃ G ₂	G ₁ G ₀	00	01	11	10	G ₃ G ₂	G ₁ G ₀	00	01	11	10
00		0	1	0	1			0	0	1	1			0	0	0	0
01		1	0	1	0			1	1	0	0			1	1	1	1
11		0	1	0	1			0	0	0	0			0	0	0	0
10		1	0	1	0			0	0	1	1			1	1	0	0

$$D_0 = \bar{G}_3\bar{G}_2\bar{G}_1G_0 + \bar{G}_3\bar{G}_2G_1\bar{G}_0 + \bar{G}_3G_2\bar{G}_1\bar{G}_0 + \bar{G}_3G_2G_1G_0 + G_3\bar{G}_2\bar{G}_1\bar{G}_0 + G_3\bar{G}_2G_1\bar{G}_0 + G_3G_2\bar{G}_1\bar{G}_0 + G_3G_2G_1G_0$$

$$= \bar{G}_3\bar{G}_2(\bar{G}_1\oplus G_0) + \bar{G}_3G_2(\bar{G}_1\oplus G_0) + G_3\bar{G}_2(\bar{G}_1\oplus G_0) + G_3G_2(\bar{G}_1\oplus G_0)$$

$$= (\bar{G}_3\oplus G_3)(\bar{G}_1\oplus G_0) + (G_3\oplus G_3)(\bar{G}_1\oplus G_0)$$

$$= G_3\oplus G_2\oplus G_1\oplus G_0$$

$$D_1 = \bar{G}_3G_2\bar{G}_1 + \bar{G}_2G_1$$

$$D_2 = \bar{G}_3G_2 + G_3\bar{G}_2\bar{G}_1$$

For D ₃				For D ₄							
G ₃ G ₂	G ₁ G ₀	00	01	11	10	G ₃ G ₂	G ₁ G ₀	00	01	11	10
00		0	0	0	0			0	0	0	0
01		0	0	0	0			0	0	0	0
11		1	1	0	0			0	0	1	1
10		0	0	0	0			1	1	1	1

$$D_3 = G_3G_2\bar{G}_1$$

$$D_4 = G_3\bar{G}_2 + G_3G_1$$

Fig. 4.20.9

Logic Diagram

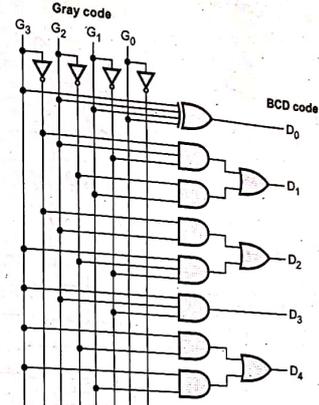


Fig. 4.20.10

Example 4.20.6 Design 4 bit excess-3 to BCD code converter and implement using logic gates.

Solution : 4-bit excess - 3 to BCD code converter :

Decoder	Inputs				Outputs			
	E ₃	E ₂	E ₁	E ₀	D ₃	D ₂	D ₁	D ₀
3	0	0	1	1	0	0	0	0
4	0	1	0	0	0	0	0	1
5	0	1	0	1	0	0	1	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	0	1	0	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	1	1
11	1	0	1	1	1	0	0	0
12	1	1	0	0	1	0	0	1

K-map simplification

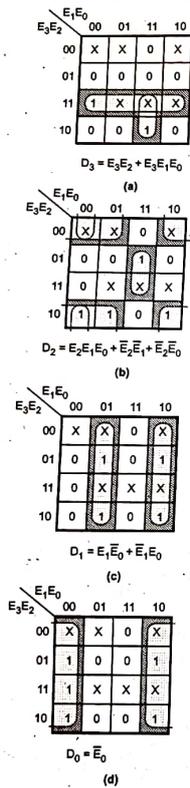


Fig. 4.20.11

Example for Practice

Example 4.20.7 : Design a logic circuit to convert gray code to binary code.

(Ans. : $B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$ $B_1 = G_3 \oplus G_2 \oplus G_1$
 $B_2 = G_3 \oplus G_2$ $B_3 = G_3$)

Implementation using logic gates :

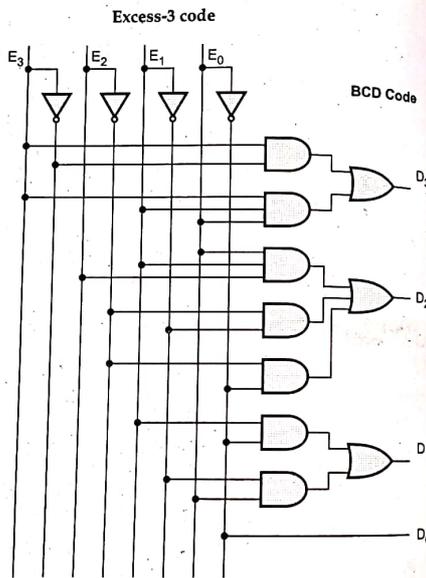


Fig. 4.20.12

4.21 ALU and Elementary ALU Design

4.21.1 Design of Arithmetic Unit

The Arithmetic and Logic Unit (ALU) performs all the necessary adding, subtracting, and logical operations. It requires one or two operands upon which to operate arithmetic instructions are realized. Simple ALUs that perform fixed point addition and subtraction, as well as word based logic operations, can be realized by combinational circuits. ALUs that also perform multiplication and division can be constructed using circuits discussed in preceding sections for them. Let us see the simple ALU design with combinational circuits.

The basic component of the arithmetic section of a simplest ALU is a parallel adder. A parallel adder can be constructed using number of full-adder circuits connected in cascade. Let us see the implementation of various functions of arithmetic unit using parallel adder. Table 4.21.1 shows these implementations.

Sr. No	Function	Implementation
1.	$Y \leftarrow A$	
2.	$Y \leftarrow A + 1$	
3.	$Y \leftarrow A + B$	

4.	$Y \leftarrow A + B + 1$	
5.	$Y \leftarrow A + \bar{B}$	
6.	$Y = A + \bar{B} + 1$	
7.	$Y = A - 1$	
8.	$Y = A$	

Table 4.21.1 Implementation of basic arithmetic operations

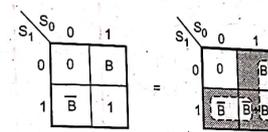
Looking at Table 4.21.1 we can realize that by selecting proper B and C_{in} inputs we can implement basic arithmetic operations. There are four possible B inputs: true, complement, all 1s and all 0s and two possible C_{in} inputs 0 and 1.

Referring Table 4.21.2, we can write truth table for B input with respect to S_0 and S_1 signals as follows :

S_1	S_0	B'
0	0	0
0	1	B
1	0	\bar{B}
1	1	1

Note - B' indicates modified B input

Table 4.21.2 Truth table



$\therefore B' = S_1 \bar{B} + S_0 B$

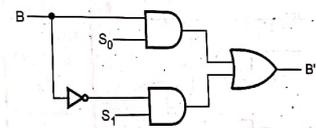


Fig. 4.21.1 K-map simplification and logic diagram of modified B input

K-map simplification

Using the logic diagram of modified B input we can draw the logic diagram of arithmetic circuit, as shown in Fig. 4.21.2.

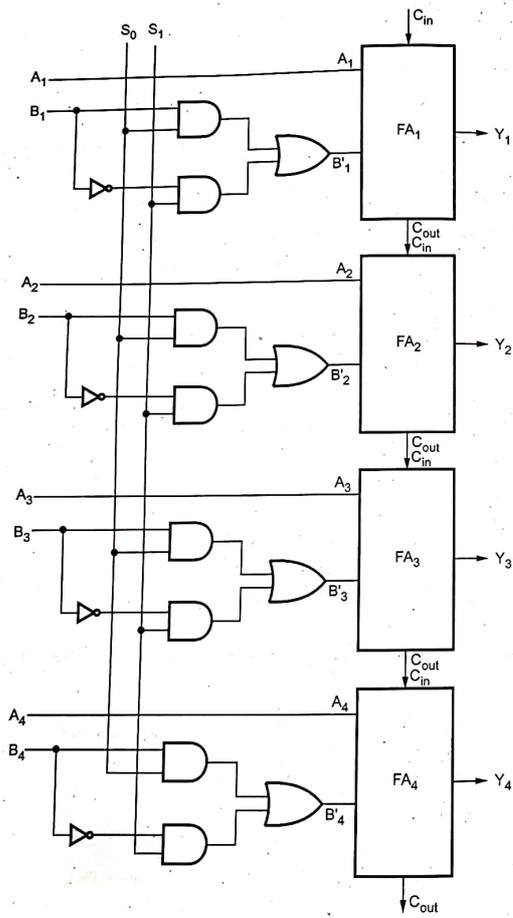


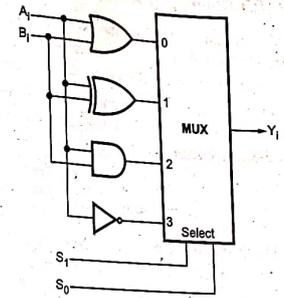
Fig. 4.21.2 Logic diagram of arithmetic circuit

4.21.2 Design of Logic Circuit

The design of logic circuit is comparatively simple than the design of arithmetic circuit. Fig. 4.21.3 shows the function table and the logic diagram for logic circuit.

S_1	S_0	Output	Function
0	0	$Y = A \vee B$	OR
0	1	$Y = A \oplus B$	XOR
1	0	$Y = A \wedge B$	AND
1	1	$Y = \bar{A}$	NOT

a) Function table



b) Logic diagram

Fig. 4.21.3 Logic circuit

Note : The logic diagram shown in Fig. 4.21.3 (b) is repeated n times for n-bit logic circuit. Therefore, inputs A and B, and output Y are shown with subscript i, where $i = 1, 2, \dots, n$.

We have seen the design of arithmetic and logic circuits for a simple ALU. By combining both circuits with the help of multiplexer we can get the arithmetic and logic circuit, as shown in the Fig. 4.21.4. When S (mode select) is 0, the output of arithmetic circuit is transferred as a final output; otherwise the output of logic circuit is transferred as a final output.

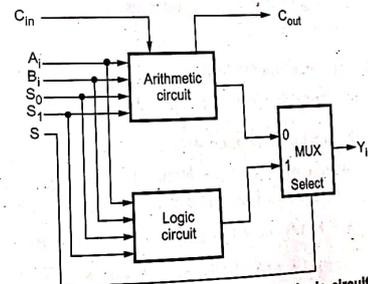


Fig. 4.21.4 Combining arithmetic and logic circuits

4.21.3 Combining Arithmetic and Logic Unit

The design of ALU in above mentioned way is the simplest and straight forward. A more efficient ALU can be implemented if we investigate the possibility of generating logic operations in an already available arithmetic circuit.

We know that carry input is not required in the logic circuits. Hence, when logic operation is selected ($S = 1$), the carry input must be zero. This gives us the output sum in full-adder circuit as

$$Y_i = A_i \oplus B_i \oplus 0 \quad \because C_{in} = 0$$

$$= A_i \oplus B_i$$

Using this relation we have to change the outputs as shown in Table 4.21.3.

S	S ₁	S ₀	A _i '	B _i '	C _i	F _i = A _i ⊕ B _i	Operation	Required operation
1	0	0	A _i	0	0	Y _i = A _i	Transfer A	OR
1	0	1	A _i	B _i	0	Y _i = A _i ⊕ B _i	XOR	XOR
1	1	0	A _i	\bar{B}_i	0	Y _i = A _i ⊙ B _i	X-NOR	AND
1	1	1	A _i	1	0	Y _i = \bar{A}_i	NOT	NOT

Table 4.21.3 Excitation table for ALU

Let us see, how we can change these outputs.

Case 1 : S₁ S₀ = 00 Required operation OR

Here, Y_i = A_i. To make Y_i = A_i ∨ B_i, we must change the input A_i to each full adder circuit from A_i to A_i + B_i.

Case 2 : S₁ S₀ = 01 Required operation XOR

Here, Y_i = A_i ⊕ B_i. Hence change is not required.

Case 3 : S₁ S₀ = 10 Required operation AND

Here, Y_i = A_i ⊙ B_i and we want Y_i = A_i B_i. Let us investigate the possibility of ORing each input A_i with some boolean function K_i. Therefore, now

$$Y_i = (A_i + K_i) \oplus \bar{B}_i = (A_i + K_i) B_i + (\overline{A_i + K_i}) \bar{B}_i$$

$$= A_i B_i + K_i B_i + (\bar{A}_i \cdot \bar{K}_i) \bar{B}_i = A_i B_i + K_i B_i + \bar{A}_i \bar{K}_i \bar{B}_i$$

To have Y_i = A_i B_i, terms 2 and 3 must be 0. i.e. K_i B_i + $\bar{A}_i \bar{K}_i \bar{B}_i = 0$. This result can be obtained when K_i = \bar{B}_i . This is illustrated as follows :

When

$$K_i = \bar{B}_i$$

$$Y_i = A_i B_i + \bar{B}_i B_i + \bar{A}_i \bar{B}_i \bar{B}_i$$

$$= A_i B_i + \bar{B}_i B_i + \bar{A}_i B_i \bar{B}_i$$

$$= A_i B_i$$

$$\because \bar{B}_i B_i = 0$$

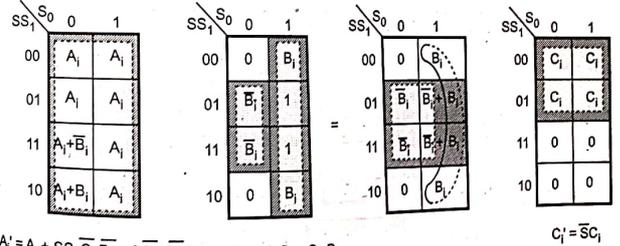
Case 4 : S₁ S₀ = 11 Required operation NOT

Here, Y_i = \bar{A}_i . Hence change is not required. With above changes we can write excitation table for ALU as shown in Table 4.21.4.

S	S ₁	S ₀	C _i '	A _i '	B _i '
0	0	0	C _i	A _i	0
0	0	1	C _i	A _i	B _i
0	1	0	C _i	A _i	\bar{B}_i
0	1	1	C _i	A _i	1
1	0	0	0	A _i + B _i	0
1	0	1	0	A _i	B _i
1	1	0	0	A _i + \bar{B}_i	\bar{B}_i
1	1	1	0	A _i	1

Table 4.21.4 Excitation table for ALU

K-map simplification for A_i', B_i' and C_i'



$$A_i' = A_i + S S_1 \bar{S}_0 \bar{B}_i + S S_1 \bar{S}_0 B_i$$

$$B_i' = S_1 \bar{B}_i + S_0 B_i$$

$$C_i' = \bar{S} C_i$$

Fig. 4.21.5

Therefore, Boolean expressions for ALU inputs can be given as

$$A_i' = A_i + S S_1 \bar{S}_0 \bar{B}_i + S S_1 \bar{S}_0 B_i$$

$$B_i' = S_1 \bar{B}_i + S_0 B_i$$

$$C_i' = \bar{S} C_i$$

When $S = 1$, these equations reduce to

$$\begin{aligned} A_i' &= A_i \\ B_i' &= S_i \bar{B}_i + S_0 B_i \\ C_i' &= 0 \end{aligned}$$

which are the functions of arithmetic circuits. Fig. 4.21.6 shows the final ALU circuit. It shows only first two stages, but can easily be extended to more stages.

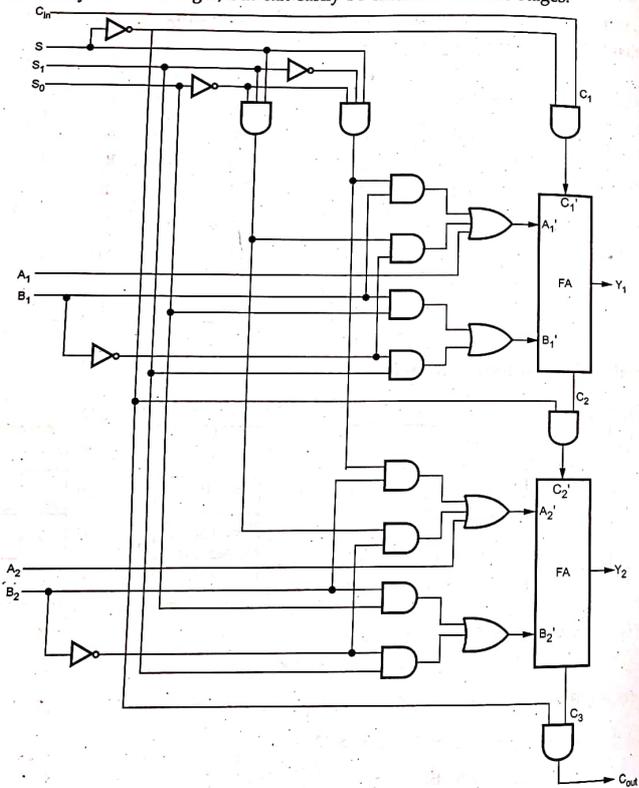


Fig. 4.21.6 Logic diagram of arithmetic logic unit (ALU)

Review Questions

1. What is ALU? What is its function?
2. Explain the arithmetic logic unit.

Oral Questions and Answers

- Q.1** Name the two basic types of Boolean expressions.
Ans.: There are two basic types of Boolean expressions are :
 • Sum of product Form (SOP) and
 • Product of Sum Form (POS)
- Q.2** Name the two canonical forms for Boolean algebra.
Ans.: Standard SOP and standard POS forms.
- Q.3** Express $F = BC' + AC$ in a canonical SOP form.
Ans.: $F = B\bar{C} + AC = (A + \bar{A})B\bar{C} + A C(B + \bar{B})$
 $= A B\bar{C} + \bar{A} B\bar{C} + A B C + A \bar{B} C$
- Q.4** What is variable mapping?
Ans.: Representing the minterms of the sum of product expression in the Karnaugh-map of appropriate variables is known as variable mapping.
- Q.5** What code is used to label the row headings and column heading of K-map and why?
Ans.:
 • Gray code is used to label the rows and columns of K-map.
 • In case of Gray code, only one variable changes between two consecutive number. This is useful in grouping pair, quad, or octets in k-maps and thus eliminating variables in the final expression. Hence, Gray code is used to label the rows and columns of K-map.
- Q.6** What are don't care conditions and incompletely specified functions?
Ans.: Sometimes, while designing a digital circuit, certain conditions of input are of no use. Consider an example of BCD input for a seven segment display. In this case, inputs from 0 through 9 are valid inputs. Thus, rest of the inputs from 10 through 15 do not signify anything at the output side. The outputs for which inputs are not specified are called don't care outputs. The Boolean function in which don't care outputs exists is called incomplete Boolean function or incompletely specified functions.

Q.7 Distinguish between completely specified function and incompletely specified function.

Ans. :

Sr. No.	Completely specified function	Incompletely specified function
1.	All input conditions occur.	Certain input conditions never occur.
2.	Each output corresponding to input conditions is defined.	Outputs corresponding to non-occurring input conditions are undefined.
3.	Each output has certain logical value, either 0 or 1.	Undefined output doesn't have certain logical value, but it is indicated by 'x' or 'd' in truth tables.
4.	In expression, $f(A, B, C) = \sum m(0, 1, 3, 5, 6)$ $= \pi M(1, 4, 7)$	In expression, $f(A, B, C) = \sum m(0, 1, 3) + d(5, 6)$ $= \pi M(2, 4, 7) + d(5, 6)$ Here outputs corresponding to terms 5 and 6 are assumed to be undefined ('x' or 'd') called as 'don't care'.

Q.8 What are prime implicants ?

Ans. : All the implicants of a function determined using a Karnaugh map are called prime implicants.

Q.9 Write the names of universal gates.

Ans. : Universal gates are : NAND gate and NOR gate.

Q.10 Why are NAND and NOR gates known as Universal gates ?

Ans. : NAND and NOR are the gates that can be used alone to generate remaining gates such as NOT, AND and OR. Thus, with only any of the two gates, we can implement the logic circuit. Hence, they are called Universal gates.

Q.11 How can a NAND gate be used as an inverter ?

Ans. :

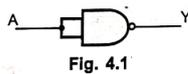


Fig. 4.1

Q.12 Define a combinational logic circuit. Give an example.

Ans. : When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called 'combinational logic circuit'.

A combinational circuit consists of input variables, logic gates and output variables. For example, consider following Boolean expression,

$$Y = AB + BC + AC$$

The combinational logic circuit for this would require 3 AND gates and 1 OR gate as shown in Fig. 4.2.

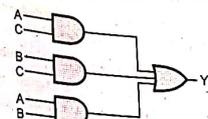


Fig. 4.2

Q.13 Define half adder and full adder.

Ans. :

1) Half adder : The logic circuit which performs the arithmetic sum of two bits is called a half adder.

2) Full adder : The logic circuit which performs the arithmetic sum of 3 bits (bit 1 : input 1, bit 2 : input 2, bit 3 : carry from the previous addition) is called a full adder.

Q.14 Define half subtractor and full subtractor.

Ans. :

1) Half subtractor : It is a combinational circuit that subtracts two bits and produces their difference and borrow.

2) Full subtractor : It is a combinational circuit that performs a subtraction between 2 bits. It also takes into account borrow of the lower significant stage.

Q.15 What is a data selector ? or What is multiplexer ? or Why is MUX called as data detector ?

Ans. :

- Multiplexer is a digital switch. Particularly, it has 2^n input lines and n selection lines whose bit combinations determine which input line is selected and routed onto available only single output line.

- Hence, multiplexer is a selector of one out of several data sources available at its input lines, to connect it to output line. Simply it is a 'many into one' device and also called 'data selector'.

Q.16 What is decoder ?

Ans. : A decoder is a multiple - input, multiple-output logic circuit which converts coded inputs into coded outputs, where the input and output codes are different. In a binary decoder n-inputs produce 2^n outputs. Usually, a decoder is provided with enable inputs to activate decoded output.

Q.17 What is binary decoder ?

Ans. : A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n outputs lines.

Q.18 What do you mean by encoder ?

Ans. : An encoder is a digital circuit that performs the inverse operation of a decoder. Encoder has 2^n (or fewer) input lines and n output lines. Encoder has enable inputs to activate encoded outputs.

Q.19 Write a short note on priority encoder. OR What is a priority encoder ?

Ans. : A priority encoder is an encoder circuit in which if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_0	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Table 4.1 Truth table of 4-bit priority encoder

- As per the table, when D_3 is high, regardless of other inputs, the output is 11.
- D_2 has next priority, thus, with $D_2 = 1$ and $D_3 = 0$, output will be 10.
- Output for D_1 is generated only if higher priority inputs are 0, and so on.
- If all inputs are 0, two outputs of the circuit are not used.

Q.20 What do you mean by comparator ? OR Write a short note on 1-bit comparator.

Ans. : It is a special combinational circuit designed primarily to compare the relative magnitudes of two binary numbers. An n -bit comparator receives two n -bit numbers, A and B , outputs are : $A > B$, $A = B$ and $A < B$. As per the magnitudes of the two numbers, one of the outputs will be high.

□□

5

Sequential Circuits and Systems

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5.1	Introduction	Winter-15,	Marks 3
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5.4	Clocked Flip-Flops	Winter-15, Summer-18,	Marks 7
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5.5	Excitation Tables	Winter-15, 17, 18,	Marks 7
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	Oral Questions and Answers		

5.1 Introduction

GTU : Winter-15

- Fig. 5.1.1 shows the block diagram of sequential circuit/Finite State Machine (FSM).
- Memory elements are connected to the combinational circuit as a feedback path.

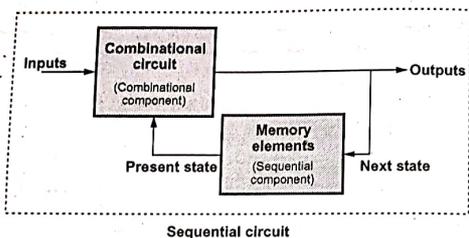


Fig. 5.1.1 Block diagram of sequential circuit / FSM

- The information stored in the memory elements at any given time defines the **present state** of the sequential circuit.
- The **present state** and the external inputs determine the outputs and the **next state** of the sequential circuit.
- Thus we can specify the sequential circuit by a time sequence of external inputs, internal states (present states and next states), and outputs.
- The counters and registers are the common examples of sequential circuits.

The memory element used in sequential circuits is a flip-flop which is capable of storing 1-bit binary information.

5.1.1 Comparison between Combinational and Sequential Logic Circuits

Sr. No.	Combinational circuits	Sequential circuits
1.	In combinational circuits, the output variables are at all times dependent on the combination of input variables.	In sequential circuits, the output variables depend not only on the present input variables but they also depend upon the past history of these input variables.
2.	Memory unit is not required in combinational circuits.	Memory unit is required to store the past history of input variables in the sequential circuit.

3.	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits.
4.	Combinational circuits are easy to design.	Sequential circuits are comparatively harder to design.
5.	Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

Table 5.1.1 Comparison between combinational and sequential circuits

5.1.2 Clock

- A clock signal is a particular type of signal that oscillates between a high and a low state and is utilized to co-ordinate actions of circuits.
- It is produced by a clock generator.
- The most common clock signal is in the form of a square wave with a 50 % duty cycle, usually with a fixed, constant frequency as shown in Fig. 5.1.2.
- Circuits using the clock signal for synchronization may become active at either the rising edge, falling edge or in the case of double data rate, both in the rising and in the falling edges of the clock cycle.
- The time required to complete one cycle is called 'clock period' or 'clock cycle'.
- Ideally, the clock signal should have sharp transitions from one level to other as shown in Fig. 5.1.2.



Fig. 5.1.2 Clock signal

Review Questions

1. Define sequential logic circuit.
2. What is flip-flop ?
3. Give the comparison between combinational and sequential logic circuits.
4. What is clock ? State its use.
5. Draw a general model for a sequential or state machine. Also list out various types of FSMs.

GTU : Winter-15, Marks 3

5.2 One-Bit Memory and the Circuit Properties of Bistable Latch

The Fig. 5.2.1 shows the basic bistable element used in latches and flip-flops.

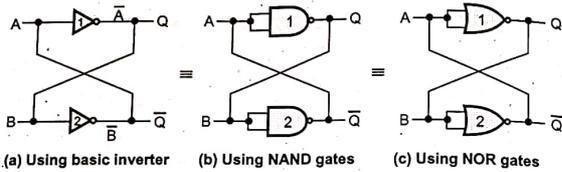


Fig. 5.2.1 Basic bistable element (1-bit memory cell)

- The basic bistable element has two outputs Q and \bar{Q} .
- It has two cross-coupled inverters, i.e., the output of the first inverter is connected as an input to the second inverter and the output of second inverter is connected as an input to the first inverter.
- The basic bistable element circuit has two stable states logic 0 and logic 1, hence the name 'bistable'.
- When $A = 0$, the output of inverter 1 is 1 (\bar{A}), i.e., $Q = 1$.
- Since the output of inverter 1 is the input to the inverter 2, $\bar{A} = B = 1$. Consequently, the output of inverter 2, i.e., \bar{B} is 0.
- Since the output of the inverter 2 is connected to the input of the inverter 1, $\bar{Q} = \bar{B} = A = 0$.
- We have assumed same value for A . Thus, the circuit is stable with $\bar{Q} = A = \bar{B} = 0$ and $Q = \bar{A} = B = 1$.
- Using similar explanation it is easy to show that if it is assumed that $A = 1$, the basic bistable element is stable with $\bar{Q} = A = \bar{B} = 1$ and $Q = \bar{A} = B = 0$. This is a second stable condition of the basic bistable element.
- The two stable states of basic bistable elements are used to store two binary elements, 0 and 1.
- In positive logic system, state $Q = 1$ is used to store logic 1, and state $Q = 0$ is used to store logic 0.
- Two outputs are complementary. That is when $Q = 0$, $\bar{Q} = 1$; and when $Q = 1$, $\bar{Q} = 0$.

Important Points

- The outputs Q and \bar{Q} are always complementary.
- The circuit has two stable states. The state corresponds to $Q = 1$ is referred to as 1 state or set state and state corresponds to $Q = 0$ is referred to as 0 state or reset state.
- If the circuit is in the set (1) state, it will remain in the set state and if the circuit is in the reset (0) state, it will remain in the reset state. This property of the circuit shows that it can store 1-bit of digital information. Therefore, the circuit is called a 1-bit memory cell.
- The 1-bit information stored in the circuit is locked or latched in the circuit. Therefore, this circuit is also referred to as a latch.

Review Question

- Explain the operation of one-bit memory cell.

5.3 Latches

GTU : Winter-15, Summer-18

5.3.1 SR Latch

- Fig. 5.3.1 shows SR latch which is 1-bit memory cell.
- Two inverters 3 and 4 are connected to enter the digital information.
- Input for gate 3 is S and input for gate 4 is R . This latch is also called RS latch.

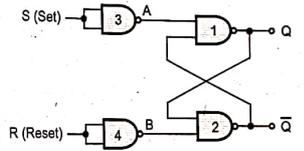


Fig. 5.3.1 SR latch

- For understanding the circuit operation, we must first determine the output of NAND gate whose one of the input is logic 0 and accordingly we have to determine the output of other NAND gate in the cross coupled circuit.
- Because the output of NAND gate is 1 if any one input is 0.
- The circuit operation is as follows. In Fig. 5.3.2, the output of shaded NAND gate is determined first, and the 0 input that decides the output of shaded NAND as 1 is shown in bold.

Case 1 : $S = R = 0$

In this case, $\bar{S} = \bar{R} = 1$. If Q is 1, Q and B inputs for NAND gate 2 are both 1 and hence output $\bar{Q} = 0$. Since $\bar{Q} = 0$ and $\bar{S} = 1$, the output of NAND gate 1 is 1, i.e. $Q = 1$.

If Q is 0, Q and \bar{R} inputs for NAND gate 2 are 0 and 1, and hence output $\bar{Q} = 1$. Since $\bar{Q} = 1$ and $\bar{S} = 1$, the output of NAND gate 1 is 0, i.e., $Q = 0$.

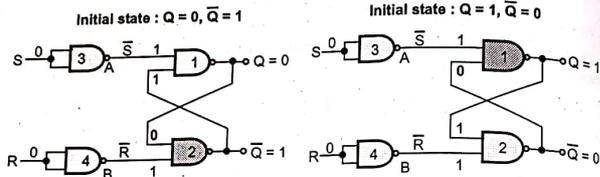


Fig. 5.3.2

This shows that when $S = R = 0$, the outputs do not change.

Case 2 : $S = 1$ and $R = 0$

In this case, $\bar{S} = 0$ and $\bar{R} = 1$. Since $\bar{S} = 0$, the output of NAND gate 1, $Q = 1$ (Recall that, for NAND any one or more input is 0, the output is 1) For NAND gate 2, both inputs Q and \bar{R} are 1, thus output $\bar{Q} = 0$.

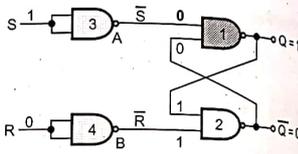


Fig. 5.3.3

The inputs $S = 1$ and $R = 0$, makes $Q = 1$, i.e., set state.

Case 3 : $S = 0$ and $R = 1$

In this case, $\bar{S} = 1$ and $\bar{R} = 0$. Since $\bar{R} = 0$, the output of NAND gate 2, $\bar{Q} = 1$. For NAND gate 1, both inputs \bar{Q} and \bar{S} are 1, thus output $Q = 0$.

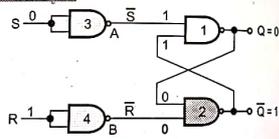


Fig. 5.3.4

The inputs $S = 0$ and $R = 1$, makes $Q = 0$, i.e., reset state.

Case 4 : $S = 1$ and $R = 1$

When $S = R = 1$, both the outputs Q and \bar{Q} try to become 1 which is not allowed and therefore, this input condition is prohibited.

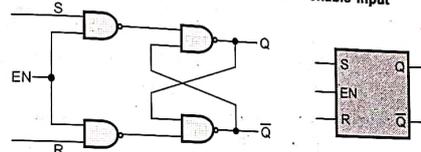
5.3.2 Gated SR Latch

- In the SR latch output changes occur immediately after the input changes occur i.e. the latch is sensitive to its S and R inputs at all times.
- It can easily be modified to create a latch that is sensitive to these inputs only when an enable input is active. Such a latch with enable input is known as gated SR latch. It is as shown in the Fig. 5.3.5.

- The Table 5.3.1 shows the truth table for gated latch.

EN	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate
1	1	1	1	X	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

Table 5.3.1 Truth table for SR latch with enable input



(a) SR latch with enable input using NAND gates (b) Logic symbol

Fig. 5.3.5

- As shown by truth table, the circuit behaves like a SR latch when $EN = 1$, and retains its previous state when $EN = 0$.

5.3.3 Gated D Latch

- For SR latch, when both inputs are same the output either does not change or it is invalid (Inputs $\rightarrow 00$, no change and inputs $\rightarrow 11$, invalid).
- In many practical applications, these input conditions are not required.
- These input conditions can be avoided by making them complement of each other. This modified SR latch is known as D latch.
- Fig. 5.3.6 shows the D latch.
- The NAND gates 1, 2, 3 and 4 form the basic SR latch with enable input.
- The fifth NAND gate is used to provide the complemented inputs.
- As shown in the Fig. 5.3.6, D input goes directly to the S input, and its complement is applied to the R input, through gate 5. Therefore, only two input conditions exist, either $S = 0$ and $R = 1$ or $S = 1$ and $R = 0$.

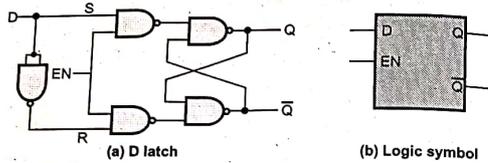


Fig. 5.3.6

The truth table for D latch is as shown in the Table 5.3.2.

EN	D	Q _n	Q _{n+1}	State
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Q _n	No Change (NC)

Table 5.3.2 Truth table for D latch

As shown in the truth table, the Q output follows the D input. For this reason D latch is sometimes called transparent latch.

Looking at the truth table for D latch with enable input and simplifying Q_{n+1} function by k-map we get the characteristic equation for D latch with enable input as

$$Q_{n+1} = EN \cdot D + \overline{EN} \cdot Q_n$$

This is illustrated in Fig. 5.3.7.

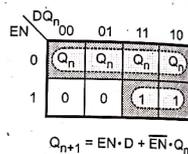


Fig. 5.3.7 Characteristic equation

Review Questions

1. What is SR latch ? Explain its operation.
2. What is gated SR latch ?
3. Explain the working of gated D latch with truth table and characteristic equation.
4. Draw gated SR latch using NAND gates only.
5. Draw and explain in brief a high assertion input SR latch.
6. Which latch is also known as transparent latch ?
7. Draw high assertion and low assertion input SR latches.
8. Draw gated SR latch using NAND gates only.

GTU : Summer-18, Marks 3
 GTU : Winter-15, Marks 3
 GTU : Winter-15, Mark 1
 GTU : Summer-18, Marks 3
 GTU : Summer-18, Marks 3

5.4 Clocked Flip-Flops

GTU : Dec.-13, May-12, 13, 14, Summer-15, 17, 18, Winter-15, 17, 18

5.4.1 Latches Vs Flip-Flops

- Latches and flip-flops are the basic building blocks of the most sequential circuits.
- The main difference between latches and flip-flops is in the method used for changing their state.
- A simple latch forms the basis for the flip-flop.
- Latches are controlled by enable signal, and they are level triggered, either positive level triggered or negative level triggered.
- The output state is free to change according to the S and R input values, when active level is maintained at the enable input.
- Flip-flops are pulse or clock edge triggered instead of level triggered.

5.4.2 Level and Edge Triggering

Level Triggering

- In the level triggering, the output state is allowed to change according to input(s) when active level (either positive or negative) is maintained at the enable input.
- There are two types of level triggered latches :
- Positive level triggered :** The output of flip-flop responds to the input changes only when its enable input is 1 (HIGH).

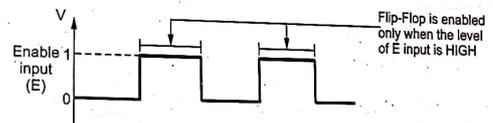


Fig. 5.4.1 Positive level triggering

- Negative level triggered :** The output of flip-flop responds to the input changes only when its enable input is 0 (LOW).

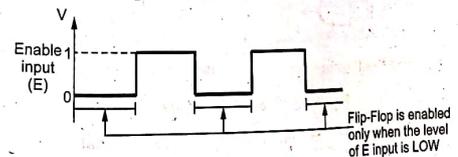


Fig. 5.4.2 Negative level triggering

Edge Triggering

- In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock pulse at the clock input.
- There are two types of edge triggering.
- **Positive edge triggering** : Here, the output responds to the changes in the input only at the positive edge of the clock pulse at the clock input.

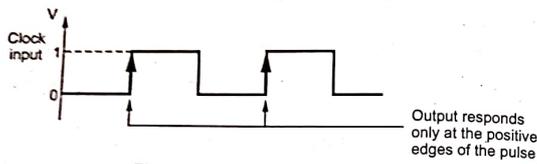


Fig. 5.4.3 Positive edge triggering

- **Negative edge triggering** : Here, the output responds to the changes in the input only at the negative edge of the clock pulse at the clock input.

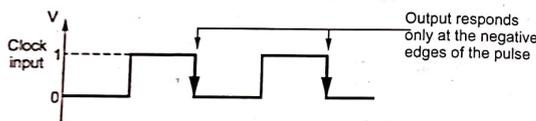


Fig. 5.4.4 Negative edge triggering

5.4.3 SR Flip-Flop

Positive Edge Triggered SR Flip-Flop

- The Fig. 5.4.5 shows the positive edge triggered clocked SR flip-flop.

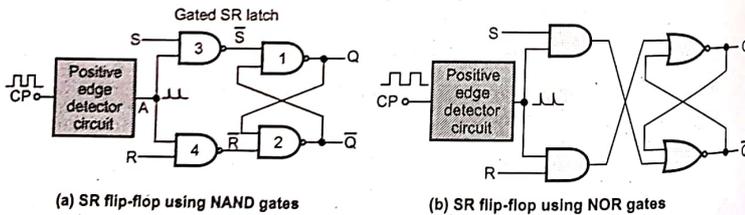
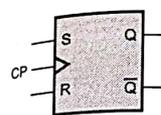


Fig. 5.4.5 Clocked SR flip-flop

- The circuit is similar to SR latch except enable signal is replaced by the Clock Pulse (CP) followed by the positive edge detector circuit.

- The edge detector circuit is a differentiator.
- The Fig. 5.4.7 shows input and output waveforms for positive edge triggered clocked SR flip-flop.
- The circuit output responds to the S and R inputs only at the positive edges of the clock pulse. At any other instants of time, the SR flip-flop will not respond to the changes in input.

The Fig. 5.4.6 shows the logic symbol and truth table of clocked SR flip-flop.



(a) Logic symbol

CP	S	R	Q _n	Q _{n+1}	State
↑	0	0	0	0	No Change(NC)
↑	0	0	1	1	No Change(NC)
↑	0	1	0	0	Reset
↑	0	1	1	0	Reset
↑	1	0	0	1	Set
↑	1	0	1	1	Set
↑	1	1	0	X	Indeterminate
↑	1	1	1	X	Indeterminate
0	X	X	0	0	No Change(NC)
0	X	X	1	1	No Change(NC)

(b) Truth table for positive edge clocked SR flip-flop

SR	Q _n	Q _{n+1}
00	0	1
01	0	0
11	X	X
10	1	1

(c) Characteristic equation
Q_{n+1} = S + R Q_n

Fig. 5.4.6

- Case 1 :** If S = R = 0 and the clock pulse is applied, the output do not change, i.e. Q_{n+1} = Q_n. This is indicated in the first row of the truth table.
- Case 2 :** If S = 0, R = 1 and the clock pulse is applied, Q_{n+1} = 0. This is indicated in the second row of the truth table.
- Case 3 :** If S = 1, R = 0 and the clock pulse is applied, Q_{n+1} = 1. This is indicated in the third row of the truth table.
- Case 4 :** If S = R = 1 and the clock pulse is applied, the state of the flip-flop is undefined and therefore is indicated as indeterminate in the fourth row of the truth table.

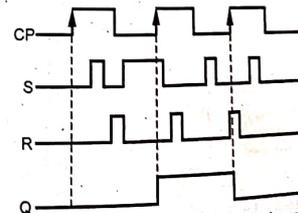
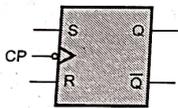


Fig. 5.4.7 Input and output waveforms for positive edge triggered clocked SR flip-flop

Negative Edge Triggered SR Flip-Flop

- In the negative edge triggered SR flip-flop, the negative edge detector circuit is used and the circuit output responds at the negative edges of the clock pulse.
- The Fig. 5.4.8 and Fig. 5.4.9 shows the logic symbol, truth table, and input and output waveforms for negative edge triggered SR flip-flop.
- The bubble at the clock input indicates that the flip-flop is negative edge triggered.



(a) Logic symbol

CP	S	R	Q _n	Q _{n+1}	State
↓	0	0	0	0	No change(NC)
↓	0	0	1	1	
↓	0	1	0	0	Reset
↓	0	1	1	0	Set
↓	1	0	0	1	
↓	1	0	1	1	Indeterminate
↓	1	1	1	X	
0	X	X	0	0	No change(NC)
0	X	X	1	1	

(b) Truth Table for negative edge clocked SR flip-flop

Fig. 5.4.8

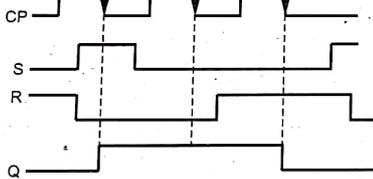


Fig. 5.4.9 Input and output waveforms for negative edge triggered clocked SR flip-flop

Example 5.4.1 Realize SR flip-flop using NOR gates.

Solution :

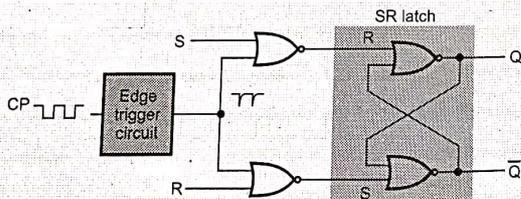
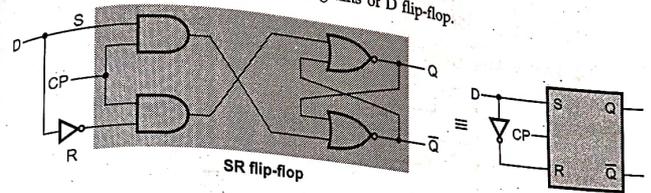


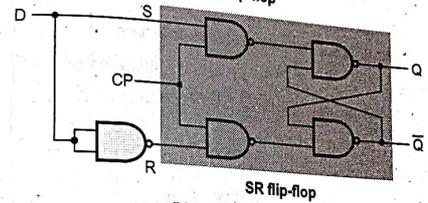
Fig. 5.4.10 Negative edge-triggered SR flip-flop using only NOR gates

5.4.4 D Flip-Flop

- The Fig. 5.4.11 shows the logic diagrams of D flip-flop.



(a) D flip-flop



(b) D flip-flop using NAND gates

Fig. 5.4.11

- The basic building block of D flip-flop is a SR flip-flop.
- The SR flip-flop has two data inputs S and R.
- The S input is made high to store 1 in the flip-flop and R input is made high to store 0 in the flip-flop.
- When both inputs are same the output either does not change or it is invalid (Inputs → 00, no change and inputs → 11, invalid).
- In many practical applications, these input conditions are not required.
- These input conditions can be avoided by making them complement of each other. This modified SR flip-flop is known as D flip-flop.
- The D input goes directly to the S input, and its complement is applied to the R input. Due to these connections, only two input conditions exists, either S = 0 and R = 1 or S = 1 and R = 0.

Truth Table

- The truth table for D flip-flop consider only these two conditions and it is as shown in the Fig. 5.4.12 (b).

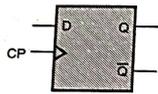


Fig. 5.4.12 (a) Logic symbol

CP	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n

Fig. 5.4.12 (b) Truth table of D flip-flop

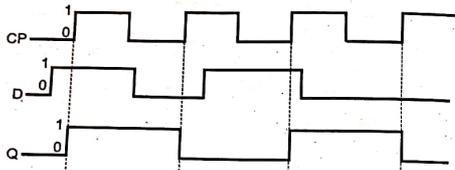


Fig. 5.4.12 (c) Input and output waveforms of clocked D flip-flop

- Q_{n+1} function follows D input at the positive going edges of the clock pulses. Hence the characteristic equation for D flip-flop is $Q_{n+1} = D$.
- The output Q_{n+1} is delayed by one clock period. Thus, D flip-flop is also known as **delay flip-flop**.

If we connect the \bar{Q} output of D flip-flop to its D input as shown in the Fig. 5.4.13, the output of D flip-flop will change either from 0 to 1 or from 1 to 0 at every positive edge of the D flip-flop.

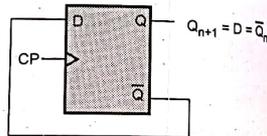
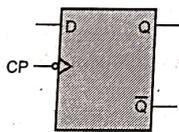


Fig. 5.4.13

Such change in the output is known as **toggling** of the flip-flop output.

Negative Edge Triggered D Flip-Flop

- In case of negative edge triggering, the output is sensitive at the negative edge of the clock input.
- The Fig. 5.4.14 shows the logic symbol and truth table for negative edge triggered D flip-flop.



(a) Logic symbol

CP	D	Q_{n+1}
↓	0	0
↓	1	1
0	X	Q_n

(b) Truth table of D flip-flop

Fig. 5.4.14

- Fig. 5.4.15 shows input and output waveforms for negative edge triggered D flip-flop.
- The bubble at the clock input indicates that the flip-flop is negative edge triggered.

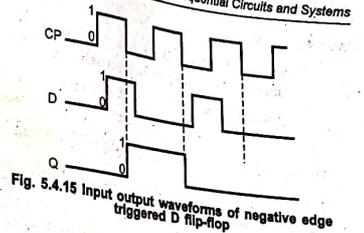


Fig. 5.4.15 Input output waveforms of negative edge triggered D flip-flop

5.4.5 JK Flip-Flop

- The uncertainty in the state of an SR flip-flop when $S = R = 1$ can be eliminated by converting it into a JK flip-flop.
- The data inputs are J and K which are ANDed with Q and \bar{Q} respectively, to obtain S and R inputs, as shown in the Fig. 5.4.16. Thus, $S = J \cdot \bar{Q}$ and $R = K \cdot Q$.

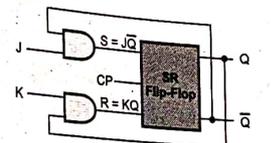


Fig. 5.4.16 JK flip-flop using SR flip-flop

Operation of JK Flip-Flop

Case 1 : J = K = 0

When $J = K = 0$, $S = R = 0$ and according to truth table of SR flip-flop there is no change in the output.

When inputs $J = K = 0$, output does not change.

Case 2 : J = 1 and K = 0

$Q = 0, \bar{Q} = 1$: When $J = 1, K = 0$ and $Q = 0, S = 1$ and $R = 0$. According to truth table of SR flip-flop it is set state and the output Q will be 1.

$Q = 1, \bar{Q} = 0$: When $J = 1, K = 0$ and $Q = 1, S = 0$ and $R = 0$. Since $SR = 00$, there is no change in the output and therefore, $Q = 1$ and $\bar{Q} = 0$.

The inputs $J = 1$ and $K = 0$, makes $Q = 1$, i.e. set state.

Case 3 : J = 0 and K = 1

$Q = 0, \bar{Q} = 1$: When $J = 0, K = 1$ and $Q = 0, S = 0$ and $R = 0$. Since $SR = 00$, there is no change in the output and therefore, $Q = 0$ and $\bar{Q} = 1$.

$Q = 1, \bar{Q} = 0$: When $J = 0, K = 1$ and $Q = 1, S = 0$ and $R = 1$. According to truth table of SR flip-flop it is a reset state and the output Q will be 0.

The inputs $J = 0$ and $K = 1$, makes $Q = 0$, i.e., reset state.

Case 4 : J = K = 1

$Q = 0, \bar{Q} = 1$: When $J = K = 1$ and $Q = 0, S = 1$ and $R = 0$. According to truth table of SR flip-flop it is a set state and the output Q will be 1.

$Q = 1, \bar{Q} = 0$: When $J = K = 1$ and $Q = 1, S = 0$ and $R = 1$. According to truth table of SR flip-flop it is a reset state and the output Q will be 0.

The input $J = K = 1$, toggles the flip-flop output.

- Fig. 5.4.17 shows the logic symbol, truth table and timing diagram of positive edge triggered JK flip-flop.

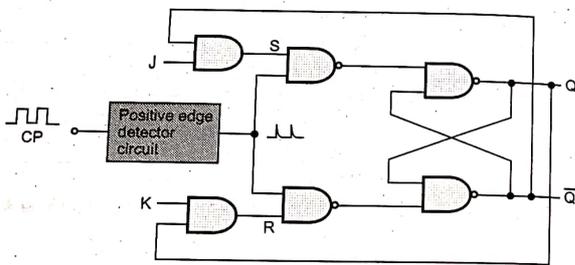


Fig. 5.4.17 (a) Clocked JK flip-flop

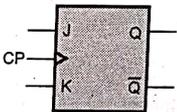


Fig. 5.4.17 (b) Logic symbol

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

Fig. 5.4.17 (c) Truth table

JK	00	01	11	10
Q_n 0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K} = J \bar{Q}_n + \bar{K} Q_n$$

Fig. 5.4.17 (d) Characteristics equation

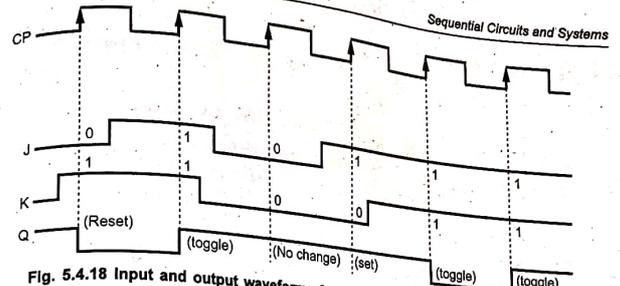


Fig. 5.4.18 Input and output waveforms for positive edge triggered JK flip-flop

Example 5.4.2 Construct a clocked JK flip-flop which is triggered at the positive edge of the clock pulse from a clocked SR flip-flop consisting of NOR gates.

Solution :

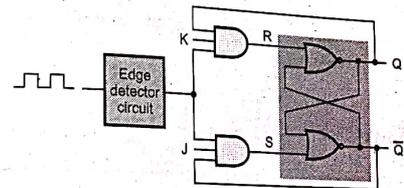


Fig. 5.4.19

5.4.5.1 JK Flip-Flop using NAND Gates

- The Fig. 5.4.20 shows the modified circuit of JK flip-flop which has only NAND gates.

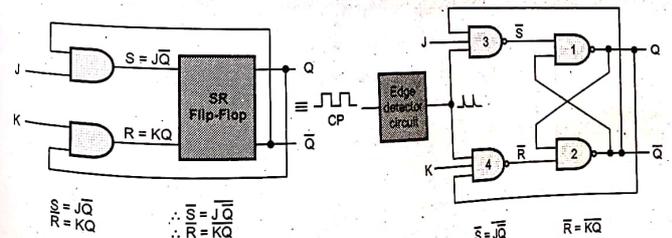


Fig. 5.4.20 JK flip-flop using NAND gates

5.4.5.2 Race-around Condition

- In JK flip-flop, when $J = K = 1$, the output toggles (output changes either from 0 to 1 or from 1 to 0).
- Consider that initially $Q = 0$ and $J = K = 1$. After a time interval Δt equal to the propagation delay through two NAND gates in series, the output will change to $Q = 1$ and after another time interval of Δt the output will change back to $Q = 0$. This toggling will continue until the flip-flop is disabled and $J = K = 1$. At the end of clock pulse the flip-flop is disabled and the value of Q is uncertain. This situation is referred to as the race-around condition. This is illustrated in Fig. 5.4.21.
- This condition exists when $t_p \geq \Delta t$. Thus by keeping $t_p < \Delta t$ we can avoid race around condition.
- We can keep $t_p < \Delta t$ by keeping the duration of edge less than Δt .
- A more practical method for overcoming this difficulty is the use of the Master-Slave (MS) configuration.

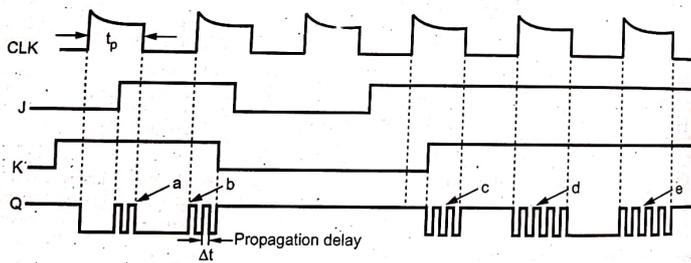


Fig. 5.4.21 Input and output waveforms for clocked JK flip-flop

Example 5.4.3 Realize a JK flip-flop using only NOR gates.

Solution :

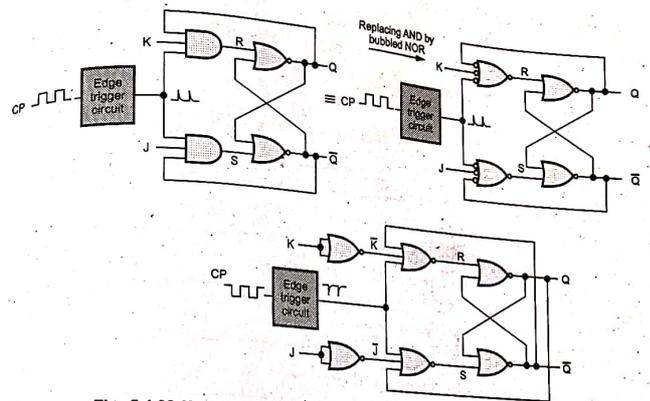


Fig. 5.4.22 Negative edge triggered JK flip-flop using only NOR gates

5.4.6 Master-Slave SR Flip-Flop

- A master-slave flip-flop is constructed from two flip-flops.
- One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a master-slave flip-flop.
- Fig. 5.4.23 shows SR master-slave flip-flop.

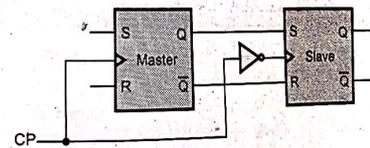


Fig. 5.4.23 Master-Slave SR flip-flop

- It consists of a master flip-flop, a slave flip-flop, and an inverter.
- Both the flip-flops are positive level triggered, but inverter connected at the clock input of the slave flip-flop forces it to trigger at the negative level.

- The output state of the master flip-flop is determined by the S and R inputs at the positive clock pulse.
- The output state of the master is then transferred as an input to the slave flip-flop. The slave flip-flop uses this input at the negative clock pulse to determine its output state.
- Fig. 5.4.24 illustrates the operation of the master-slave flip-flop.

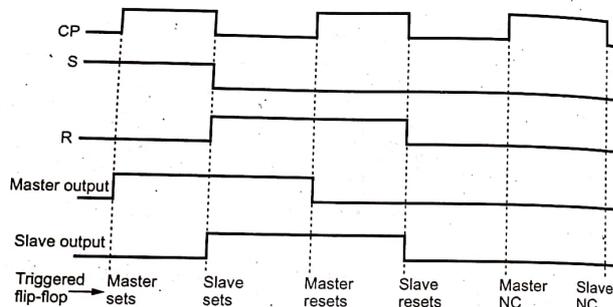


Fig. 5.4.24 Input and output waveforms for master-slave flip-flop

5.4.7 Master-Slave JK Flip-Flop

- Fig. 5.4.25 shows the master-slave JK flip-flop. Positive clock pulses are applied to first flip-flop and inverted (negative) clock pulses are applied to second flip-flop. (See Fig. 5.4.25 on next page)
- When $CK = 1$, the first flip-flop is enabled and the outputs Q_M and \bar{Q}_M responds to the inputs of J and K according to the Table 1. At this time, the second flip-flop is inhibited because its clock is low, $\bar{CK} = 0$.
- When CK goes Low ($\bar{CK} = 1$), the first flip-flop is inhibited and second flip-flop is enabled. At this time, the output of second flip-flop (Q and \bar{Q}) follow the outputs Q_M and \bar{Q}_M , respectively.
- Since the second flip-flop follows the first one, it is referred to as the **slave** and the first one as the **master**.
- In master-slave JK flip-flop state change occurs when flip-flop goes through both positive transition (first half) of clock and negative transition of the clock (second half). Thus, race-around condition does not exist in the master-slave JK flip-flop.

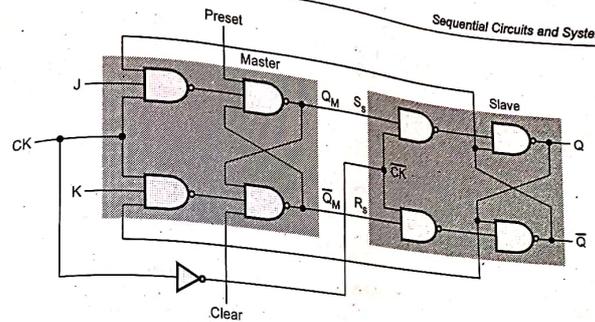


Fig. 5.4.25 Master - slave JK flip - flop

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

≡

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

Table 5.4.1 Truth table

5.4.8 T Flip-Flop

- T flip-flop is also known as 'Toggle flip-flop'.
- The T flip-flop is a modification of the JK flip-flop.
- As shown in the Fig. 5.4.27, the T flip-flop is obtained from a JK flip-flop by connecting both inputs, J and K together.

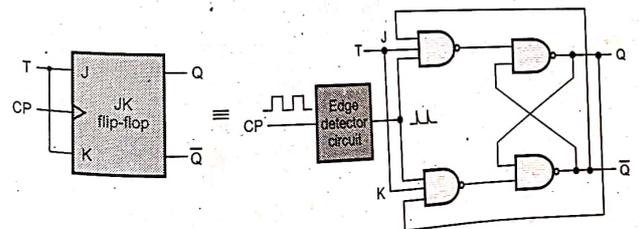
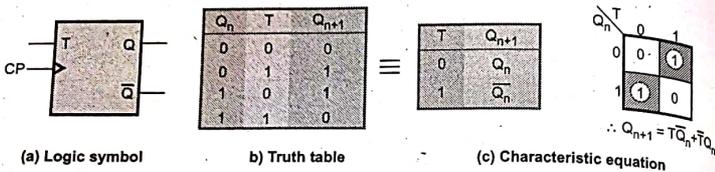
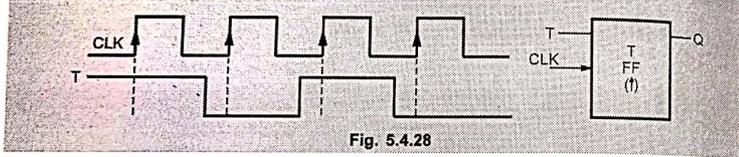


Fig. 5.4.26 T flip-flop using NAND gates

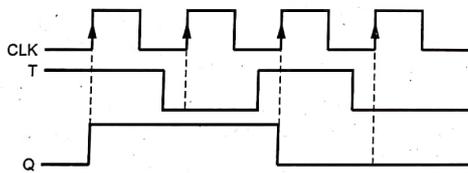
- When $T = 0$, $J = K = 0$ and hence there is no change in the output. When $T = 1$, $J = K = 1$ and hence output toggles.
- The Fig. 5.4.27 shows logic symbol, truth table and the characteristic equation for T flip-flop.



Example 5.4.4 Refer Fig. 5.4.28 and determine the Q output waveform if the flip-flop starts out RESET.



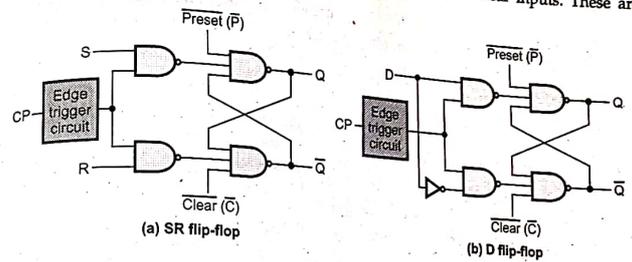
Solution :



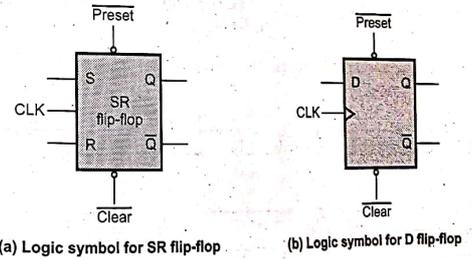
5.4.9 Preset and Clear

- For the flip-flops discussed so far, the SR, D, JK, and T, the inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.
- When power is turn ON, the state of the flip-flop is uncertain. It may come to set ($Q = 1$) or reset ($Q = 0$) state.

- In many applications, it is necessary to initially set or reset the flip-flop. Such initial state of flip-flop can be accomplished by using the direct or asynchronous inputs of the flip-flop. These inputs are : Preset (\bar{P}) and Clear (\bar{C}). They can be applied at any time between clock pulses and are not in synchronism with the active-low inputs.
- Fig. 5.4.30 shows the SR and D flip-flops with preset and clear inputs. These are



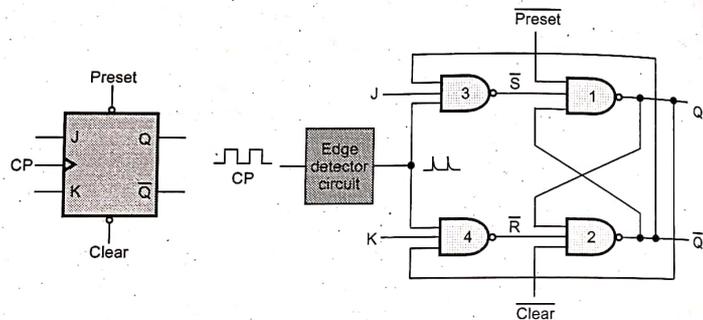
- When $\bar{P} = \bar{C} = 1$, the circuit operates in accordance with the truth table of SR flip-flop.
- If $\bar{P} = 1$ and $\bar{C} = 0$, the flip-flop is reset and $\bar{P} = 0$ and $\bar{C} = 1$, the flip-flop is set.



Note Condition $\bar{P} = \bar{C} = 0$ must not be used, since this leads to an uncertain state.

- The JK flip-flop with preset and clear is shown in Fig. 5.4.32.
- If preset and clear inputs are 1, the circuit operates in accordance with the truth table of JK flip-flop given in the Fig. 5.4.32 (c).

- If preset = 0 and clear = 1, the output of NAND gate 1 will certainly be 1. Consequently, all the three inputs to NAND gate 2 will be 1 which will make $\bar{Q} = 0$.
- Making preset = 0 sets the flip-flop.
- Preset signal is active when it is low, hence it is active low signal.
- Low (0) on the clear input resets the flip-flop making $\bar{Q} = 1$.
- A logic symbol for a JK flip-flop with active low preset and clear inputs is shown in the Fig. 5.4.32 (a). These inputs are active low, therefore they must both be kept high for synchronous operation.



(a) Logic symbol

(b) JK flip-flop with active high preset and clear
Fig. 5.4.32

- The Fig. 5.4.33 illustrates the operation of active low preset and clear inputs.

Assume $J = K = 1$

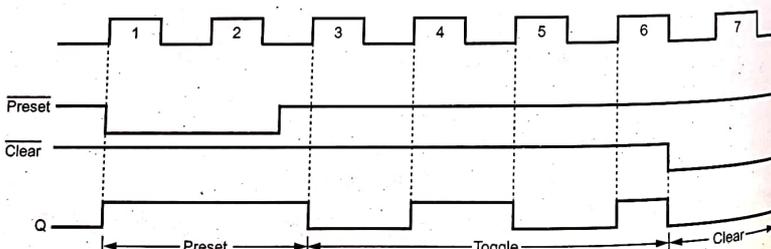


Fig. 5.4.33 Input and output waveforms showing operation of active low preset and clear inputs

- During clock pulse 1 and 2 the $\bar{\text{Preset}}$ is low, keeping the flip-flop set regardless of the synchronous inputs.
- For clock pulses 3, 4, 5 and 6, toggle operation occurs because J and K both are high with preset and clear inactive.
- For clock pulse 7, the $\bar{\text{Clear}}$ input is low, keeping the flip-flop reset regardless of the synchronous inputs.
- In some IC packages preset and clear inputs are active high. In those cases preset and clear input must both be kept low for synchronous operation.

Example 5.4.5 1. For the Fig. 5.4.34, 5.4.35 and 5.4.36, plot the output waveforms referenced to the clock signal assuming the initial contents of all FFs is $Q = 0$. Assume all FFs are edge triggered.

GTU : Winter-15, Marks 7

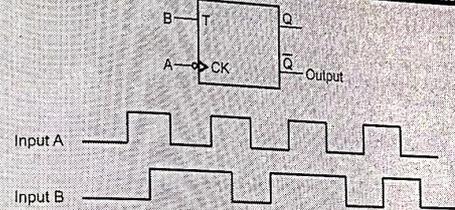


Fig. 5.4.34

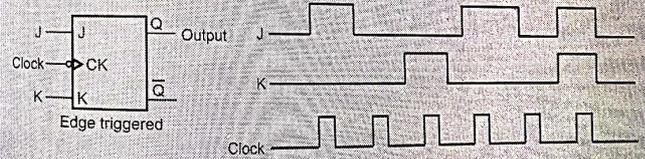


Fig. 5.4.35

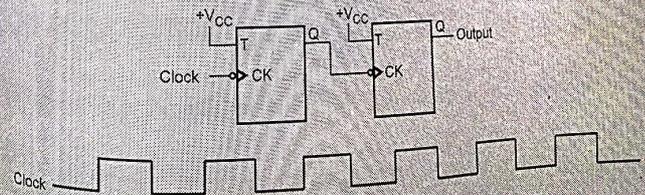
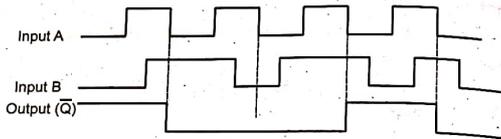


Fig. 5.4.36

Solution :



Note : In T flip-flop output toggles when T = 1

Fig. 5.4.34 (a)

2.

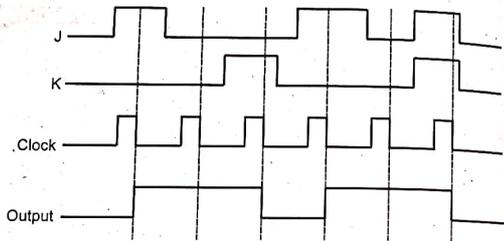


Fig. 5.4.35

3.

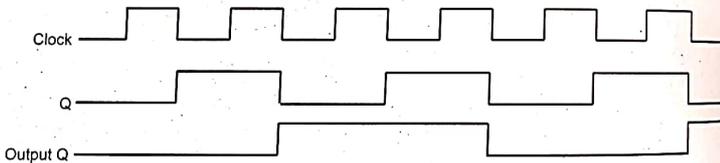


Fig. 5.4.36

Example 5.4.6 1. Fill in values for S and R to cause the Q values of the SR FF given in Fig. 5.4.37.

	t_0	t_1	t_2	t_3
S	0			
R	0			
Q	1	0	0	1

Fig. 5.4.37

GTU : Winter-15, Marks 4

Solution :

- t_1 : S = 0, R = 1
 - t_2 : S = 0, R = X
 - t_3 : S = 1, R = 0
- X : don't care

Example 5.4.7 Plot the output waveform for the inputs shown in Fig. 5.4.38, assuming the initial contents of the FF is Q = 0.

GTU : Winter-15, Marks 3

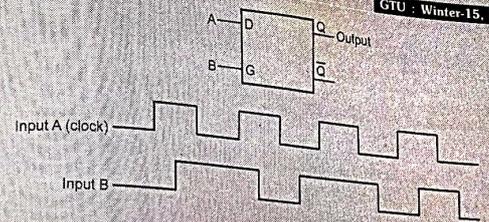


Fig. 5.4.38

Solution :

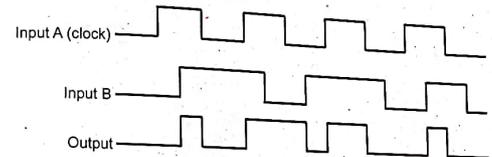


Fig. 5.4.38 (a)

Example 5.4.8 Plot the out waveform referenced to the clock signal assuming the initial contents of the flip - flops is q = 0. Assume all flip - flops are edge triggered.

GTU : Summer-17, Marks 3

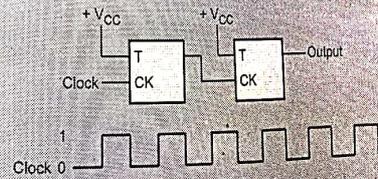


Fig. 5.4.39

Solution : Assuming flip - flops are positive edge trigger :

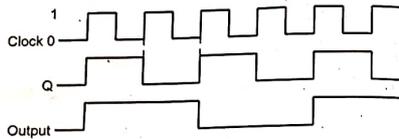


Fig. 5.4.39 (a)

Review Questions

1. Define the following term : Flip Flop. **GTU : Dec-13, Mark 1**
2. Differentiate between latches and flip-flops.
3. Explain the different types of triggering methods used for flip-flops.
4. What is S-R flip-flop ? Explain working of clocked SR flip-flop. What is edge triggering ?
5. Explain the clocked SR flip-flop using NAND gates.
6. Explain D type positive edge triggered flip flop. **GTU : May-13, Marks 7**
7. If Q output of a D-type flip-flop is connected to D input, it acts as a toggle switch. State whether true or false ? Justify your answer. **GTU : May-14, Marks 7**
8. Write a brief note on edge-triggered SR and JK flip-flops. **GTU : May-14, Marks 7**
9. Justify name delay for D flip-flop.
10. Explain the application of D flip-flop.
11. Explain the operation of JK flip-flop with truth table.
12. Draw the JK flip-flop using NAND gates.
13. Explain race around condition.
14. Discuss method to avoid race around condition in JK flip-flop.
15. Explain MS J-K flip-flop. **GTU : May-14, Dec-13, May-12, Winter-17, Marks 4**
16. Draw and explain the operation of T flip-flop.
17. Explain the application of T flip-flop.
18. Explain the use of reset and preset inputs.
19. Draw the truth table of full adder and implement using minimum number of logic gates. **GTU : Summer-15, Marks 7**
20. With the help of function table and circuit diagram explain the working of clocked SR flip flop. **GTU : Summer-15, Marks 7**
21. Draw the truth tables for JK and T flip-flop. **STU : Summer-18, Marks 4**
22. Explain working of master - slave JK flip - flop with necessary logic diagram, state equation and state diagram. **GTU : Winter-17, Marks 7**

23. Draw the truth table for JK and TFF. Using these truth tables, derive and explain the excitation tables of JK and T FF. **GTU : Summer-18, Marks 7**
24. Discuss Clocked R-S Flip-flop with Logic diagram. Symbol, Characteristic a table and Characteristic equation. **GTU : Winter-18, Marks 7**
25. Draw the characteristic table of following Flip-flop. **GTU : Winter-18, Marks 3**
i) R-S ii) J - K iii) K

5.5 Excitation Tables

- During the design process we know, from the transition table, the sequence of states, i.e., the transition from each present state to its corresponding next state. From this information we wish to find the flip-flop input conditions that will cause the required transition. For this reason, we need a table that lists the required inputs for a given change of state. Such a table is known as an excitation table of the flip-flop.
- We can derive the excitation tables for flip-flops from their truth tables.
- The excitation table consists of two columns Q_n and Q_{n+1} , and a column for each input to show how the required transition can be achieved.

5.5.1 SR Flip-Flop

- Table 5.5.1 (a) and (b) show the truth table and excitation tables for SR flip-flop, respectively.

S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	*

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(a) SR truth table

(b) SR excitation table

Table 5.5.1

- There are four possible transitions from the present state to the next state.
- For each transition, the required input condition is derived from the information available in the truth table.

Note The symbol "X" in the table represents a don't care condition, i.e. it indicates that to get required output it does not matter whether the input is either 1 or 0.

- **0 → 0 Transition :** The present state of the flip-flop is 0 and is to remain 0 when a clock pulse is applied. Looking at truth table of SR flip-flop we can understand that, this can happen either when $R = S = 0$ (no-change condition) or when $R = 1$ and $S = 0$. Thus, S has to be at 0, but R can be at either level. The table indicates this with a "0" under S and an "X" (don't care) under R.

- **0 → 1 Transition** : The present state is 0 and is to change to 1. This can happen only when $S = 1$ and $R = 0$ (set condition). Therefore, S has to be 1 and R has to be 0 for this transition to occur.
- **1 → 0 Transition** : The present state is 1 and is to change to a 0. This can happen only when $S = 0$ and $R = 1$ (reset condition). Therefore, S has to be 0 and R has to be 1 for this transition to occur.
- **1 → 1 Transition** : The present state is 1 and is to remain 1. This can happen either when $S = 1$ and $R = 0$ (set condition) or when $S = 0$ and $R = 0$ (no change condition). Thus R has to be 0, but S can be at either level. The table indicates this with a "X" under S and "0" under R .

5.5.2 JK Flip-Flop

- The truth table and excitation table for JK flip-flop are shown in Table 5.5.2 (a) and (b) respectively.
- **0 → 0 Transition** : When both present state and next state are 0, the J input must remain at 0 and the K input can be either 0 and 1.

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

(a) JK truth table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) JK excitation table

Table 5.5.2

- **0 → 1 Transition** : The present state is 0 and is to change to 1. This can happen either when $J = 1$ and $K = 0$ (set condition) or when $J = K = 1$ (toggle condition). Thus, J has to be 1, but K can be at either level for this transition to occur.
- **1 → 0 Transition** : The present state is 1 and is to change to 0. This can happen either when $J = 0$ and $K = 1$ or when $J = K = 1$. Thus, K has to be 1 but J can be at either level.
- **1 → 1 Transition** : When both present state and next are 1, the K input must remain at 0 while the J input can be 0 or 1.
- The excitation table for JK flip-flop has more don't care conditions than the excitation table for RS flip-flop.
- The don't care terms usually simplify the function. Therefore, the combinational circuits using JK flip-flops for the input functions are likely to be simpler than those using RS flip-flops.

5.5.3 D Flip-Flop

- The Table 5.5.3 (a) and (b) show the truth table and excitation table for D flip-flop, respectively.
- In D flip-flop, the next state is always equal to the D input and it is independent of the present state. Therefore, D must be 0 if Q_{n+1} has to be 0, and 1 if Q_{n+1} has to be 1, regardless of the value of Q_n .

D	Q_{n+1}
0	0
1	1

(a) D truth table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(b) D excitation table

Table 5.5.3

5.5.4 T Flip-Flop

- The Table 5.5.4 (a) and (b) show the truth table and the excitation table for T flip-flop, respectively.
- When input $T = 1$, the state of the flip-flop is complemented; when $T = 0$, the state of the flip-flop remains unchanged. Therefore, for $0 \rightarrow 0$ and $1 \rightarrow 1$ transitions T must be 0 and for $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions T must be 1.

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

(a) T truth table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) T excitation table

Table 5.5.4

Review Questions

1. Derive the excitation tables for SR, D, JK and T flip-flop.
2. Draw the truth table of full subtractor and implement using minimum number of logic gates. GTU : Summer-15, Marks 7
3. Derive and explain the excitation tables of JK and T FF. GTU : Summer-18, Marks 4

5.6 Conversion from One Type to another Type of Flip-Flop

GTU : Summer-15

- It is possible to convert one flip-flop into another flip-flop with some additional gates or simply doing some extra connection.

5.6.1 SR Flip-Flop to D Flip-Flop

- The excitation table for above conversion is as shown in Table 5.6.1.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Table 5.6.1

K-map simplification

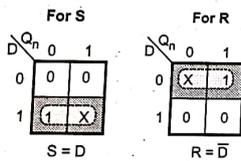


Fig. 5.6.1

Logic diagram

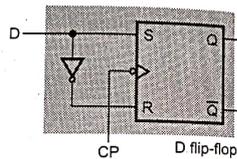


Fig. 5.6.2 SR to D flip-flop conversion

5.6.2 SR Flip-Flop to JK Flip-Flop

- The excitation table for above conversion is as shown in Table 5.6.2.

Inputs		Present state	Next state	Flip-flop inputs	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Table 5.6.2

K-map simplification

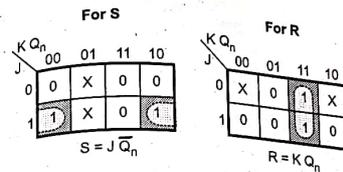


Fig. 5.6.3

Logic diagram

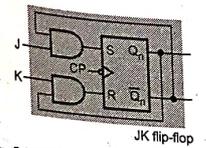


Fig. 5.6.4 SR to JK flip-flop conversion

5.6.3 SR Flip-Flop to T Flip-Flop

- The excitation table for above conversion is as shown in the Table 5.6.3.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Table 5.6.3

K-map simplification

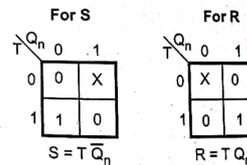


Fig. 5.6.5

Logic diagram

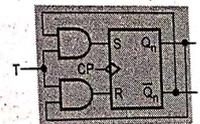


Fig. 5.6.6 SR to T flip-flop conversion

- If we apply clock pulses to the circuit, the circuit output will toggle from 0 to 1 and 1 to 0. Thus, we can build 1-bit counter using SR flip-flop by converting it to T flip-flop.

Example 5.6.1 Prepare the truth table for the circuit of Fig. 5.6.7 and show that it acts as a T-type flip-flop.

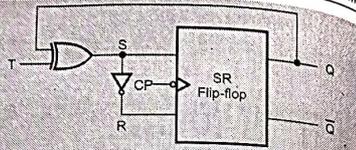


Fig. 5.6.7

Solution : For SR flip-flop,

$$Q_{n+1} = S + \bar{R}Q_n \quad \dots \text{Characteristics equation}$$

$$= S + SQ_n$$

$$= S(1 + Q_n) = S \quad \therefore R = \bar{S}$$

We have, $S = Q_n \oplus T$

$$\therefore Q_{n+1} = Q_n \oplus T$$

$$= T\bar{Q}_n + \bar{T}Q_n \quad \dots \text{Characteristic equation of T flip-flop}$$

C_P	T	Q_n	$S = Q_n \oplus T$	$R = \bar{S}$	$Q_{n+1} = S$
↓	0	0	0	1	0
↓	0	1	1	0	1
↓	1	0	1	0	1
↓	1	1	0	1	0

Table 5.6.4 Truth table for the given circuit

- Looking at column 1 and column 5 of the Table 5.6.4 we can conclude that when $T=0$, the output does not change and when $T=1$, the output toggles. Thus, the given circuit acts as a T flip-flop. This is another way of implementing T flip-flop using SR flip-flop.

5.6.4 JK Flip-Flop (OR MSJK) to T Flip-Flop

- The excitation table for above conversion is as shown in Table 5.6.5.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	J_A	K_A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Table 5.6.5

K-map simplification

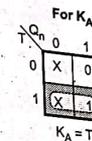
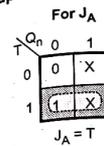


Fig. 5.6.8

Logic diagram

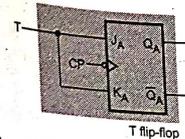


Fig. 5.6.9 JK to T flip-flop conversion

5.6.5 JK Flip-Flop (OR MSJK) to D Flip-Flop

- The excitation table for above conversion is as shown in the Table 5.6.6.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Table 5.6.6

K-map simplification

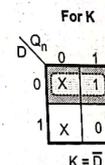
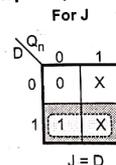


Fig. 5.6.10

Logic diagram

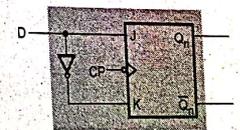


Fig. 5.6.11 JK to D flip-flop conversion

5.6.6 D Flip-Flop to T Flip-Flop

- The excitation table for above conversion is as shown in the Table 5.6.7.

Input	Present state	Next state	Flip-flop input
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Table 5.6.7

K-map simplification

		For D	
T	Q_n	0	1
0	0	1	0
1	1	0	1

Fig. 5.6.12

$$D = \bar{T}Q_n + T\bar{Q}_n = T \oplus Q_n$$

Logic diagram

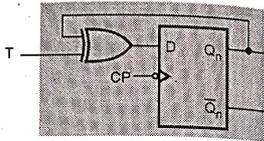


Fig. 5.6.13 D to T flip-flop conversion

Example 5.6.2 Analyze the circuit and prove that it is equivalent to T flip-flop.

Solution : To analyze the circuit means to derive the truth table for it.

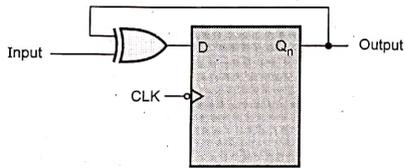


Fig. 5.6.14

We have, $D = \text{Input} \oplus Q_n$

CLK	Input	Q_n	$D = \text{Input} \oplus Q_n$	Q_{n+1}
↓	0	0	0	0
↓	0	1	1	1
↓	1	0	1	1
↓	1	1	0	0

When input is 0
output does not change

When input is 1
output toggles.

Table 5.6.8 Truth table for given circuit

- In the above circuit, output does not change when input is 0 and it toggles when input is 1. This is the characteristics of T flip-flop. Hence, the given circuit is T flip-flop constructed using D flip-flop.

5.6.7 T Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 5.6.9.

Input	Present state	Next state	Flip-flop input
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 5.6.9

K-map simplification

For T

		For T	
D	Q_n	0	1
0	0	1	0
1	1	0	1

$$T = D\bar{Q}_n + \bar{D}Q_n$$

Fig. 5.6.15

Logic diagram

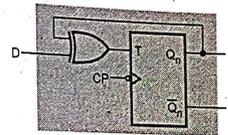


Fig. 5.6.16 T to D flip-flop conversion

5.6.8 JK Flip-Flop (OR MSJK) to SR Flip-Flop

The excitation table for above conversion is as shown in Table 5.6.10.

Inputs		Present state	Next state	Flip-flop inputs	
S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

Table 5.6.10 Excitation table for JK to SR conversion

K-map simplification

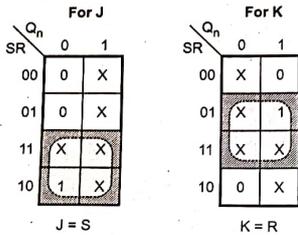


Fig. 5.6.17

Logic diagram

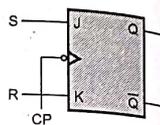


Fig. 5.6.18 JK to SR flip-flop conversion

5.6.9 D Flip-Flop to SR Flip-Flop

- The excitation table for above conversion is as shown in the Table 5.6.11.

Inputs		Present state	Next state	Flip-flop input
S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X

Table 5.6.11 Excitation table for D to SR conversion

K - map simplification

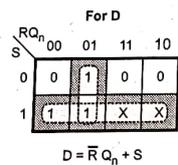


Fig. 5.6.19

Logic diagram

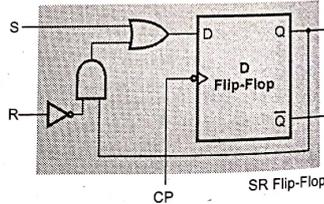


Fig. 5.6.20 D to SR flip-flop conversion

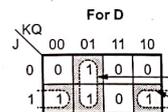
5.6.10 T Flip-Flop to SR Flip-Flop

- The excitation table for conversion of T FF into an SR FF is as shown in the Table 5.6.12.

Inputs		Present state	Next state	Flip-flop input
S	R	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	X	X
1	1	1	X	X

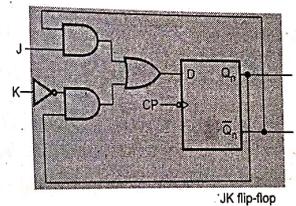
Table 5.6.12 Excitation table for T to SR conversion

K - map simplification



(a)

Logic diagram



(b)

Fig. 5.6.21

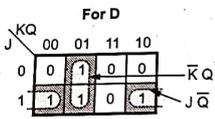
5.6.11 D Flip-Flop to JK Flip-Flop

The excitation table for conversion of D flip-flop to JK flip-flop :

Inputs		Present state	Next state	Flip-flop input
J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	0	1	1	1

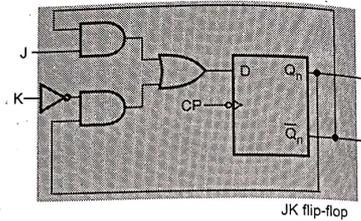
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

K - map simplification



(a)

Logic diagram



(b)

Fig. 5.6.22

Review Questions

1. Convert SR flip-flop to D flip-flop.
2. Convert SR flip-flop to JK flip-flop.
3. Convert SR flip-flop to T flip-flop.
4. Convert JK flip-flop to T flip-flop.
5. Convert JK flip-flop to D flip-flop.
6. Convert D flip-flop to T flip-flop.
7. Convert T flip-flop to D flip-flop.
8. Convert JK flip-flop to SR flip-flop.
9. Convert D flip-flop to SR flip-flop.
10. Convert D flip flop into SR flip flop.

GTU : Summer-15, Marks 7

5.7 Applications of Flip-Flops

Some of the important applications of flip-flops are :

- It can be used as a memory element.
- It can be used to eliminate key debounce.

- It is used as a basic building block in sequential circuits such as counters and registers.
- It can be used as a delay element.

5.7.1 Bounce Elimination Switch

- For interfacing keys to the digital systems, usually push button keys are used.
- Push button keys when pressed bounces a few times, closing and opening the contacts before providing a steady reading, as shown in the Fig. 5.7.1.

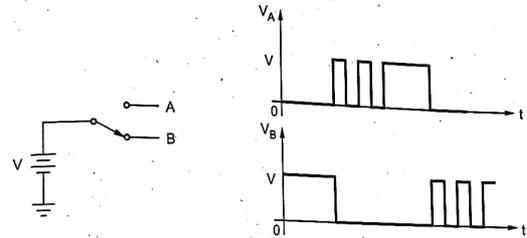


Fig. 5.7.1 Effect of key debounce

- Reading taken during bouncing period may be faulty. This problem is known as **key debounce**.
- The problem of key debounce is undesirable and it must be avoided.
- One way to avoid key debounce problem is to use SR latch.
- The circuit used to avoid keybounce with SR latch is called a **switch or contact debouncer**.
- The Fig. 5.7.2 shows the switch debouncer circuit and its waveforms.
- When key is at position A, the output of SR latch is logic 1, and when key is at position B, the output of SR latch is logic 0.
- When key is in between A and B, SR inputs are 00 and hence output does not change, preventing debouncing of key output.

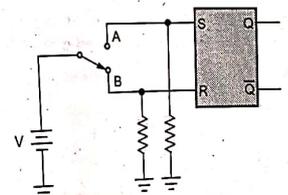


Fig. 5.7.2 (a) Switch debouncer

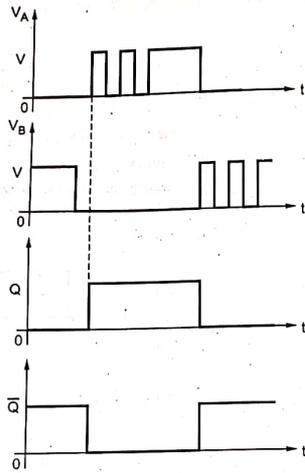


Fig. 5.7.2 Waveforms of switch debouncer

- We can say that the output does not change during transition period, eliminating key debounce.

5.7.2 Registers

- A group of flip-flops connected together forms a register.
- A register is used solely for storing and shifting data which is in the form of 1s and/or 0s, entered from an external source.
- Fig. 5.7.3 shows 3-bit register using three D flip-flops.
- Preset, reset and clock inputs are connected in parallel and 3-bit input is applied to D inputs of the flip-flop.
- During positive edge of the clock, D inputs of the flip-flops are stored within the flip-flop and are available at the outputs of D flip-flops.

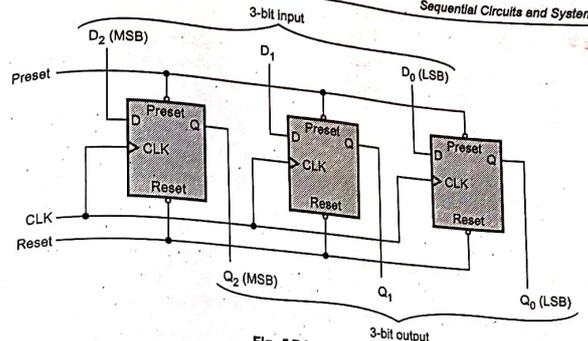


Fig. 5.7.3 Register

5.7.3 Counters

- A counter is a register capable of counting the number of clock pulses arriving at its clock input.
- Count represents the number of clock pulses arrived.
- On arrival of each clock pulse, the counter is incremented by one.
- In case of down counter, it is decremented by one.
- Fig. 5.7.4 shows 3-bit counter.
- It consists of three flip-flops.
- A counter with n flip-flops has 2^n possible states.
- The 3-bit counter can count from decimal 0 to 7.

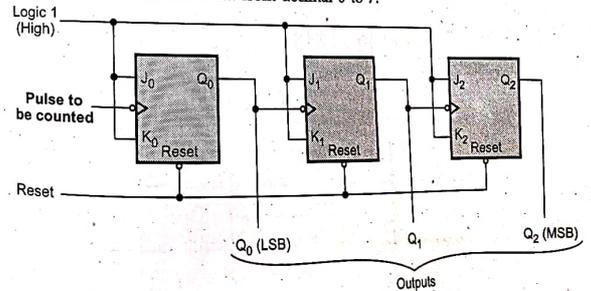


Fig. 5.7.4 Counter

5.7.4 Frequency Division

- A frequency divider, also called a clock divider or scaler or prescaler, is a circuit that takes an input signal of a frequency, f_{in} and generates an output signal of a frequency :

$$f_{out} = \frac{f_{in}}{n}$$

where n is an integer.

- For power-of-2 integer division, a simple binary counter can be used, clocked by the input signal. The least-significant output bit alternates at 1/2 the rate of the input clock, the next bit at 1/4 the rate, the third bit at 1/8 the rate, etc.
- An arrangement of flip-flops are a classic method for integer-n division.
- The easiest configuration is a series where each flip-flop is a divide-by-2. For a series of three of these, such system would be a divide-by-8.
- By adding additional logic gates to the chain of flip-flops, other division ratios can be obtained.
- The Fig. 5.7.6 shows frequency divider using D flip-flops. Here, D flip-flops are used as toggle flip-flops. After each stage frequency is divided by 2.

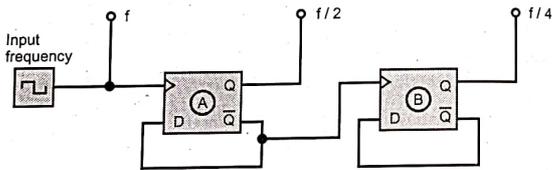


Fig. 5.7.5 Frequency divider using D flip-flops

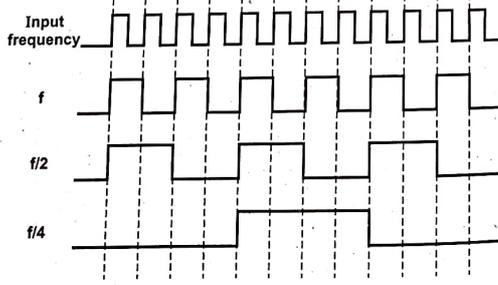


Fig. 5.7.6 Frequency divider waveform

5.7.5 Clock System with Delayed Clock Signal

- In many digital systems, a clock signal with 50 % duty cycle is used to drive the digital system and in turn it initiates actions in various components. As the transition occurs only every half-period for a 50 % duty cycle clock, it helps to generate a second clock signal with a one-quarter delay of clock period. Thus, the occurrence of transition increases due to both the clock signal and delayed

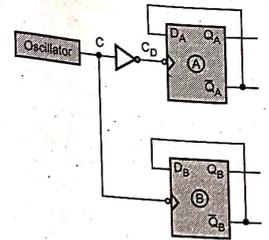


Fig. 5.7.7 Clock system with delayed clock signal

- Fig. 5.7.7 shows the clock system with delayed clock signal. The oscillator generates a clock signal C and its delayed version (C_D) is obtained by inverting the clock signal C. As shown in Fig. 5.7.8 the signal Q_A generates clock transition at the one-quarter and three-quarter points of the period and signal Q_B generates clock transition at the beginning and at the one-half point of the period.
- The main disadvantage of this technique is that the oscillator need to generate an output frequency that is twice the required frequency.

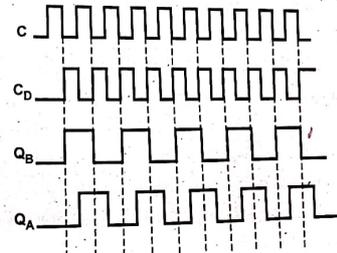


Fig. 5.7.8 Waveforms of clock system with delayed clock signal

5.7.6 A Two Phase Clock Circuit

- Fig. 5.7.9 shows the two phase clock circuit that consists of two separate signals and each of them go high for a portion of the clock cycle but not simultaneously.
- The glitches at point a on ϕ_1 and at point b on ϕ_2 can be eliminated by the use of delaying inverters.
- The signal C_D must go low before signal C goes high so as to avoid glitch at point a on ϕ_1 . Same is the case at point b on ϕ_2 .
- The delay introduced by the inverters must exceed delay introduced by flip-flops.

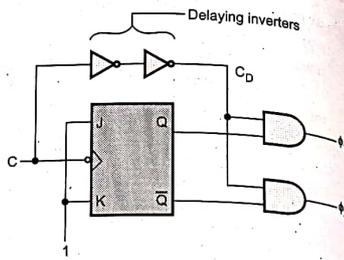


Fig. 5.7.9 Two phase clock circuit

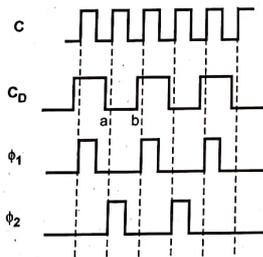


Fig. 5.7.10 Waveforms of two phase clock circuit

Review Questions

1. List the applications of flip-flops.
2. How keyboard debouncing is eliminated using flip-flop? Explain with suitable circuit diagram.
3. Write a short note on frequency division.
4. Explain in detail clock system with delayed clock signal.
5. Write a note on two phase clock circuit.

5.8 Registers and Shift Registers

GTU : Dec-13, May-13, 14, Summer-15, 18, Winter-18

- A group of flip-flops can be used to store a word, which is called register.
- A flip-flop can store 1-bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

Buffer Register

- Fig. 5.8.1 shows the simplest register constructed with four D flip-flops. This register is also called buffer register.

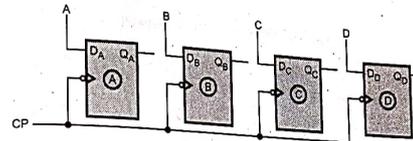


Fig. 5.8.1 Buffer register

- Each D flip-flop is triggered with a common negative edge clock pulse.
- The input bits set up the flip-flops for loading.
- When the first negative clock edge arrives, the stored binary information becomes, $Q_A Q_B Q_C Q_D = ABCD$
- In this register, four D flip-flops are used. So it can store 4-bit binary information.
- The number of flip-flop stages in a register determines its total storage capacity.

Controlled Buffer Register

- We can control input and output of the register by connecting tri-state devices at the input and output sides of register as shown in Fig. 4.8.2. So this register is called 'controlled buffer register'.
- Here, tri-state switches are used to control the operation.
- When you want to store data in the register, you have to make \overline{LOAD} or \overline{WR} signal low to activate the tri-state buffers.
- When you want the data at the output, you have to make \overline{RD} signal low to activate the buffers.
- Controlled buffer registers are commonly used for temporary storage of data within a digital system.

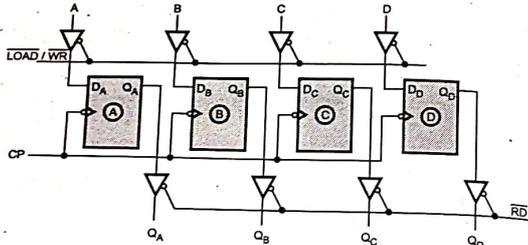


Fig. 5.8.2 Controlled buffer register

- As seen above the 4-bit register can store 4-bit binary information. In general, n-bit register can store n-bit binary information.

Example 5.8.1 Determine the number of flip-flops needed to construct a register capable of storing,

- i) A 6-bit binary number
- ii) Decimal numbers up to 32
- iii) Hexadecimal numbers up to F
- iv) Octal numbers up to 10.

Solution :

- i) A 6-bit binary number requires register with 6 flip-flops.
- ii) $(32)_{10} = (100000)_2$. The number of bits required to represent 32 in binary are six, therefore, 6 flip-flops are needed to construct a register capable of storing 32 decimal.
- iii) $(F)_{16} = (1111)_2$. The number of bits required to represent $(F)_{16}$ in binary are four, therefore four flip-flops are needed to construct a register capable of storing $(F)_{16}$.
- iv) $(10)_8 = (1000)_2$. The number of bits required to represent $(10)_8$ in binary are four, therefore, four flip-flops are needed to construct a register capable of storing $(10)_8$.

5.8.1 Shift Registers

- The binary information (data) in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to a group of registers called 'shift registers'.

- They are very important in applications involving the storage and transfer of data in a digital system.
- Fig. 5.8.3 gives the symbolical representation of the different types of data movement in shift register operations.

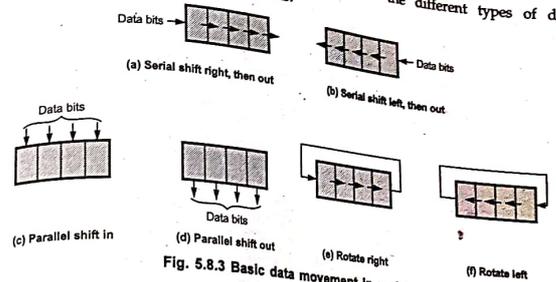


Fig. 5.8.3 Basic data movement in registers

- According to the data movement in a register, there are different types of shift registers.

5.8.2 Types of Shift Registers

5.8.2.1 Serial in Serial Out (SISO) Shift Register

Shift Left Mode

- Fig. 5.8.4 shows serial-in serial-out shift-left register.

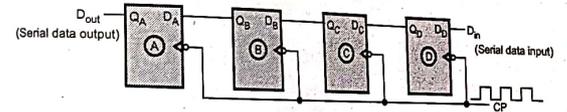
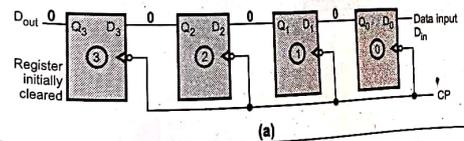


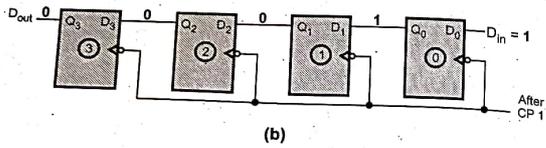
Fig. 5.8.4 Shift-left register

- We will illustrate the entry of the four bit binary number 1111 into the register, beginning with the left-most bit. Initially, register is cleared.

So $Q_3Q_2Q_1Q_0 = 0000$

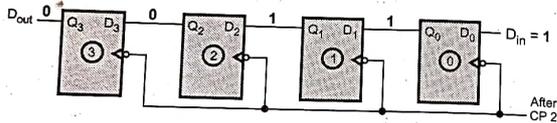


a) When data 1 1 1 1 is applied serially, i.e. left-most 1 is applied as D_{in} , $D_{in} = 1$, $Q_3Q_2Q_1Q_0 = 0 0 0 0$. The arrival of the first falling clock edge sets the right-most flip-flop, and the stored word becomes, $Q_3Q_2Q_1Q_0 = 0 0 0 1$



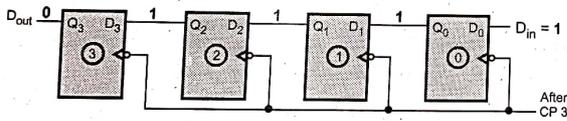
(b)

b) When the next negative clock edge hits, the Q_1 flip-flop sets and the register contents become, $Q_3Q_2Q_1Q_0 = 0 0 1 1$



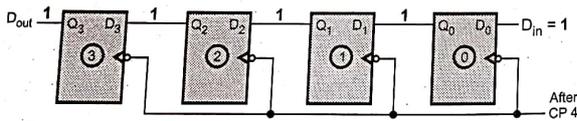
(c)

c) The third negative clock edge result: in, $Q_3Q_2Q_1Q_0 = 0 1 1 1$



(d)

d) The fourth falling clock edge gives, $Q_3Q_2Q_1Q_0 = 1 1 1 1$.



(e)

Fig. 5.8.5 Four bits 1111 being serially entered into shift-left register

The Table 5.8.1 summarizes the shift left operation.

CP	Q_3	Q_2	Q_1	Q_0	D_{in}
Initially	0	0	0	0	1
1 st	0	0	0	1	1
2 nd	0	0	1	1	1
3 rd	0	1	1	1	1
4 th	1	1	1	1	1

Table 5.8.1 Shift left operation

Fig. 5.8.6 shows waveforms for shift left operation

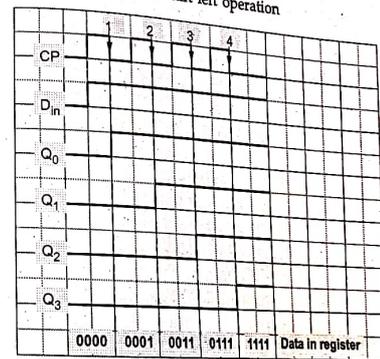


Fig. 5.8.6 Waveforms for shift left register

Shift Right Mode

Fig. 5.8.7 shows serial-in serial-out shift-right register.

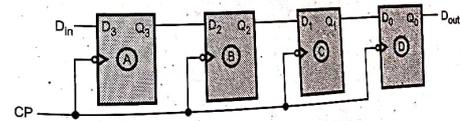
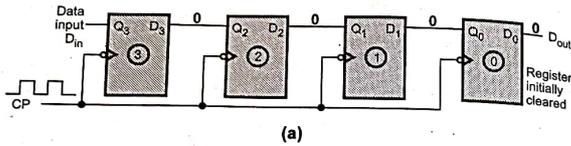


Fig. 5.8.7 Shift-right register

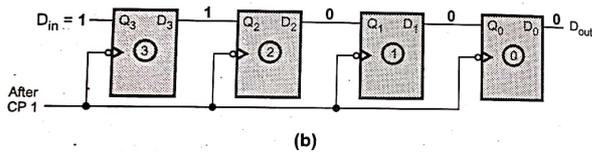
- We will illustrate the entry of the four bit binary number 1111 into the register, beginning with the left-most bit.



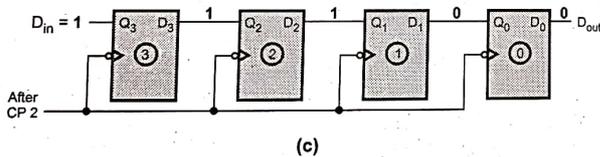
Initially, register is cleared. So $Q_3Q_2Q_1Q_0 = 0000$

a) When data 1111 is applied serially, i.e. left-most 1 is applied as D_{in} ,
 $D_{in} = 1, Q_3Q_2Q_1Q_0 = 0000$

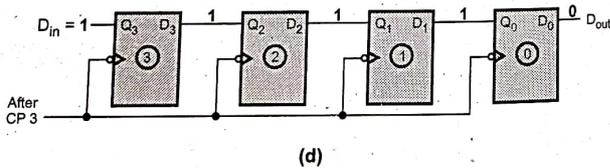
- The arrival of the first falling clock edge sets the left-most flip-flop, and the stored word becomes, $Q_3Q_2Q_1Q_0 = 1000$



b) When the next falling clock edge hits, the Q_2 flip-flop sets and the register contents become, $Q_3Q_2Q_1Q_0 = 1100$



c) The third falling clock edge results in, $Q_3Q_2Q_1Q_0 = 1110$.



- d) The fourth falling clock edge gives, $Q_3Q_2Q_1Q_0 = 1111$.

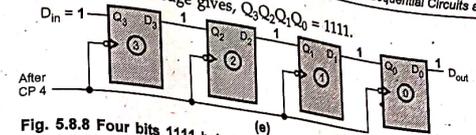


Fig. 5.8.8 Four bits 1111 being serially entered into shift-right register

- Table 5.8.2 summarizes the shift right operation.

CP	D_{in}	Q_3	Q_2	Q_1	Q_0
Initially	1	0	0	0	0
↓ 1 st	1	1	0	0	0
↓ 2 nd	1	1	1	0	0
↓ 3 rd	1	1	1	1	0
↓ 4 th	1	1	1	1	1

Table 5.8.2 Shift right operation

The Fig. 5.8.9 shows waveforms for shift right operation.

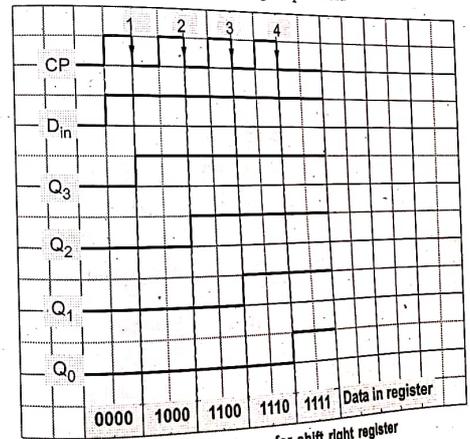


Fig. 5.8.9 Waveforms for shift right register

5.8.2.2 Serial In Parallel Out (SIPO) Shift Register

- The data bits are entered serially into the register but the output is taken in parallel.
- Once the data are stored, each bit appears on its respective output line and all bits are available simultaneously as shown in Fig. 5.8.10.

CP	Q ₃	Q ₂	Q ₁	Q ₀
-	NC	NC	NC	NC
↓	D ₃	D ₂	D ₁	D ₀

Table 5.8.3 Truth table

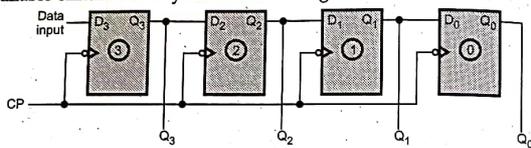


Fig. 5.8.10 A Serial In Parallel Out (SIPO) shift register

5.8.2.3 Parallel In Serial Out (PISO) Shift Register

- In this type, the bits are entered in parallel i.e. simultaneously into their respective stages, on parallel lines.
- Fig. 5.8.11 illustrates a four-bit parallel in serial out register.

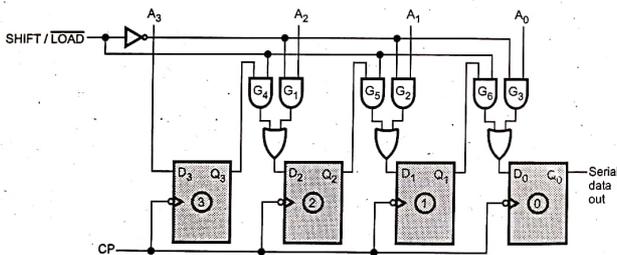


Fig. 5.8.11 Parallel In Serial Out (PISO) shift register

- There are four input lines A₃, A₂, A₁, A₀ for entering data in parallel into the register.
- SHIFT/LOAD is the control input which allows shift or loading data operation of the register.
- When SHIFT/LOAD is low, gates G₁, G₂, G₃ are enabled, allowing each input data bit to be applied to D input of its respective flip-flop.
- When a clock pulse is applied, the flip-flops with D = 1 will SET and those with D = 0 will RESET.
- All four bits are stored simultaneously.

- When SHIFT/LOAD is high, gates G₁, G₂, G₃ are disabled and gates G₄, G₅, G₆ are enabled. This allows the data bits to shift right from one stage to the next.
- The OR gates at the D-inputs of the flip-flops allow either the parallel data entry operation or shift operation, depending on which AND gates are enabled by the level on the SHIFT/LOAD input.

5.8.2.4 Parallel In Parallel Out (PIPO) Shift Register

- In 'parallel in parallel out register', there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously.
- Fig. 5.8.12 shows this type of register.

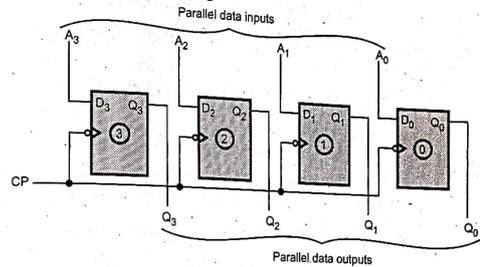


Fig. 5.8.12 Parallel In Parallel Out (PIPO) shift register

5.8.2.5 Bidirectional Shift Register

- This type of register allows shifting of data either to the left or to the right side. It can be implemented by using logic gate circuitry that enables the transfer of data from one stage to the next stage to the right or to the left, depending on the level of a control line.
- Fig. 5.8.13 illustrates a four-bit bidirectional register.

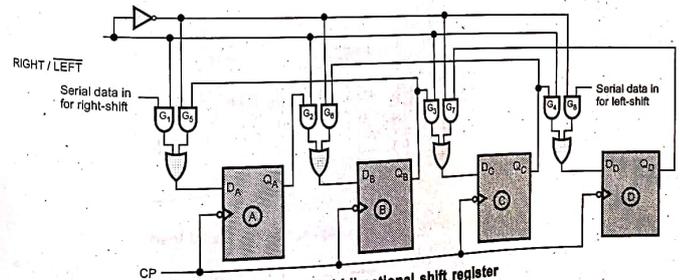


Fig. 5.8.13 4-bit bidirectional shift register

- The RIGHT/LEFT is the control input signal which allows data shifting either towards right or towards left.
- A high on this line enables the shifting of data towards right and a low enables it towards left.
- When RIGHT/LEFT signal is high, gates G_1, G_2, G_3, G_4 are enabled.
- The state of the Q output of each flip-flop is passed through the D input of the following flip-flop.
- When a clock pulse arrives, the data are shifted one place to the right.
- When the RIGHT/LEFT signal is low, gates G_5, G_6, G_7, G_8 are enabled.
- The Q output of each flip-flop is passed through the D input of the preceding flip-flop.
- When clock pulse arrives, the data are shifted one place to the left.

Bidirectional Shift Register with Parallel Load

- When parallel load capability is added to the shift register, the data entered in parallel can be taken out in serial fashion by shifting the data stored in the register. Such a register is called bidirectional shift register with parallel load.
- Fig. 5.8.14 shows bidirectional shift register with parallel load.
- As shown in the Fig. 5.8.14, the D input of each flip-flop has three sources : Output of left adjacent flip-flop, output of right adjacent flip-flop and parallel input. Out of these three sources one source is selected at a time and it is done with the help of decoder. The decoder select lines (SL_1 and SL_0) select the one source out of three as shown in the Table 5.8.4.

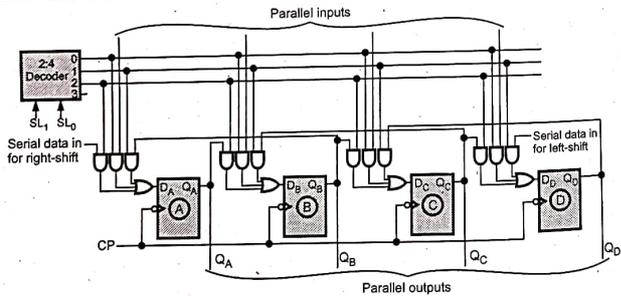


Fig. 5.8.14 4-bit bidirectional shift register with parallel load

- When select lines are 00 (i.e. $SL_1 = 0$ and $SL_0 = 0$), data from the parallel inputs is loaded into the 4-bit register.

- When select lines are 01 (i.e. $SL_1 = 0$ and $SL_0 = 1$), data within the register is shifted 1-bit left.
- When select lines are 10 (i.e. $SL_1 = 1$ and $SL_0 = 0$), data within the register is shifted 1-bit right.

SL_1	SL_0	Selected source
0	0	Parallel input
0	1	Output of right adjacent FF
1	0	Output of left adjacent FF

Table 5.8.4

5.8.3 Universal Shift Register

- A register capable of shifting in one direction only is a unidirectional shift register.
- A register capable of shifting in both directions is a bidirectional shift register.
- If the register has both shifts (right shift and left shift) and parallel load capabilities, it is referred to as universal shift register.
- The Fig. 5.8.15 shows the 4-bit universal shift register.

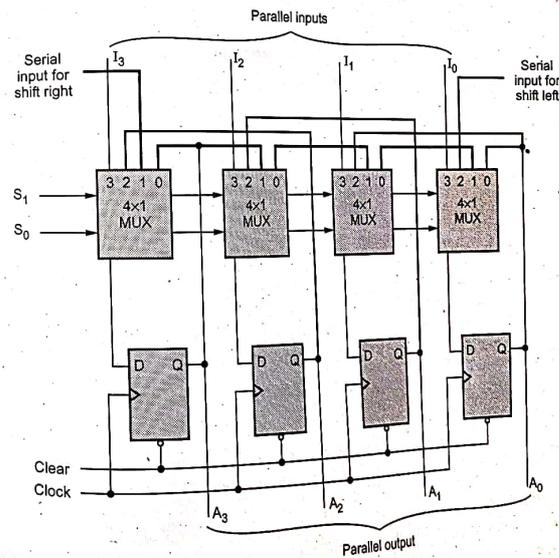


Fig. 5.8.15 4-bit universal shift register

- It consists of four flip-flops and four multiplexers.
- The four multiplexers have two common selection inputs S_1 and S_0 , and they select appropriate input for D flip-flop.
- The Table 5.8.5 shows the register operation depending on the selection inputs of multiplexers.
- When $S_1S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in the register value.
- When $S_1S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift register.
- When $S_1S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left shift register.
- Finally, when $S_1S_0 = 11$, the binary information on the parallel input lines is transferred into the register simultaneously and it is a parallel load operation.

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Table 5.8.5 Mode control and register operation

Example 5.8.2 Draw the logic diagram of a 4-bit shift register with four D flip-flops and four 4x1 multiplexer with mode selection inputs S_1 and S_0 . The register operates as follows.

S_1	S_0	Register operation
0	0	No change
0	1	Complement
1	0	Clear to 0
1	1	Load parallel data

Solution : The Fig. 5.8.16 shows the register that does the given operations.
(See Fig. 5.8.16 on next page)

5.8.4 Applications of Shift Registers

- Primary use of shift register is temporary data storage and bit manipulations. Some of the common applications of shift registers are as discussed below.

5.8.4.1 Delay Line

- A Serial-In-Serial-Out (SISO) shift register can be used to introduce time delay Δt in digital signals. The time delay can be given as

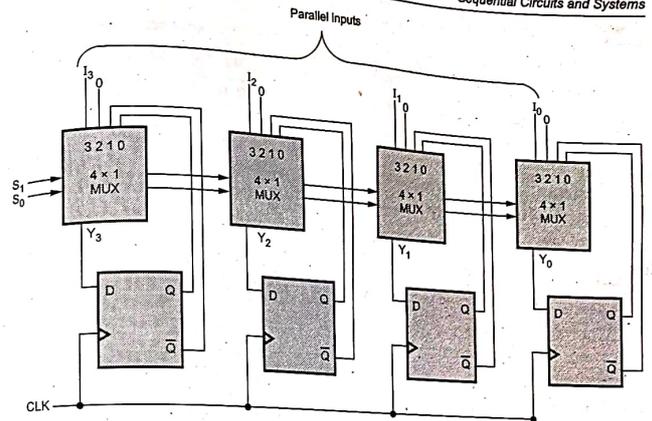


Fig. 5.8.16

$$\Delta t = N \times \frac{1}{f_c}$$

where N is the number of stages (i.e. flip-flops) and f_c is the clock frequency.

- An input pulse train appears at the output delayed by Δt .
- The amount of delay can be controlled by the clock frequency or by the number of flip-flops in the shift register.

5.8.4.2 Serial-to-Parallel Converter

- A Serial-In-Parallel-Out (SIPO) shift register can be used to convert data in the serial form to the parallel form.

5.8.4.3 Parallel-to-Serial Converter

- A Parallel-In-Serial-Out (PISO) shift register can be used to convert data in the parallel form to the serial form.

5.8.4.4 Shift Register Counters

- A shift register with the serial output connected back to the serial input is called **shift register counter**.
- The most common shift register counters are the ring counter and the Johnson counter.

5.8.4.5 Pseudo-Random Binary Sequence (PRBS) Generator

- A shift register can be used as a pseudo-random binary sequence generator.
- A suitable feedback is used to generate pseudo-random sequence.
- The term random here means that the outputs do not cycle through a normal binary count sequence.
- The term pseudo here refers to the fact that the sequence is not truly random because it does cycle through all possible combinations once every $2^n - 1$ clock cycles, where n represents the number of shift register stages (number of flip-flops).

5.8.4.6 Sequence Generator

- The shift register can be used to generate a particular bit pattern repetitively.

The Fig. 5.8.17 shows the basic block diagram of a sequence generator.

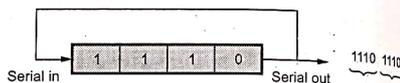


Fig. 5.8.17 4-bit sequence generator

- Left most flip-flop input accepts the serial input and the right most flip-flop gives serial data output.
- The serial data output signal is connected as a serial data in.
- On every clock pulse the data shift operation takes place.
- The loaded bit pattern at the serial output is in a sequence.
- Same bit pattern is again loaded in the register since serial output is connected serial in of the register. Thus, the circuit generates a particular bit pattern repetitively.

5.8.4.7 Sequence Detector

- The shift register can be used to detect the desired sequence.
- The detection process requires two registers : one register stores the bit pattern to be detected i.e. R_1 and other register accepts the input data stream i.e. R_2 .
- Input data stream enters a shift register as serial data in and leaves as serial out.
- In every clock cycle, bit-wise comparisons of these two registers are done using EX-NOR gates as shown in the Fig. 5.8.18. The two-input EX-NOR gate gives logic high output when both inputs are either low or high, i.e. when both are equal. When outputs of all the EX-NORs gates are logic high we can say that all bits are matched and hence the desired bit pattern is detected. The final output which indicates that the pattern is detected is taken from four-input AND gate.

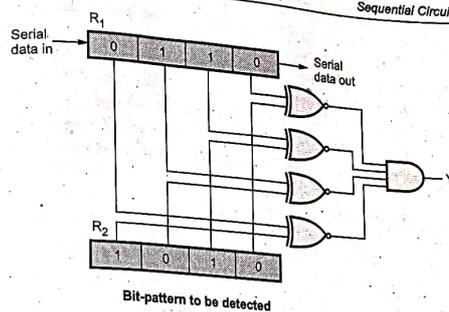


Fig. 5.8.18 4-bit sequence detector

- The 4-bit sequence detector shown in Fig. 5.8.18 can be made programmable by loading the desired 4-bit data in the register R_2 .

Review Questions

1. Define register. GTU : Dec.-13, Mark 1
2. What is buffer register ?
3. Draw and explain 4-bit controlled buffer register.
4. List the basic types of shift registers in terms of data movements.
5. Draw the logical diagram of a 4-bit shift register. Explain how shift left and shift right operations are performed.
6. What is the difference between serial and parallel transfer ? What type of registers are used in each case ? GTU : May-13, Marks 7
7. Explain modes of operation of shift register.
8. Explain with a neat diagram working of parallel in serial out 4-bit shift register. Draw necessary timing diagram.
9. Design a circuit for 4-bits parallel register with load with D flip-flops. Load input decides whether to load new input or to apply no change conditions. GTU : May-14, Marks 7
10. Explain the operation of 4-bit SISO shift register using D flip-flops. GTU : Summer-18, Marks 4
11. Draw and explain SISO and PIPO for the shift register.
12. Draw and explain the circuit diagram of 3-bit register with the following facility
i) Parallel in serial output ii) Reset.
13. Explain how shift registers are used as serial to parallel converters.

14. Draw and explain 5-bit shift register having parallel in and serial in (left to right) facilities. Explain any one application of such register.
15. Explain serial to parallel shift register with neat circuit diagram and timing diagram.
16. Explain with the help of neat diagram, the operation of 3-bit bidirectional shift register.
17. Draw the circuit and explain the function of 4-bit bidirectional shift register.
18. Explain with the help of neat diagram the operation of 4-bit universal shift register.
19. Draw and explain 4-bit shift register having shift left, shift right and parallel in facilities. Use suitable multiplexers in your circuit. Explain any one application of such register.
20. Design 4-bit shift register with the following facilities :
 - i) Shift-left (if $L1 = 0$ and $L0 = 0$)
 - ii) Shift-right (if $L1 = 0$ and $L0 = 1$)
 - iii) Parallel-in (if $L1 = 1$ and $L0 = 1$)
 Control signals 'L1 L0' will select one of the possible operation.
21. State applications of shift registers.
22. With neat sketch design 4-bit bidirectional shift register.
23. Explain serial transfer w.r.t. shift register with suitable example.

GTU : Summer-15, Marks 7

GTU : Winter-18, Marks 4

5.9 Counters

GTU : May-12, 14, Dec.-12, 13, Summer-15, 16, 18, Winter-14, 15

- A counter is a register capable of counting the number of clock pulses arriving at its clock input.
- Count represents the number of clock pulses arrived.
- On arrival of each clock pulse, the counter is incremented by one.
- In case of down counter, on arrival of each clock pulse, it is decremented by one.
- The Fig. 5.9.1 shows the logic symbol of a binary counter.

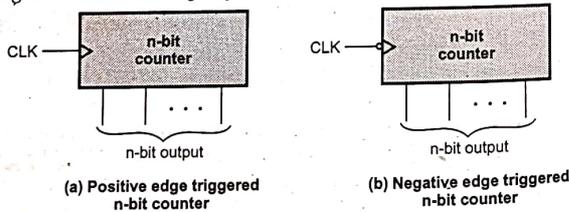


Fig. 5.9.1 Logic symbol of counter

- External clock is applied to the clock input of the counter.
- The counter can be positive edge triggered or negative edge triggered.
- The n-bit binary counter has n flip-flops and it has 2^n distinct states of outputs.

- For example, 2-bit counter has 2 flip-flops and it has $4(2^2)$ distinct states : 00, 01, 10 and 11.
- The 3-bit binary counter has 3 flip-flops and it has $8(2^3)$ distinct states : 000, 001, 010, 011, 100, 101 110 and 111.
- The maximum count that the binary counter can count is $2^n - 1$.
- For example, in 2-bit binary counter, the maximum count is $2^2 - 1 = 3$ (11 in binary).
- After reaching the maximum count the counter resets to 0 on arrival of the next clock pulse and it starts counting again.

Synchronous Counter

- When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called synchronous counter.

Asynchronous Counter / Ripple Counter

- A binary asynchronous/ripple counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the clock input of the next higher-order flip-flop.
- The flip-flop holding the least significant bit receives the incoming clock pulses.
- The Table 5.9.1 shows the comparison between synchronous and asynchronous counters.

Sr. No.	Asynchronous counters	Synchronous counters
1.	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2.	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3.	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip-flops increases in the given design.

Table 5.9.1 Synchronous Vs Asynchronous counters

Modulus of Counter

- The total number of counts or stable states a counter can indicate is called 'Modulus'.

- The modulus of a four-stage counter would be 16_{10} , since it is capable of indicating 0000_2 to 1111_2 .
- The term 'modulo' is used to describe the count capability of counters.
- For example, mod 6 counter goes through states 0 to 5 and mod 4 counter goes through states 0 - 3.

Example 5.9.1 Draw the state diagram of MOD-10 counter.

Solution :

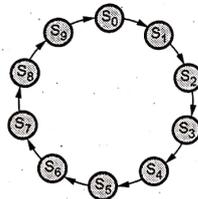


Fig. 5.9.2

Example 5.9.2 Assume that the 5-bit binary counter starts in the 00000 state. What will be the count after 144 input pulses ?

Solution : $(144)_{10} = (1001\ 0000)_2$

Since counter is a 5-bit counter, it resets after $2^5 = 32$ clock pulses.

$$\begin{array}{r} 4 \\ 32 \overline{)144} \\ \underline{-128} \\ 16 \end{array}$$

Therefore, counter resets four times and then it counts remaining 16 clock pulses. Thus, the count will be $(10000)_2$, i.e., 16 in decimal.

In general,

$$\text{Count} = \text{Remainder of } \left[\frac{\text{Number of input pulses}}{2^n} \right] \text{ in binary}$$

where n = Number of counter bits

5.9.1 Ripple / Asynchronous Counters

- A binary ripple/asynchronous counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the clock input of the next higher-order flip-flop.

- The flip-flop holding the least significant bit receives the incoming clock pulses.
- A complementing flip-flops can be obtained from a JK flip-flop with the J and K inputs tied together as shown in the Fig. 5.9.3 or from a T flip-flop.
- A third alternative is to use a D flip-flop with the complement output connected to the D input.
- The D input is always the complement of the present state and the next clock pulse will cause the flip-flop to complement.

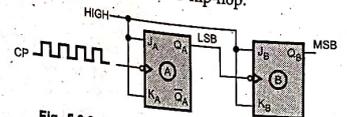


Fig. 5.9.3 (a) A two-bit asynchronous binary counter

- Fig. 5.9.3 (a) shows 2-bit asynchronous counter using JK flip-flops.
- The clock signal is connected to the clock input of only first stage flip-flop.
- The clock input of the second stage flip-flop is triggered by the Q_A output of the first stage.
- Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse and a transition of the Q_A output of first stage can never occur at exactly the same time. Therefore, the two flip-flops are never simultaneously triggered, which results in asynchronous counter operation.
- Fig. 5.9.3 (b) shows the timing diagram for two-bit asynchronous counter. It illustrates the changes in the state of the flip-flop outputs in response to the clock.
- J and K input of JK flip-flops are tied to logic HIGH hence output will toggle for each negative edge of the clock input.

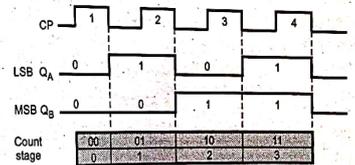


Fig. 5.9.3 (b) Timing diagram for the counter of Fig. 5.9.3 (a)

Example 5.9.3 Extend the counter shown in Fig. 5.9.3 (a) for 3-stages, and draw output waveforms.

Solution : In Fig. 5.9.4 (b), timing diagram for 3-bit asynchronous counter we have not considered the propagation delays of flip-flops, for simplicity. If we consider the propagation delays of flip-flops we get timing diagram as shown in Fig. 5.9.5.

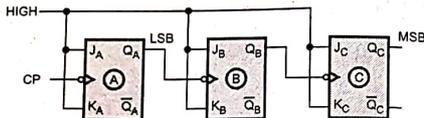


Fig. 5.9.4 (a) Logic diagram

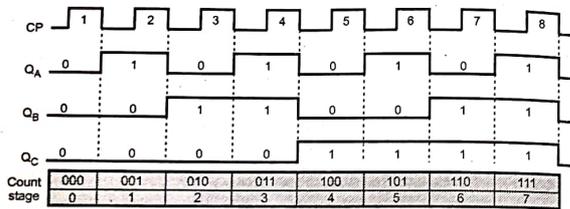


Fig. 5.9.4 (b) Output waveforms for 3-bit asynchronous counter

The timing diagram shows propagation delays. We can see that propagation delay of the first stage is added in the propagation delay of second stage to decide the transition time for third stage. This cumulative delay of an asynchronous counter is a major disadvantage in many applications because it limits the rate at which the counter can be clocked and creates decoding problems.

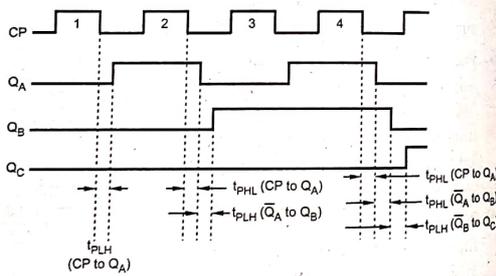


Fig. 5.9.5 Propagation delays in a ripple clocked binary counter

Example 5.9.4 Draw the logic diagram for 3-stage asynchronous counter with negative edge triggered flip-flops.

GTU : Summer-18, Marks 4

Solution : When flip-flops are negatively edge triggered, the Q output of previous stage is connected to the clock input of the next stage. Fig. 5.9.6 shows 3-stage asynchronous counter with negative edge triggered flip-flops.

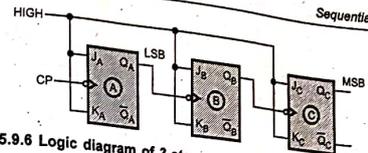


Fig. 5.9.6 Logic diagram of 3-stage negative edge triggered counter

Example 5.9.5 A counter has 14 stable states 0000 through 1101. If the input frequency is 50 kHz, what will be its output frequency?

Solution :
$$\frac{50 \text{ kHz}}{14} = 3.57 \text{ kHz}$$

Example 5.9.6 The t_{pd} for each flip-flop is 50 ns, determine the maximum operating frequency for MOD-32 ripple counter.

Solution : We know that MOD-32 uses five flip-flops. With $t_{pd} = 50 \text{ ns}$, the f_{max} for ripple counter can be given as,

$$f_{max} (\text{ripple}) = \frac{1}{5 \times 50 \text{ ns}} = 4 \text{ MHz}$$

Example 5.9.7 Draw the logic diagram for 4-stage asynchronous counter with positive edge triggered flip-flops. Also draw necessary timing diagram. Is there any frequency division concept in it.

Solution : When flip-flops are positive edge triggered, the Q output of previous stage is connected to the clock input of the next stage. Fig. 5.9.7 shows 4-stage asynchronous counter with positive edge triggered flip-flops.

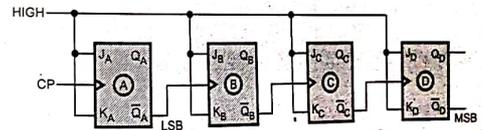


Fig. 5.9.7 Logic diagram of 4-stage positive edge triggered ripple counter

The Fig. 5.9.8 shows the timing diagram for 4-bit ripple up counter using positive edge triggered JK-FFs.

From the timing diagram we can observe that

- Frequency at output $Q_A = \frac{F_{CLK}}{2}$
- Frequency at output $Q_B = \frac{Q_A}{2} = \frac{F_{CLK}}{4}$

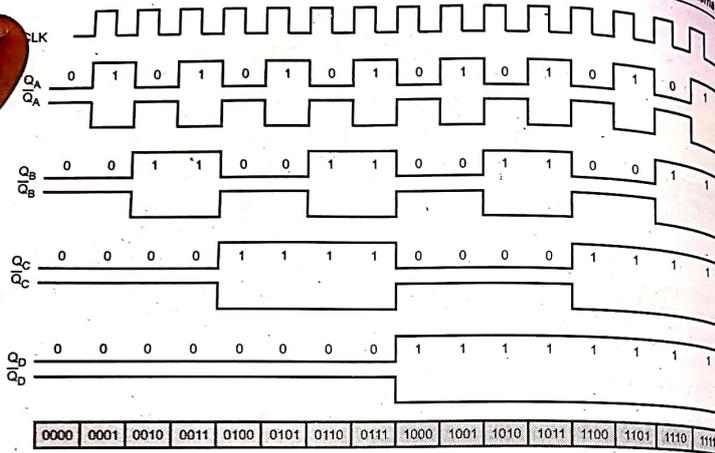


Fig. 5.9.8

- Frequency at output $Q_C = \frac{Q_B}{2} = \frac{Q_A}{4} = \frac{F_{CLK}}{8}$
- Frequency at output $Q_D = \frac{Q_C}{2} = \frac{Q_B}{4} = \frac{Q_A}{8} = \frac{F_{CLK}}{16}$

In general we can say that the frequency at the MSB output of counter is $\frac{F_{CLK}}{2^N}$ where N represents number of stages/bits of the counter.

5.9.1.1 Asynchronous / Ripple Down Counter

- The down counter will count downward from a maximum count to zero.

• The Fig. 5.9.9 shows the 4-bit asynchronous down counter using JK flip-flops.

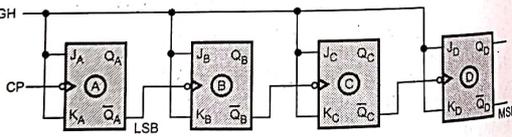


Fig. 5.9.9 4-bit asynchronous down counter

- The clock signal is connected to the clock input of only first flip-flop.
- The clock input of the remaining flip-flops is triggered by the \bar{Q}_A output of the previous stage instead of Q_A output of the previous stage.

- The Fig. 5.9.10 shows the timing diagram for 4-bit asynchronous down counter. It illustrates the changes in the state of the flip-flop outputs in response to the clock.

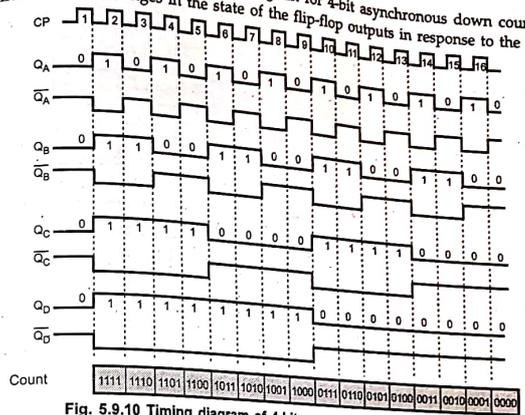


Fig. 5.9.10 Timing diagram of 4-bit asynchronous down counter

- The J and K inputs of JK flip-flops are tied to logic HIGH hence output will toggle for each negative edge of the clock input.
- Down counters are not as widely used as up counters. They are used in situations where it must be known when a desired number of input pulses has occurred. In these situations the down counter is preset to the desired number and then allowed to count down as the pulses are applied. When the counter reaches the zero state it is detected by a logic gate whose output then indicates that the preset number of pulses have occurred.

Example 5.9.8 For the ripple counter shown in Fig. 5.9.11, show the complete timing diagram for eight clock pulses, showing the clock, Q_0 and Q_1 waveforms.

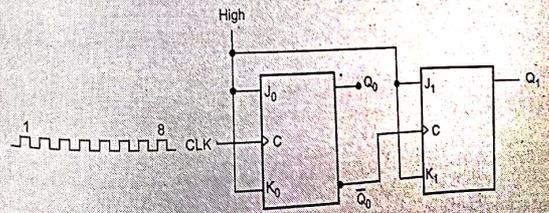


Fig. 5.9.11

Solution :

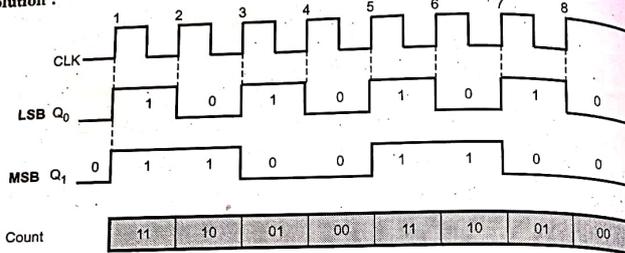


Fig. 5.9.11 (a)

5.9.1.2 Asynchronous Up / Down Counter

- To form an asynchronous up/down counter one control input say M is necessary to control the operation of the up/down counter.
- When M = 0, the counter will count up and when M = 1, the counter will count down. To achieve this the M input should be used to control whether the normal flip-flop output (Q) or the inverted flip-flop output (\bar{Q}) is fed to drive the clock signal of the successive stage flip-flop, as shown in Fig. 5.9.12 (a).
- The truth table is shown in Fig. 5.9.12 (b).

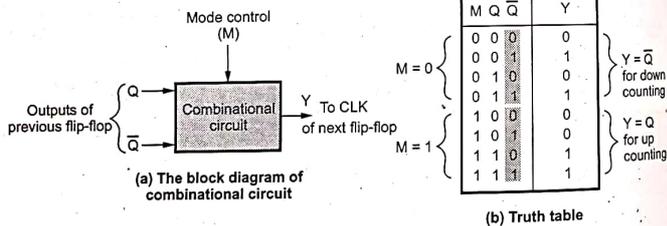


Fig. 5.9.12

- Fig. 5.9.14 shows the 3-bit up/down counter that will count from 000 up to 111 when the mode control input M is 1 and from 111 down to 000 when mode control input M is 0.
- A logic 1 on M enables AND gates 1 and 2 and disables AND gates 3 and 4. This allows the Q_A and Q_B outputs to drive the clock inputs of their respective next stages. So that counter will count up.

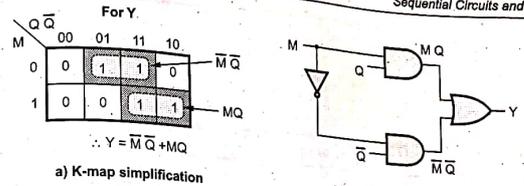


Fig. 5.9.13

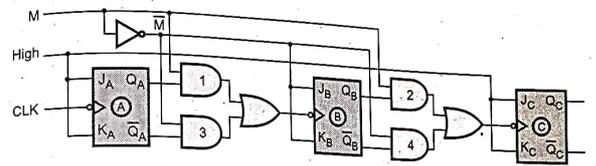


Fig. 5.9.14 3-bit asynchronous up/down counter

- When M is logic 0, AND gates 1 and 2 are disabled and AND gate 3 and 4 are enabled. This allows the Q_A and Q_B outputs to drive the clock inputs of their respective next stages so that counter will count down.
- Fig. 5.9.15 shows the timing diagram for 3-bit up/down ripple counter. (See Fig. 5.9.15 on next page)

Example 5.9.9 Design a 4-bit up/down ripple counter with a control for up/down counting.

Solution : The 4-bit counter needs four flip-flops. The circuit for 4-bit up/down ripple counter is similar to 3-bit up/down ripple counter except that 4-bit counter has one more flip-flop and its clock driving circuiting.

The Fig. 5.9.16 shows the 4-bit up/down ripple counter.

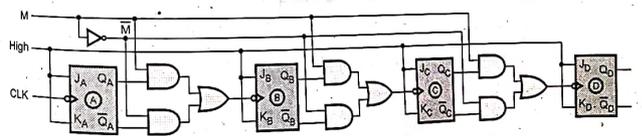


Fig. 5.9.16 4-bit asynchronous up/down counter

5.9.1.3 Decoding Gates

- Decoding gates are used to indicate whether counter has reached to particular state.

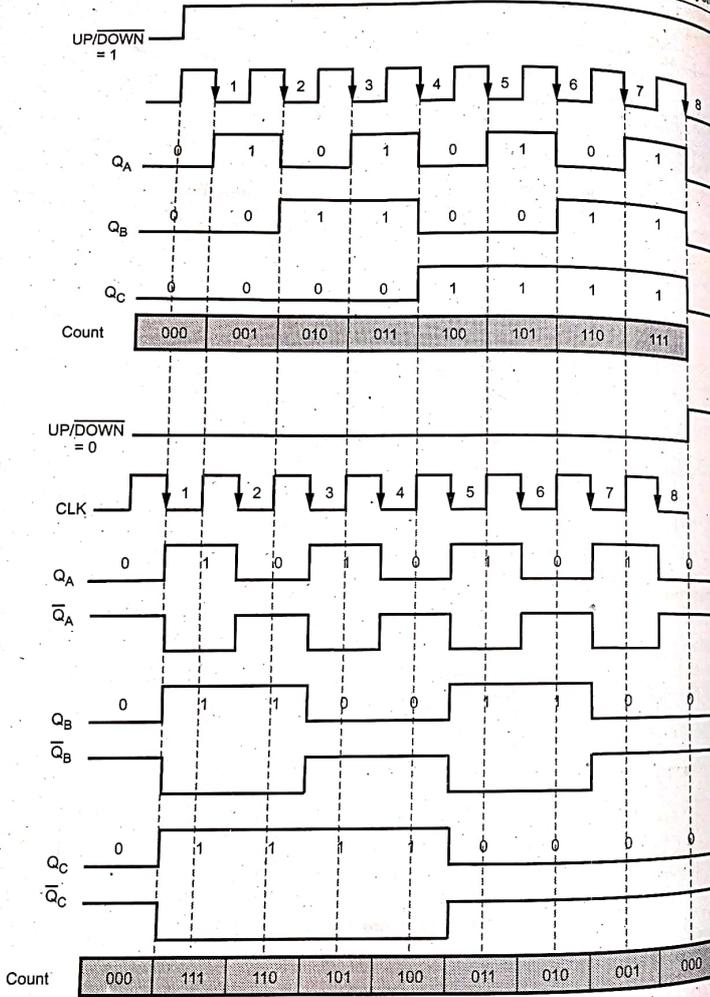


Fig. 5.9.15 Timing diagram for 3-bit UP/ DOWN ripple counter

- The outputs of the counter are connected to the AND gate as inputs and the output of the AND gate goes high for particular state.
- As shown in Fig. 5.9.17 (a), the output of decoding gate goes high when counter outputs are C = 1, B = 1 and A = 1.
- As shown in Fig. 5.9.17 (b) the output of decoding gate goes high when counter outputs are C = 1, B = 0 and A = 0.

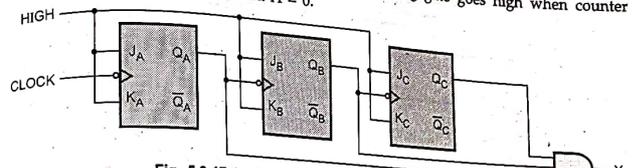


Fig. 5.9.17 (a) Decoding gate to indicate state 7 (111)

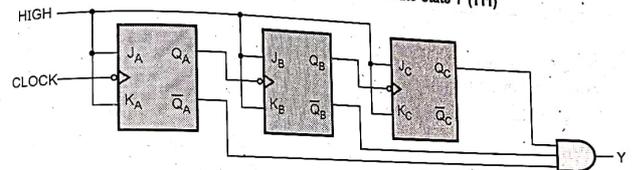


Fig. 5.9.17 (b) Decoding gate to indicate state 4 (100)

- We can connect corresponding outputs to decoding gate inputs to indicate desired state.
- The Fig. 5.9.18 gives these connections for all possible state detection for 3-bit counter.

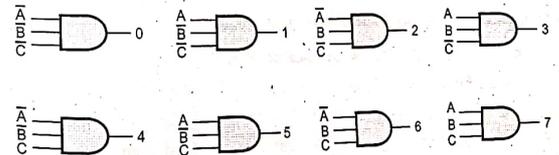


Fig. 5.9.18 Decoding gate connections

5.9.1.4 Problem Faced by Ripple Counters (Glitch Problem)

- Due to the propagation delay the output flip-flop is delayed by time t_p .
- Fig. 5.9.19 shows the waveform of the circuit which decodes state 7.

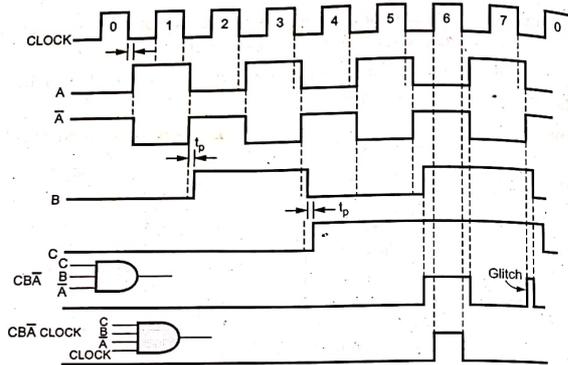


Fig. 5.9.19 Elimination of glitch

- Here, the output of flip-flop A triggers the flip-flop B, hence the B waveform is delayed by one flip-flop delay time (t_p) from the negative transition of A.
- The C waveform is delayed by t_p from each negative transition of B.
- At point X, A goes low (\bar{A} goes high); however, because of flip-flop delay time, B does not go low until point Y. Thus between points X and Y we have the condition $C = 1, B = 1$ and $A = 1$. As a result, the output is high between points X and Y. This undesirable output is known as glitch.
- We can avoid the glitch on the output waveform by connecting clock as a fourth input to the decoding gate along with inputs A, B and C. This is illustrated in the Fig. 5.9.19.

5.9.2 Design of Ripple (Asynchronous) Counters

Steps involved in the design of asynchronous counter

1. Determine the number of flip-flops needed.
2. Choose the type of flip-flops to be used : T or JK. If T flip-flops are used connect T input of all flip-flops to logic 1. If JK flip-flops are used connect both J and K inputs of all flip flops to logic 1. Such connection toggles the flip-flop output on each clock transition.
3. Write the truth table for the counter.
4. Derive the reset logic by K-map simplification.
5. Draw the logic diagram.

Example 5.9.10 Design BCD (mod-10) ripple counter using JK flip-flop.

GTU : May-14, Marks 7

Solution :

- Step 1 :** Determine the number of flip-flops needed. The BCD counter goes through states 0-9, i.e. total 10 states. Thus, $N = 10$ and for $2^n \geq N$, we need $n = 4$, i.e. 4 flip-flops required.
- Step 2 :** Type of flip-flops to be used : JK
- Step 3 :** Write the truth table for the counter

CLK	A	B	C	D	Output of reset logic Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
-	1	0	1	0	0
-	1	0	1	1	0
-	1	1	0	0	0
-	1	1	0	1	0
-	1	1	1	0	0
-	1	1	1	1	0

Table 5.9.2 Truth table for BCD counter

Note : The reset input (CLR) of each Flip-Flop is active-low input. By making CLR input of all Flip-Flops logic 0, we can reset the counter. Thus reset logic is designed such a way that for invalid states, $Y = 0$ and counter resets.

Valid states

Invalid states

Step 4 : Derive reset logic

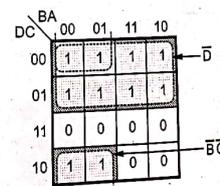


Fig. 5.9.20

Step 5 : Draw logic diagram.

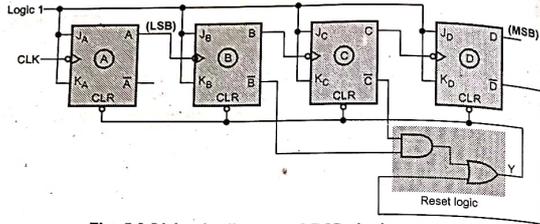


Fig. 5.9.21 Logic diagram of BCD ripple counter

Example 5.9.11 Design a 3-bit asynchronous ripple counter using T flip-flops and explain its operation.

Solution : The Fig. 5.9.22 shows a 3-bit asynchronous ripple counter using T flip-flops. As shown in Fig. 5.9.22, the clock input of only first stage flip-flop. The clock input of the second stage flip-flop is triggered by the QA output of the first stage and third stage flip-flop is triggered by the QA output of second stage. Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse and a transition of the QA output of previous stage can never occur at exactly the same time. Therefore, flip-flops are never simultaneously triggered, which results in asynchronous counter operation.

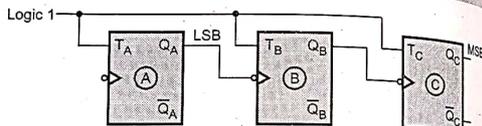


Fig. 5.9.22 3-bit asynchronous counter using T flip-flops

- Since, T input is connected to logic 1 each flip-flop toggles at clock input. The Fig. 5.9.23 shows the timing diagram for 3-bit asynchronous counter.

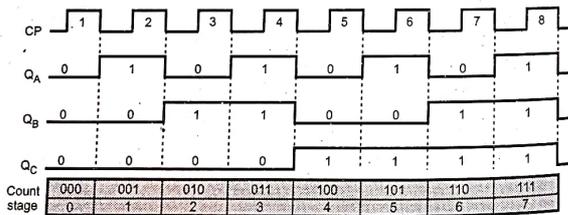


Fig. 5.9.23 Output waveforms for 3-bit asynchronous counter

Example 5.9.12 Design mod 6 ripple counter using T flip-flops.

Solution :

- Step 1 :** Determine the number of flip-flop required. Here, counter goes through 0 - 5 states, i.e., total 6 states. Thus $N = 6$ and for $2^n \geq N$ we need $n = 3$, i.e. 3 flip-flops.
- Step 2 :** Type of flip-flops to be used : T
- Step 3 :** Write the truth table for counter
- Step 4 :** Derive reset logic

CLK	C	B	A	Output of reset logic Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
-	1	1	0	0
-	1	1	1	0

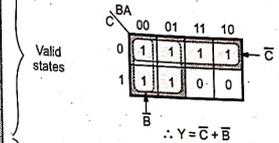


Fig. 5.9.24

Fig. 5.9.25

Step 5 : Draw logic diagram

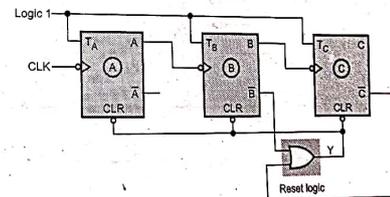


Fig. 5.9.26

Example 5.9.13 Design ripple counter for state diagram shown.

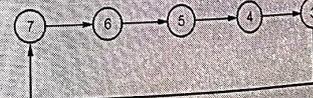


Fig. 5.9.27

Solution :

Step 1 : Determine the number of flip-flops needed.

We know that $2^n \geq N$. Here, $N = 8 \therefore n = 3$ i.e. 3 flip-flops needed.

Step 2 : Type of flip-flops to be used : JK

Step 3 : Write truth table for counter.

CLK	C	B	A	Output of reset logic Y
0	1	1	1	1
1	1	1	0	1
2	1	0	1	1
3	1	0	0	1
4	0	1	1	1
5	0	1	0	0
6	0	0	1	0
7	0	0	0	0

Table 5.9.3 Truth table

Step 5 : Draw logic diagram.

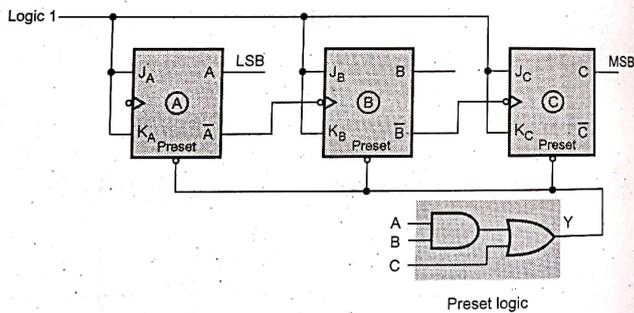


Fig. 5.9.29

- Since it is a down counter, the clock of the next flip-flop is given by the \bar{Q} output of the previous flip-flop.

5.9.3 Synchronous Counters

- When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called as synchronous counter.

5.9.3.1 2-bit Synchronous Binary Up Counter

- Fig. 5.9.30 shows two stage synchronous counter.

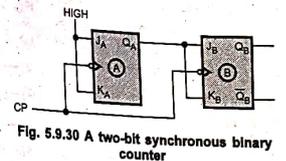


Fig. 5.9.30 A two-bit synchronous binary counter

- Clock signal is connected in parallel to clock inputs of both the flip-flops.
- The Q_A output of first stage is used to drive the J and K inputs of the second stage.
- Initially, we assume that the $Q_A = Q_B = 0$.
- When positive edge of the first clock pulse is applied, flip-flop A will toggle because $J_A = K_A = 1$, whereas flip-flop B output will remain zero because $J_B = K_B = 0$.
- After first clock pulse $Q_A = 1$ and $Q_B = 0$.
- At negative going edge of the second clock pulse both flip-flops will toggle because they both have a toggle condition on their J and K inputs ($J_A = K_A = J_B = K_B = 1$). Thus after second clock pulse, $Q_A = 0$ and $Q_B = 1$.
- At negative going edge of the third clock pulse flip-flop A toggles making $Q_A = 1$, but flip-flop B remains set i.e. $Q_B = 1$.
- Finally, at the leading edge of the fourth clock pulse both flip-flops toggle as their JK inputs are at logic 1. This results $Q_A = Q_B = 0$ and counter recycled back to its original state.
- The timing details of above operation is shown in Fig. 5.9.31.

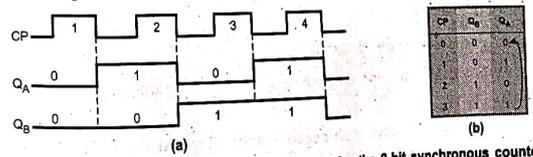


Fig. 5.9.31 Timing diagram and state sequence for the 2-bit synchronous counter

5.9.3.2 3-bit Synchronous Binary Up Counter

- Fig. 5.9.32 (a) shows 3-bit synchronous binary counter and its timing diagram.

- The state sequence for this counter is shown in Table 5.9.4.
- Looking at Fig. 5.9.32 (b), we can see that Q_A changes on each clock pulse as we progress from its original state to its final state and then back to its original state.
- Flip-flop A is held in the toggle mode by connecting J and K inputs to HIGH.
- Flip-flop B toggles, when Q_A is 1.
- When Q_A is 0, flip-flop B is in the no-change mode and remains in its present state.
- Looking at the Table 5.9.4 we can notice that flip-flop C has to change its state only when Q_B and Q_A both are at logic 1. This condition is detected by AND gate and applied to the J and K inputs of flip-flop C. Whenever both Q_A and Q_B are HIGH, the output of the AND gate makes the J and K inputs of flip-flop C HIGH and flip-flop C toggles on the following clock pulse. At all other times, the J and K inputs of flip-flop C are held LOW by the AND gate output and flip-flop does not change state.

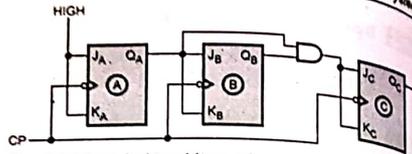


Fig. 5.9.32 (a) A three-bit synchronous binary counter

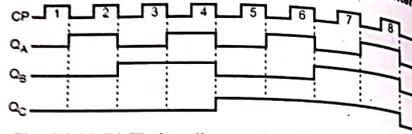


Fig. 5.9.32 (b) Timing diagram for 3-bit synchronous binary counter

CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 5.9.4 State sequence for 3-bit binary counter

5.9.3.3 4-bit Synchronous Binary Up Counter

- Fig. 5.9.33 (a) shows logic diagram and timing diagram for 4-bit synchronous binary counter.
- As counter is implemented with negative edge triggered flip-flops, the transitions occur at the negative edge of the clock pulse.
- In this circuit, first three flip-flops work same as 3-bit counter discussed previously.

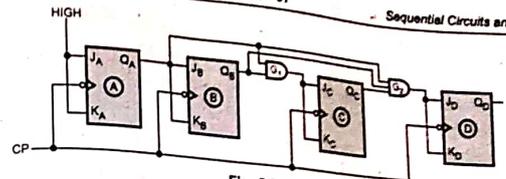


Fig. 5.9.33 (a)

- For the fourth stage, flip-flop has to change the state when $Q_A = Q_B = Q_C = 1$. This condition is decoded by 3-input AND gate C_2 . Therefore, when $Q_A = Q_B = Q_C = 1$, flip-flop D toggles and for all other times it is in no change condition.

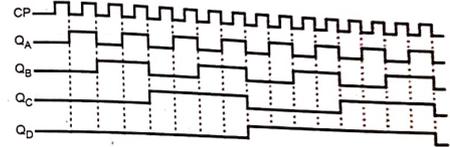


Fig. 5.9.33 (b) A 4-bit synchronous binary counter and timing diagram

Example 5.9.14 Determine f_{max} for the 4-bit synchronous counter if t_{pd} for each flip-flop is 50 ns and t_{pd} for each AND gate is 20 ns. Compare this with f_{max} for a MOD-16 ripple counter.

Solution : For a synchronous counter the total delay that must be allowed between input clock pulses is equal to flip-flop t_{pd} + AND gate t_{pd} . Thus $T_{clock} \geq 50 + 20 = 70$ ns and so the counter has

$$f_{max} = \frac{1}{70 \text{ ns}} = 14.3 \text{ MHz}$$

We know that MOD-16 ripple counter used four flip-flops. With flip-flop $t_{pd} = 50$ ns, the f_{max} for ripple counter can be given as,

$$f_{max} (\text{ripple}) = \frac{1}{4 \times 50 \text{ ns}} = 5 \text{ MHz}$$

5.9.3.4 Synchronous Down and Up / Down Counters

- A parallel/synchronous down counter can be constructed by using the inverted FF outputs to drive the following JK inputs.

- For example, the parallel up counter of Fig. 5.9.33 (a) can be converted to a down counter by connecting the \bar{Q}_A , \bar{Q}_B , \bar{Q}_C and \bar{Q}_D outputs in place of Q_A , Q_B , Q_C and Q_D respectively.
- The counter will then proceed through the following sequence as input pulses are applied :
- To form a parallel up/down counter the control input (UP/DOWN) is used to control whether the normal flip-flop outputs or the inverted flip-flop outputs are fed to the J and K inputs of the following flip-flops.
- A logic 1 on the Up/Down enables AND gates 1 and 2 and disables AND gates 3 and 4. This allows the Q_A and Q_B outputs through to the J and K inputs of the next flip-flops so that the counter will count up as pulses are applied.

1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

Fig. 5.9.34

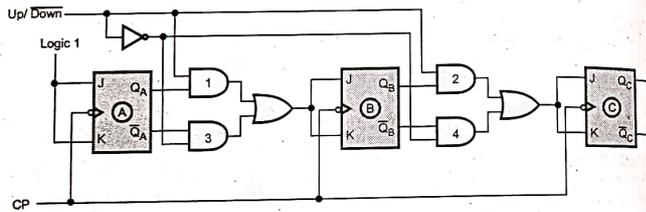


Fig. 5.9.35 3-bit synchronous / parallel up / down counter

- When Up/Down line is logic 0, AND gates 1 and 2 are disabled and AND gates 3 and 4 are enabled. This allows the \bar{Q}_A and \bar{Q}_B outputs through to the J and K inputs of the next flip-flops so that the counter will count down as pulses are applied.
- Fig. 5.9.36 shows the timing diagram for 3-bit up-down counter.

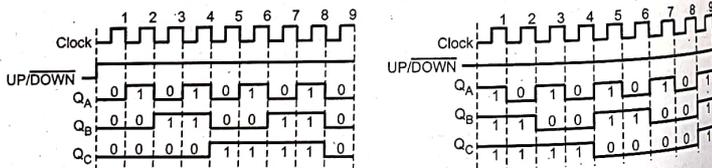


Fig. 5.9.36 Timing diagram

5.9.4 Design of Synchronous Counters

- Determine the number of flip-flops needed. If n represents number of flip-flops $2^n \geq$ number of states in the counter.
- Choose the type of flip-flops to be used.
- Using excitation table for selected flip-flop determine the excitation table for the counter.
- Use K-map or any other simplification method to derive the flip-flop input functions.
- Draw the logic diagram.

Example 5.9.15 Design a MOD-5 synchronous counter using JK flip-flops and implement it. Also draw the timing diagram.

Solution :

Step 1 : Determine the number of flip-flop needed

Flip-flops required are

$$2^n \geq N$$

Here $N = 5 \therefore n = 3$ i.e. three flip-flops are required.

Step 2 : Type of flip-flop to be used : JK

Step 3 : Determine the excitation table for the counter.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1

Table 5.9.5 Excitation table for JK flip-flop

Present state			Next state			Flip-flop inputs					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1

1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Table 5.9.6 Excitation table for counter

Step 4 : K-map simplification

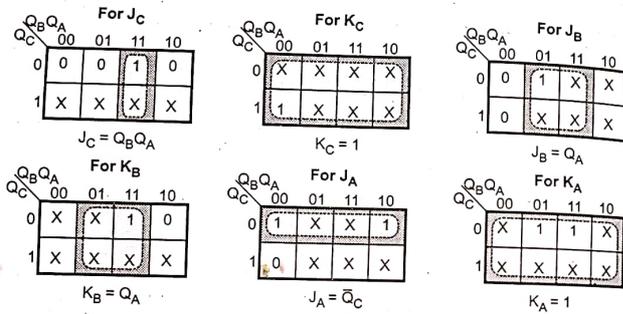


Fig. 5.9.37

Step 5 : Draw the logic diagram

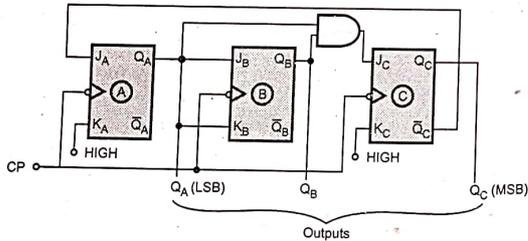


Fig. 5.9.37 (a) MOD-5 synchronous counter

Timing diagram

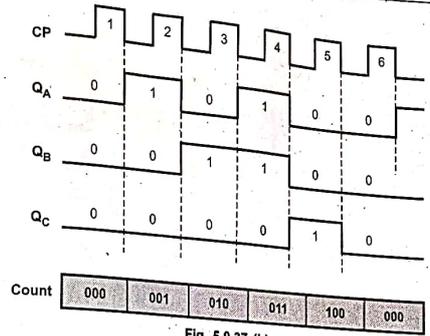


Fig. 5.9.37 (b)

Example 5.9.16 Design divide by 6 counter using T-flip-flops. Write state table and reduce the expression using K-map.

Solution : Step 1 : Determine the number of flip-flops needed.

For designing mod 6 counter using the formula

$$2^n \geq N$$

Here $N = 6 \therefore n = 3$ i.e. 3 flip-flops are required.

Step 2 : Type of flip-flops to be used : T

Step 3 : Determine the excitation table for counter.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 5.9.7 Excitation table for T-flip-flop

CP	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	0	0	0	1	0	1

Table 5.9.8 Excitation table for counter

Step 4 : K-map simplification.

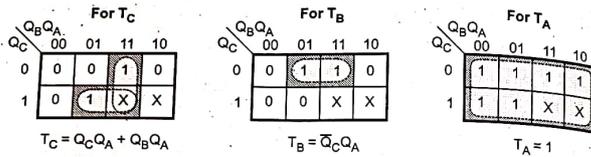


Fig. 5.9.38

Step 5 : Draw the logic diagram.

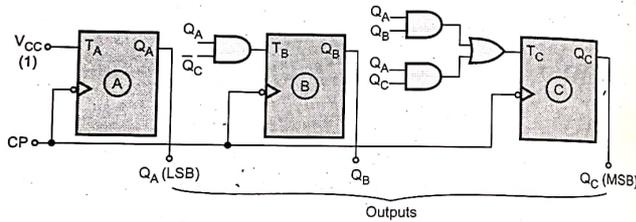


Fig. 5.9.38 (a) Logic diagram

Example 5.9.17 Design a synchronous decade counter using D flip-flop.

Solution : The decade counter is a mod-10 counter. It has ten states : 0 - 9.

Step 1 : Determine the number of flip-flops needed.

We know that $2^n \geq N$. Here, $N = 10 \therefore n = 4$ i.e. 4 flip-flops needed.

Step 2 : Types of flip-flops to be used : D

Step 3 : Determine the excitation table for counter.

Present state				Next state			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1

0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	1	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Table 5.9.9 Excitation table for counter

Step 4 : K-map simplification

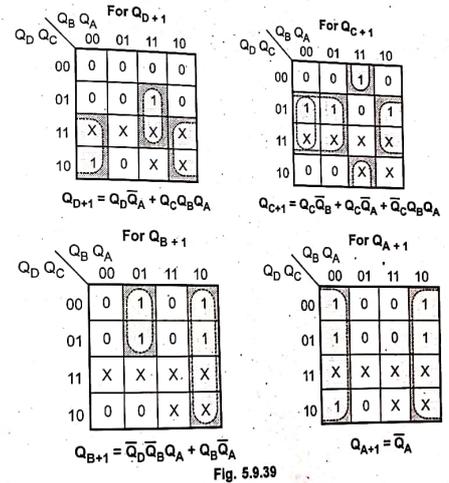


Fig. 5.9.39

$$Q_{D+1} = Q_D \bar{Q}_A + Q_C Q_B Q_A$$

$$Q_{D+1} = Q_D \bar{Q}_A + Q_C Q_B Q_A$$

$$Q_{C+1} = Q_C \bar{Q}_B + Q_C \bar{Q}_A + Q_C Q_B Q_A$$

$$Q_{B+1} = \bar{Q}_D \bar{Q}_B Q_A + Q_B \bar{Q}_A$$

$$Q_{A+1} = \bar{Q}_A$$

Step 5 : Draw the logic diagram.

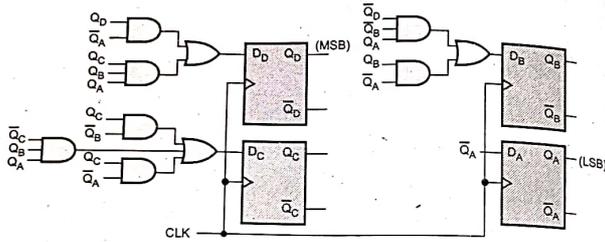


Fig. 5.9.39 (a) Logic diagram

Example 5.9.18 Design a BCD up/down counter using SR flip-flops.

Solution :

Step 1 : Number of flip-flops needed = 4

Step 2 : Flip-flops to be used = SR

Step 3 : Excitation table for counter

I/P	Present state				Next state				Flip-flop inputs								
U/D	A	B	C	D	A+	B+	C+	D+	S _A	R _A	S _B	R _B	S _C	R _C	S _D	R _D	
0	0	0	0	0	0	1	0	0	1	1	0	0	x	0	x	1	0
0	0	0	0	1	0	0	0	0	0	0	x	0	x	0	1	0	1
0	0	0	1	0	0	0	0	1	0	1	0	x	0	1	1	0	0
0	0	0	1	1	0	0	1	0	0	1	0	x	1	0	0	1	0
0	0	1	0	0	0	0	1	1	0	1	0	1	1	0	1	0	0
0	0	1	0	1	0	1	0	0	0	1	1	0	0	1	0	1	0
0	0	1	1	0	0	1	0	1	0	1	1	0	0	1	1	0	0
0	0	1	1	1	0	1	1	0	0	1	1	0	1	0	1	0	0
0	1	0	0	0	0	1	1	1	0	1	1	0	1	0	1	0	0
0	1	0	0	1	1	0	0	0	x	0	0	1	0	1	0	1	0

1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	
1	0	0	0	1	0	0	0	1	0	0	1	0	0	1	0	0	1	
1	0	0	1	0	0	0	0	1	1	0	1	0	1	0	1	0	0	
1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	1	
1	0	1	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	
1	0	1	0	1	0	1	0	1	1	0	0	1	1	0	1	0	0	
1	0	1	1	0	0	0	1	1	1	1	0	1	1	0	1	0	0	
1	0	1	1	1	0	1	0	0	0	1	0	0	1	0	0	1	0	1
1	1	0	0	0	1	0	0	1	x	0	0	1	0	1	0	1	0	
1	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	0	

Table 5.9.10

Step 4 : K-map simplification

For S_A

M = U/D = 0

00	1	0	0	0
01	0	0	0	0
11	x	x	x	x
10	0	x	x	x

M = U/D = 1

00	0	0	0	0
01	0	0	1	0
11	x	x	x	x
10	x	0	x	x

For R_A

M = 0

00	0	x	x	x
01	x	x	x	x
11	x	x	x	x
10	1	0	x	x

M = 1

00	x	x	x	x
01	x	x	0	x
11	x	x	x	x
10	0	1	x	x

$S_A = \overline{M} \overline{A} \overline{B} \overline{C} \overline{D} + M \overline{B} \overline{C} \overline{D}$

$R_A = \overline{M} \overline{A} \overline{D} + M \overline{A} \overline{D}$

For S_B

M = 0

00	0	0	0	0
01	0	x	x	x
11	x	x	x	x
10	1	0	x	x

M = 1

00	0	0	1	0
01	x	x	0	x
11	x	x	x	x
10	0	0	x	x

$S_B = \overline{M} \overline{A} \overline{D} + M \overline{B} \overline{C} \overline{D}$

For R_B

M = 0

00	x	x	x	x
01	1	0	0	0
11	x	x	x	x
10	0	x	x	x

M = 1

00	x	x	0	x
01	0	0	1	0
11	x	x	x	x
10	x	x	x	x

$R_B = \overline{M} \overline{B} \overline{C} \overline{D} + M \overline{B} \overline{C} \overline{D}$

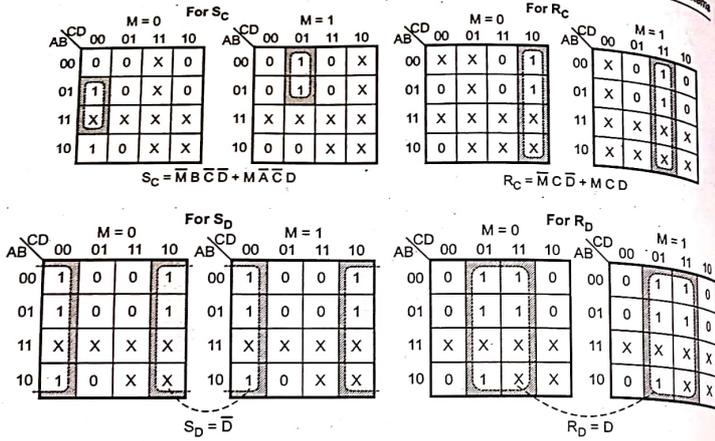


Fig. 5.9.40

Step 5 : Logic diagram

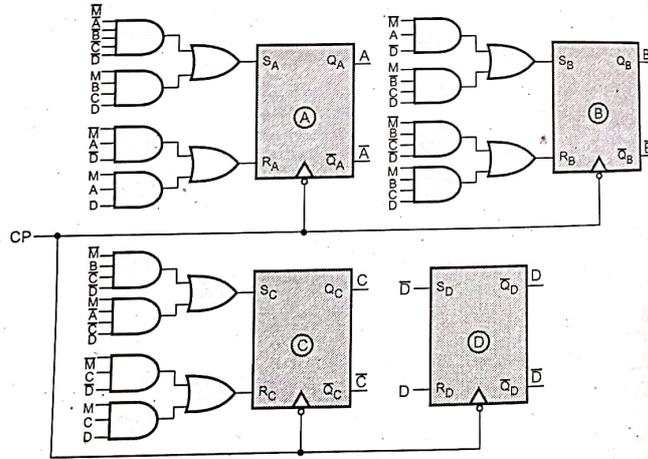


Fig. 5.9.41

Example 5.9.19 Design a mod-12 synchronous up counter using D flip-flop.

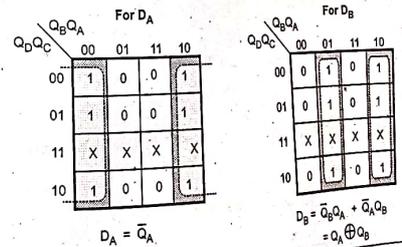
Solution : Mod-12 synchronous counter using D flip-flop.

Let, Number of flip-flop required = n
 $2^n \geq 12$
 $n = 4$

Excitation table

Present state		Next state					
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	0

K-map simplification



		For D _C				For D _D			
Q _D Q _C	Q _B Q _A	00	01	11	10	00	01	11	10
00		0	0	1	0	0	0	0	0
01		1	1	0	1	0	0	1	0
11		X	X	X	X	X	X	X	X
10		0	0	0	0	1	1	0	1

$$D_C = Q_C \bar{Q}_B + Q_C \bar{Q}_A + \bar{Q}_D \bar{Q}_C Q_B Q_A$$

$$D_D = Q_D \bar{Q}_B + Q_C Q_B Q_A + Q_D \bar{Q}_A$$

Logic diagram

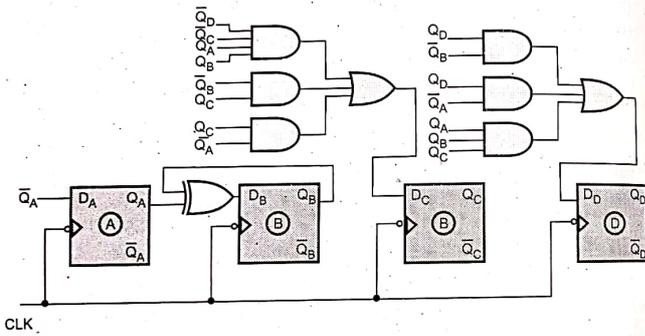


Fig. 5.9.42

Example 5.9.20 Design a synchronous BCD counter with JK flip-flops.

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Solution : The mod-10 counter has ten states : 0 to 9.

Step 1 : Determine the number of flip-flops needed.

We know that $2^n \geq N$. Here $N = 10 \therefore n = 4$ i.e. 4 flip-flops needed.

Step 2 : Types of flip-flops to be used : JK.

Step 3 : Determine the excitation table for counter.

Present state				Next state				Flip-flop inputs							
Q _D	Q _C	Q _B	Q _A	Q _{B+1}	Q _{C+1}	Q _{D+1}	Q _{A+1}	J _D	K _D	J _C	K _C	J _B	K _B	J _A	K _A
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	0	1	X
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Excitation table for counter

Step 4 : K-map simplification

		For J _D				For K _D			
Q _D Q _C	Q _B Q _A	00	01	11	10	00	01	11	10
00		0	0	0	0	X	X	X	X
01		0	0	1	0	X	X	X	X
11		X	X	X	X	X	X	X	X
10		X	X	X	X	0	1	X	X

$$J_D = Q_A Q_B Q_C$$

$$K_D = Q_A$$

		For J _C				For K _C			
Q _D Q _C	Q _B Q _A	00	01	11	10	00	01	11	10
00		0	0	1	0	X	X	X	X
01		X	X	X	X	0	0	1	0
11		X	X	X	X	X	X	X	X
10		0	0	X	X	X	X	X	X

$$J_C = Q_A Q_B \bar{Q}_D$$

$$K_C = Q_A Q_B$$

		For J _B				For K _B			
Q _D Q _C	Q _B Q _A	00	01	11	10	00	01	11	10
00		0	1	X	X	X	X	1	0
01		0	1	X	X	X	X	1	0
11		X	X	X	X	X	X	X	X
10		0	0	X	X	X	X	X	X

$$J_B = Q_A \bar{Q}_D$$

$$K_B = Q_A$$

		For J _A				For K _A							
Q _D	Q _C	Q _B	Q _A	00	01	11	10	Q _D	Q _C	Q _B	Q _A		
00	00	1	x	x	1	x	1	x	00	x	1	1	x
01	01	1	x	x	1	x	1	x	01	x	1	1	x
11	11	x	x	x	x	x	x	x	11	x	x	x	x
10	10	1	x	x	x	x	x	10	x	1	x	x	x

$J_A = 1$ $K_A = 1$

Step 5 : Logic diagram

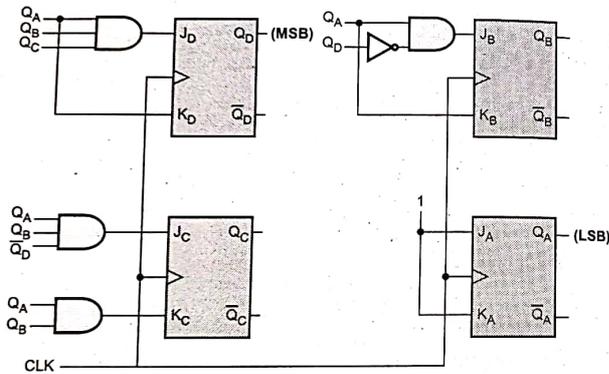


Fig. 5.9.43

Examples for Practice

Example 5.9.21 : Design a 3 bit synchronous counter using T flip-flop.

Example 5.9.22 : The following sequence is to be realized by a counter consisting of 3 JK FF's.

A ₁	0	0	0	0	1	1	0
A ₂	0	1	1	0	0	1	0
A ₃	0	1	0	1	1	0	0

Design the counter.

Example 5.9.23 : Design MOD-2 synchronous counter.

Example 5.9.24 : Design 3-bit up/down synchronous counter with directional mode control.

Example 5.9.25 : Design MOD-5 synchronous counter using T-flip flops.

Example 5.9.26 : Design 4-bit synchronous counter and explain its operation with truth table.

Example 5.9.27 : Design MOD-10 synchronous counter using J-K flip-flop and explain its operation.

5.9.5 Presettable Counters

- Presettable Counters can be preset to any desired starting count either asynchronously (independent of the clock signal) or synchronously (on the active transition of the clock signal).
- This presetting operation is also referred to as parallel loading the counter.
- Fig. 5.9.44 shows the logic circuit for a three-bit presettable parallel up counter
- The J, K and CLK inputs are wired for operation as a parallel up counter. The asynchronous PRESET and CLEAR inputs are wired to perform asynchronous presetting.

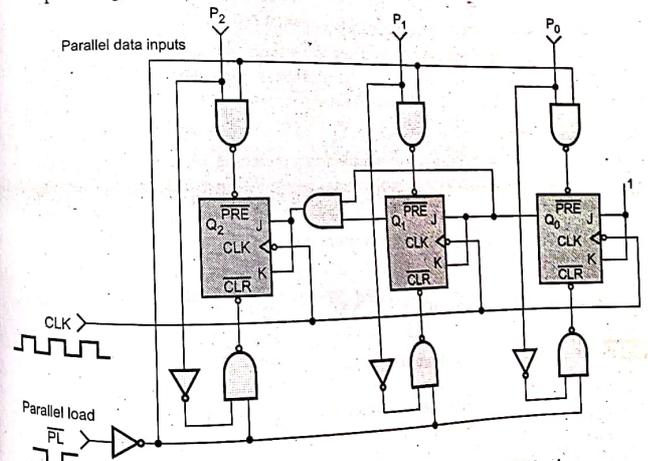


Fig. 5.9.44 Synchronous counter with asynchronous parallel load

- The counter is loaded with any desired count at any time by performing following steps :
 1. Apply the desired count to the parallel data inputs, P_2, P_1 and P_0 .
 2. Apply a LOW pulse to the PARALLEL LOAD input, \overline{PL} .
- The effect of the CLK input will be disabled as long as \overline{PL} is in its active-LOW state because each flip-flop will have one of its asynchronous inputs activated while $\overline{PL} = 0$.
- Once \overline{PL} returns HIGH, the flip-flops can respond to their CLK inputs and can resume the counting-up operation starting from the count that was loaded into the counter.
- For example, let's say that $P_2 = 0, P_1 = 1$ and $P_0 = 0$. While \overline{PL} is HIGH, these parallel data inputs have no effect.
- If clock pulses are present, the counter will perform the normal count-up operation.
- Now let's say that \overline{PL} is pulsed LOW when the counter is at the 100 count (i.e. $Q_2 = 1, Q_1 = 0$ and $Q_0 = 0$). This LOW at \overline{PL} will produce LOWs at the PRE input of Q_1 and at the CLR inputs of Q_2 and Q_0 so that the counter will go to the 010 count regardless of what is occurring at the CLK input. The count will hold at 010 until \overline{PL} is deactivated (returned HIGH); at that time the counter will resume counting up at each clock pulse from the count of 010.
- The asynchronous presetting is used by several counter ICs such as TTL 74ALS190, 74ALS191, 74ALS192 and 74ALS193 and the CMOS equivalents, 74HC190, 74HC191, 74CH192 and 74HC193.

Synchronous Presetting

- Some parallel counter ICs use synchronous presetting whereby the counter is preset on the active transition of the same clock signal that is used for counting.
- The logic level on the parallel load control input determines if the counter is preset with the applied input data at the next active clock transition.
- Examples of IC counters that use synchronous presetting include the TTL 74ALS160, 74ALS161, 74ALS162 and 74ALS163 and their CMOS equivalents, 74HC160, 74HC161, 74HC162 and 74HC163.

5.9.6 Design of Skipping State Counter

- The skipping state counter is a counter in which some states are missing in the sequence. For example, if counter goes through states : 0, 2, 4, 6 and 0 we can say that states 1, 3, 5 and 7 are missing, i.e. counter skips states 1, 3, 5 and 7. The skipping states are also known as **unused states**.

- In a skipping state counter, if the next state of some unused state is again an unused state and if by chance the counter happens to find itself in the unused states and never arrived at a used state then the counter is said to be in the lockout conditions. This is illustrated in the Fig. 5.9.45.
- The counter which never goes in lockout condition. This is illustrated in the Fig. 5.9.45.
- The circuit that goes in lockout condition is called **self starting counter**.
- To make sure that the counter will come to the initial state from any unused state, the additional logic circuit is necessary.
- To ensure that the lock out does not occur, the counter should be designed by forcing the next state to be the initial state from the unused states as shown in Fig. 5.9.46.
- For example, as shown in Fig. 5.9.46, actually it is not necessary to force all unused states into initial state. Forcing any one state is sufficient. Because if unused state. This will continue until it reaches the forced unused state. Once forced unused state is reached next state is used state, and circuit is lock free circuit. This is illustrated in Fig. 5.9.46 (b).

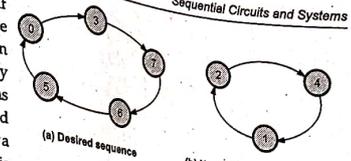


Fig. 5.9.45

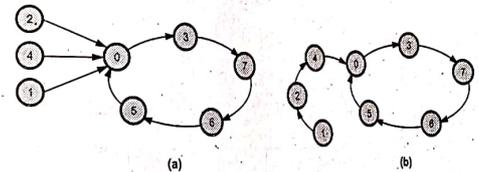


Fig. 5.9.46 State diagram for removing lockout

Example 5.9.28 Design a synchronous counter for
 $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4 \dots$
 Avoid lockout condition. Use JK type design.

Solution :

Step 1 : State diagram

Here, states 5, 2 and 0 are forced to go into 6, 3 and 1 state, respectively to avoid lockout condition.

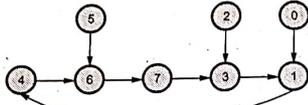


Fig. 5.9.47

Step 2 : Excitation table

Present states			Next states			Flip-flop inputs					
A	B	C	A ₊₁	B ₊₁	C ₊₁	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	1	0	0	1	X	0	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	0	0	1	0	X	X	1	X	0
1	0	0	1	1	0	X	0	1	X	0	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	1	1	X	1	X	0	X	0

Table 5.9.11

Step 3 : K-map simplification

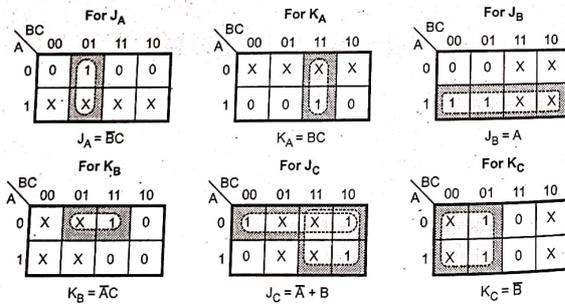


Fig. 5.9.48

Step 4 : Logic diagram

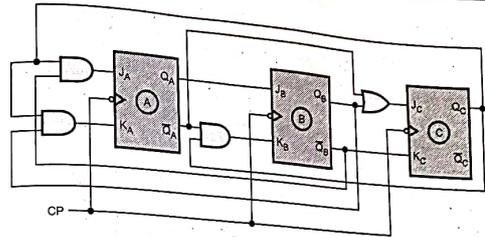
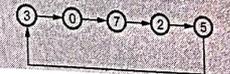


Fig. 5.9.49

Example 5.9.29 Design synchronous counter which will go through the following step, using JK flip-flop. (Avoid lock out condition.)



Solution : The Fig. 5.9.50 shows the state diagram for the given counter. To avoid lock-out condition states 1, 4 and 6 are force to enter into state 3.

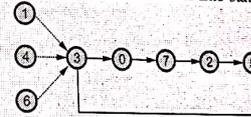


Fig. 5.9.50

• Flip-flop excitation table is as shown below.

Present state			Next state		
A	B	C	A ₊₁	B ₊₁	C ₊₁
0	0	0	1	1	1
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	0

Table 5.9.12

K-map simplification

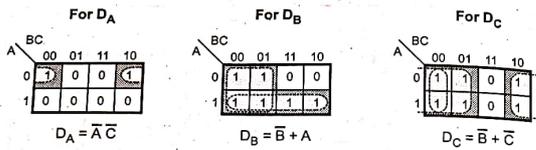


Fig. 5.9.51 (a)

Logic diagram

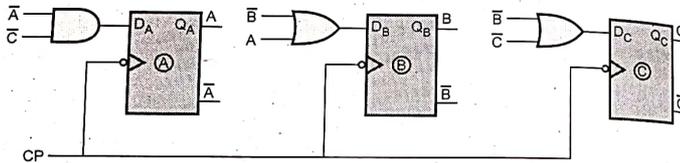


Fig. 5.9.51 (b)

Example 5.9.30 Design a counter with the following binary sequence : 0, 1, 3, 7, 6, 4 and repeat. Use T-flip flop. **GTU : Dec.-12, Marks 7**

Solution :

Step 1 : State diagram

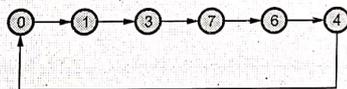


Fig. 5.9.52 (a)

Step 2 : Truth table

Present state			Next state			Flip-Flop inputs		
Q _A	Q _B	Q _C	Q _A [*]	Q _B [*]	Q _C [*]	T _A	T _B	T _C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	1	1	1	0	0

1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

Table 5.9.13

Step 3 : K-map simplification

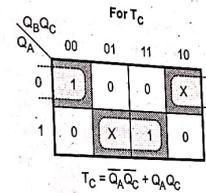
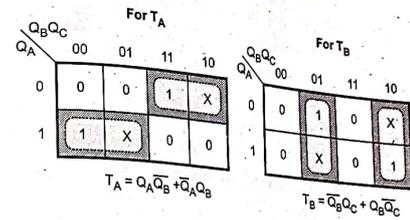


Fig. 5.9.52 (b)

Step 4 : Logic diagram

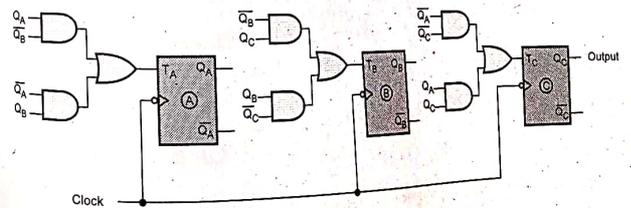
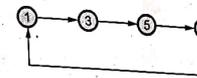


Fig. 5.9.52 (c)

Review Questions

1. Define counters.
2. State types of counters.
3. Compare synchronous and asynchronous counter.
4. What is MOD counter ?
5. Give comparison between synchronous and asynchronous counters.
6. Write a note on binary ripple counter. **GTU : Dec.-13, Marks 1**
7. Draw and explain 3-bit asynchronous up counter using flip-flops and explain with output waveforms. **GTU : May-14, Marks 7**
8. With logic diagram explain the operation of 4-bit binary ripple counter. How up counter can be converted into down counter ? **GTU : Dec.-13, Marks 7**
9. Draw 4-bit asynchronous counter. Also explain timing diagram for the same.
10. Design 3-bit up/down asynchronous counter.
11. What do you mean by decoding gates ?
12. Explain the problem of glitches in asynchronous counter circuits and solution for the same.
13. Explain using suitable waveforms : Problems faced by ripple counter.
14. Write a note on asynchronous counters.
15. What are decoding glitches and how these can be eliminated ?
16. Design mod-8 ripple counter using J-K flip-flop. Also draw its waveforms.
17. Design modulo-5 ripple counter using 3-bit ripple counter. Draw waveforms also.
18. What do you mean by ripple counter ?
19. Draw and explain 3-bit asynchronous up counter using flip-flops and explain with output waveforms.
20. Explain 4-bit up-down binary synchronous counter. **GTU : May-12, Marks 7**
21. Design 4-bit ripple counter using negative edge triggered JK flip flop. **GTU : Summer-15, Marks 7**
22. Draw a frequency divider using JK FFs to divide input clock frequency by a factor of 8. **GTU : Winter-15, Marks 3**
23. Design a 3-bit synchronous up counter using K-maps and positive edge-triggered JK FFs. **GTU : Winter-15, Marks 7**
24. Explain the steps in design of synchronous counter with the help of example.
25. Write a short note on up-down synchronous counter.
26. Design mod-8 ripple counter using J-K flip-flop. Also draw its waveforms.

27. Design modulo-5 ripple counter using 3-bit ripple counter. Draw waveforms also.
28. What is meant when we say that a counter is presettable ?
29. Describe the difference between asynchronous and synchronous presetting.
30. Write a note on skipping state counter.
31. What is lockout condition ?
32. What is a self starting counter ?
33. How to avoid lockout condition.



34. Design sequence generator using JK FFs. Avoid lockout condition.

5.10 Shift Register Counters

GTU : May-12

5.10.1 Ring Counter

- Fig. 4.9.1 shows the logic diagram for four-bit ring counter.

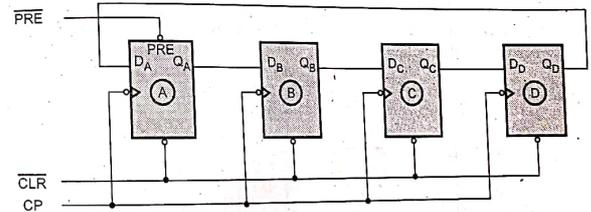


Fig. 5.10.1 Four-bit ring counter

- The Q output of each stage is connected to the D input of the next stage and the output of last stage is fed back to the input of first stage.
- The $\overline{\text{CLR}}$ followed by $\overline{\text{PRE}}$ makes the output of first stage to '1' and remaining outputs are zero, i.e. Q_A is one and Q_B, Q_C, Q_D are zero.
- The first clock pulse produces $Q_B = 1$ and remaining outputs are zero.
- According to the clock pulses applied at the clock input CP, a sequence of four states is produced. These states are listed in Table 5.10.1.

- 1 is always retained in the counter and simply shifted 'around the ring', advancing one stage for each clock pulse. In this case four stages of flip-flops are used. So a sequence of four states is produced and repeated.

Clock pulse	Q _A	Q _B	Q _C	Q _D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Table 5.10.1 Ring counter sequence 4-bits

- Fig. 5.10.1 gives the timing sequence for a four-bit ring counter.
- The ring counter can be used for counting the number of pulses.
- The number of pulses counted is read by noting which flip-flop is in state 1.
- No decoding circuitry is required.
- Since there is one pulse at the output for each of the N clock pulses, this circuit is also referred to as a divide-by-N-counter or an N : 1 scalar.
- Ring counters can be instructed for any desired MOD number, that is MOD-N ring counter requires N flip-flops.

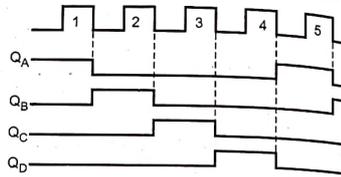


Fig. 5.10.2 Timing sequence for a four-bit ring counter

5.10.2 Johnson or Twisting Ring or Switch Tail Counter

- In a Johnson counter, the Q output of each stage of flip-flop is connected to the D input of the next stage.

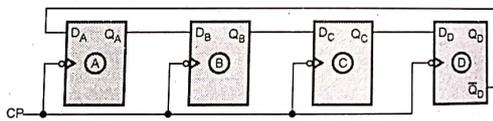


Fig. 5.10.3 Four-bit Johnson counter

- The single exception is that the complement output of the last flip-flop is connected back to the D-input of the first flip-flop as shown in Fig. 5.10.3.

Note Johnson counter can be implemented with SR or JK flip-flops as well.

- As shown in Fig. 5.10.3 there is a feedback from the rightmost flip-flop complement output to the leftmost flip-flop input. This arrangement produces a unique sequence of states.

- Initially, the register (all flip-flops) is cleared. So all the outputs, Q_A, Q_B, Q_C, Q_D are zero.
- The output of last stage, Q_D is zero. Therefore complement output of last stage, \bar{Q}_D is one. This is connected back to the D input of first stage. So D_A is one.
- The first falling clock edge produces Q_A = 1 and Q_B = 0, Q_C = 0, Q_D = 0 since D_B, D_C, D_D are zero.
- The next clock pulse produces Q_A = 1, Q_B = 1, Q_C = 0, Q_D = 0.
- The sequence of states is summarized in Table 5.10.2.

Clock pulse	Q _A	Q _B	Q _C	Q _D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table 5.10.2 Four-bit Johnson sequence

- The sequence of states is summarized in Table 5.10.2.

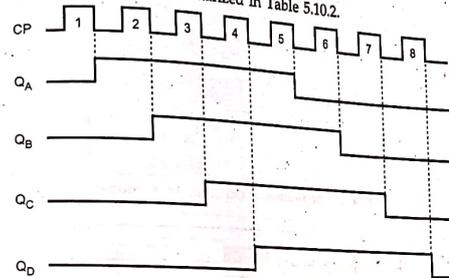


Fig. 5.10.4 Timing sequence for a four-bit Johnson counter

- After 8 states the same sequence is repeated.
- In this case, four-bit register is used. So the four-bit sequence has a total of eight states.

Clock pulse	Q _A	Q _B	Q _C	Q _D	Q _E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Table 5.10.3 Five-bit Johnson sequence

- Fig. 5.10.4 gives the timing sequence for a four-bit Johnson counter.
- If we design a counter of five-bit sequence, it has a total of ten states, as shown in Table 5.10.3.
- An n-stage Johnson counter will produce a modulus of 2 × n, where n is the number of stages (i.e. flip-flops) in the counter.

- Johnson counter requires only half the number of flip-flops compared to the standard ring counter. However, it requires more flip-flop than binary counter.
- As shown in tables, the counter will 'fill up' with 1s from left to right and then it will 'fill up' with 0s again.
- Another advantage of this type of sequence is that it is readily decoded with two input AND gates.
- Table 5.10.4 gives the count sequence and required decoding.

Clock pulse	Q _A	Q _B	Q _C	Q _D	AND Gate required for output
0	0	0	0	0	Q _A Q _D
1	1	0	0	0	Q _A Q _B
2	1	1	0	0	Q _B Q _C
3	1	1	1	0	Q _C Q _D
4	1	1	1	1	Q _A Q _D
5	0	1	1	1	Q _A Q _B
6	0	0	1	1	Q _B Q _C
7	0	0	0	1	Q _C Q _D

Table 5.10.4 Count sequence and required decoding

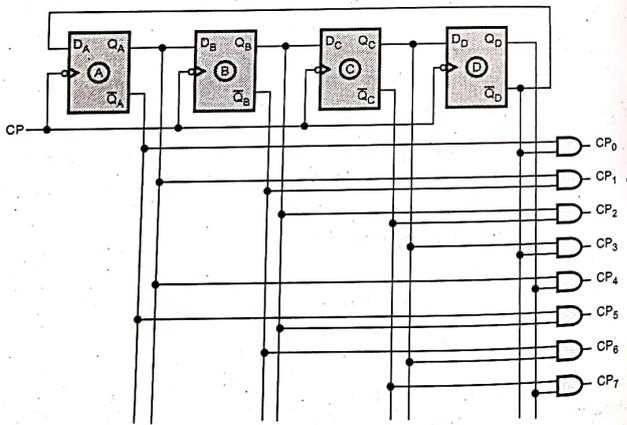


Fig. 5.10.5 Johnson counter with decoder

Review Questions

1. Draw and explain the working of 4-bit ring counter.
2. Describe the operation of shift register as ring counter.
3. Explain ring counter with design having initial state '01011', from initial state explain all possible states in that ring.
4. Explain ring counter design for the initial condition '10110' also explain twisted ring counter in brief.
5. Explain Johnson counters.
6. What is the difference between ring counter and Johnson's counter? GTU - May-12, Marks 7
7. Draw the neat circuit diagram of 3-bit Johnson's counter. Draw the relevant output waveforms.
8. Explain the use of shift register as twisted ring counter with diagrams.

5.11 Sequence Generator

GTU - Summer-18, Winter-18

5.11.1 Sequence Generator using Counters

- A sequential circuit which generates a prescribed sequence of bits, in synchronism with a clock, is referred to as a sequence generator. Fig. 5.11.1 shows the basic structure of a sequence generator using counters.

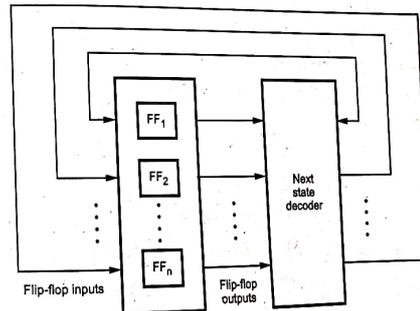


Fig. 5.11.1 Basic structure of a sequence generator

- For the design of sequence generator, we must determine the required number of flip-flops and the logic circuit for next state decoder.

Number of flip-flops required

- Number of flip-flops required to generate particular sequence can be determined as follows :

- Find the number of 1s in the sequence.
- Find the number of 0s in the sequence.
- Take the maximum out of two.
- If N is the required number of flip-flops, choose minimum value of n to satisfy equation given below.
 $\max(0s, 1s) \leq 2^n - 1$

Examples with Solutions

Example 5.11.1 Find the number of flip-flops required to generate the sequence 1101011.

Solution : The given sequence number of 0s are 2 and number of 1s are 5. Therefore equation becomes,

$$\therefore \max(2, 5) \leq 2^n - 1$$

$$\therefore 5 \leq 2^n - 1$$

$$\therefore n = 4$$

- Once the number of flip-flops are decided, we have to assign unique states corresponding to each bit in the given sequence such that flip-flop representing least significant bit generates the given sequence. (Usually, the output of the flip-flop representing least significant bit is used to generate the given sequence).

Example 5.11.2 Find the state assignments for sequence 1101011.

Solution : We have already seen that this sequence requires four flip-flops. Assuming the output of D flip-flop as a desired sequence state assignments are shown in Table 5.11.1.

A	B	C	D	States
0	0	0	1	1
0	0	1	1	3
0	0	0	0	0
0	1	0	1	5
0	0	1	0	2
0	1	1	1	7
1	0	0	1	9

Table 5.11.1

Example 5.11.3 Referring Table 5.11.1, draw state diagram and implement the sequence generator.

Solution :

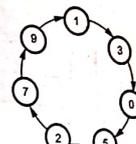


Fig. 5.11.2 State diagram

Present state				Next state				Flip-flop inputs							
Q _A	Q _B	Q _C	Q _D	Q _{A+1}	Q _{B+1}	Q _{C+1}	Q _{D+1}	J _A	K _A	J _B	K _B	J _C	K _C	J _D	K _D
0	0	0	0	0	1	0	1	0	X	1	X	0	X	1	X
0	0	0	1	0	0	1	1	0	X	0	X	1	X	X	0
0	0	1	0	0	1	1	1	0	X	1	X	X	0	1	X
0	0	1	1	0	0	0	0	0	X	0	X	X	1	X	1
0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
0	1	0	1	0	0	1	0	0	X	X	1	1	X	X	1
0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
0	1	1	1	1	0	0	1	1	X	X	1	X	1	X	0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	0	1	0	0	0	1	X	1	0	X	0	X	X	0
1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

Table 5.11.2

K-map simplification

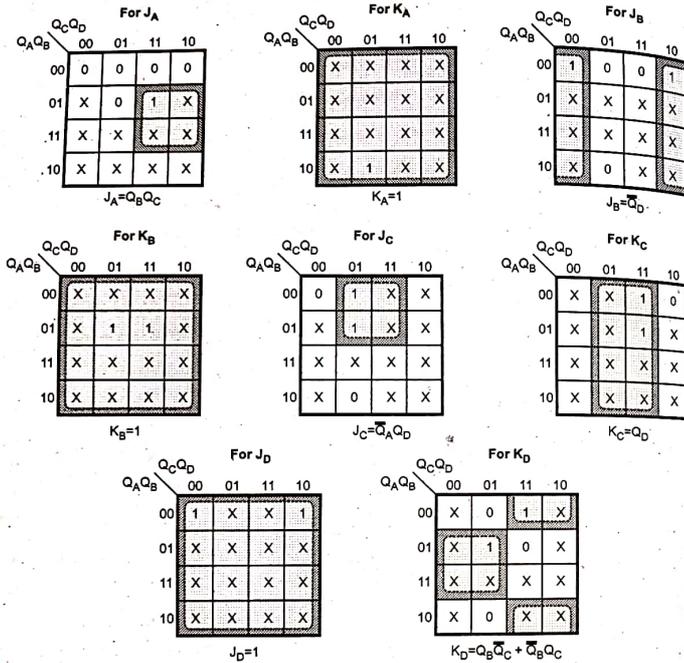


Fig. 5.11.3

Logic diagram

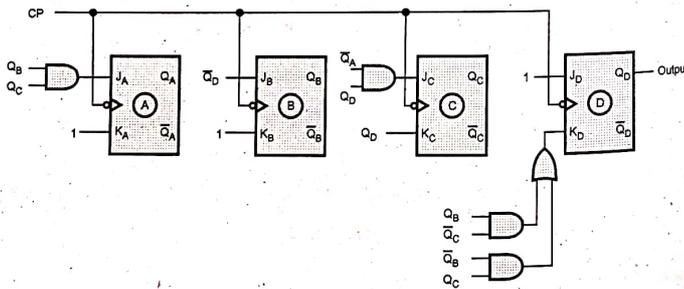


Fig. 5.11.4

Example 5.11.4 Design synchronous counter using D flip-flop for the sequence as shown in the Fig. 5.11.5.

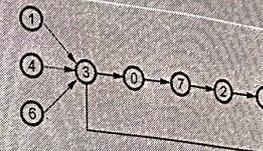


Fig. 5.11.5

Solution : Flip-flop excitation table is as shown below.

Present state			Next state		
A	B	C	A _{n+1}	B _{n+1}	C _{n+1}
0	0	0	1	1	1
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	0

Table 5.11.3

K-map simplification

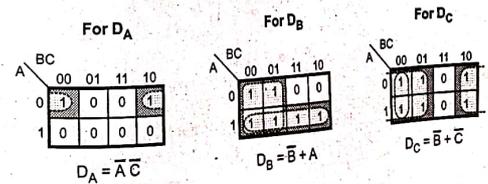


Fig. 5.11.6

Logic diagram

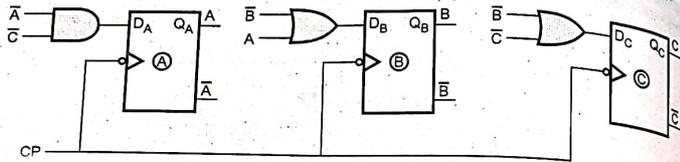


Fig. 5.11.7

Example 5.11.5 Using J-K flip-flops, design a synchronous counter that has the following sequence :
 0 → 2 → 5 → 6 → 0
 undesired states 1, 3, 4, 7 must always go to 0 on the next clock pulse.

Solution : Excitation table

Present state			Next state			Flip-flop inputs					
A	B	C	A ₊₁	B ₊₁	C ₊₁	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	0	0	0	0	X	0	X	X	1
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

Table 5.11.4

K-map simplification

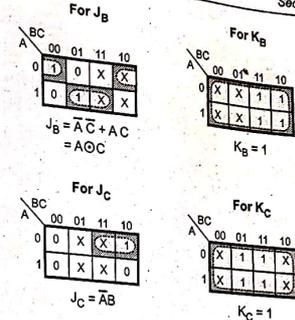
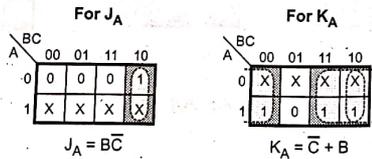


Fig. 5.11.8

Logic diagram

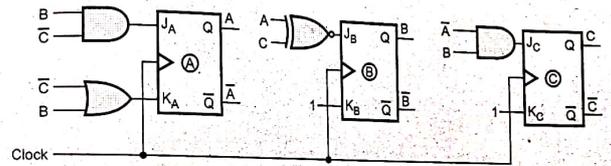


Fig. 5.11.9

Example 5.11.6 Design and implement 4-bit binary counter (using D flip-flops) which counts all possible odd numbers only.

Solution : The state diagram for given problem is as shown in the Fig. 5.11.10.

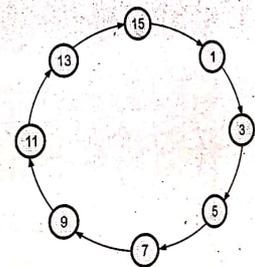


Fig. 5.11.10 State diagram

Excitation table

Present state				Next state			
Q _A	Q _B	Q _C	Q _D	Q _{A+}	Q _{B+}	Q _{C+}	Q _{D+}
0	0	0	0	X	X	X	X
0	0	0	1	0	0	1	1
0	0	1	0	X	X	X	X
0	0	1	1	0	1	0	1
0	1	0	0	X	X	X	X
0	1	0	1	0	1	1	1
0	1	1	0	X	X	X	X
0	1	1	1	1	0	0	1
1	0	0	0	X	X	X	X
1	0	0	1	1	0	1	1
1	0	1	0	X	X	X	X
1	0	1	1	1	1	0	1
1	1	0	0	X	X	X	X
1	1	0	1	1	1	1	1
1	1	1	0	X	X	X	X
1	1	1	1	0	0	0	1

K-map simplification

For D_A

00	X	0	0	X
01	X	0	1	X
11	X	1	0	X
10	X	1	1	X

$D_A = Q_A \bar{Q}_C + Q_A \bar{Q}_B + \bar{Q}_A Q_B Q_C$

For D_B

00	X	0	1	X
01	X	1	0	X
11	X	1	0	X
10	X	0	1	X

$D_B = Q_B \bar{Q}_C + \bar{Q}_B Q_C$

For D_C

00	X	1	0	X
01	X	1	0	X
11	X	1	0	X
10	X	1	0	X

$D_C = \bar{Q}_C$

For D_D

00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

$D_D = 1$

Fig. 5.11.11

Logic diagram

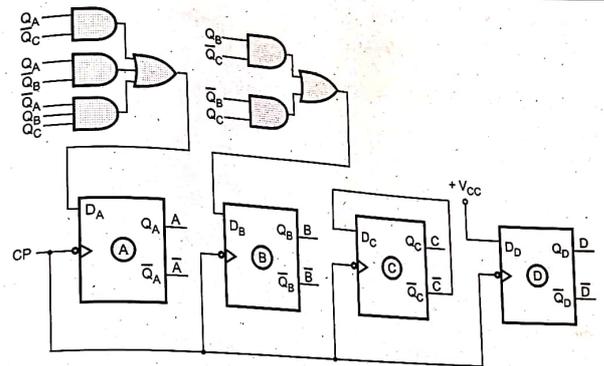


Fig. 5.11.12

Example 5.11.7 Design a pulse-train generator to generate a pulse train 110011..... using 'D' flip-flop.

Solution : The minimum number of flip-flops can be given as $N \leq 2^n - 1$.

Here $N = 6$, therefore $n = 3$. Table 5.11.5 shows state encoding for given sequence using 3 flip-flops.

CP	FF O/Ps			States
	Q _A	Q _B	Q _C	
1	1	1	1	7
2	1	1	0	6
3	0	0	1	1
4	0	0	0	0
5	1	0	0	4
6	1	0	1	5

Table 5.11.5

Therefore, design a circuit to get above state. In case of D flip-flop, flip-flop inputs are same as next states.

Excitation table

Present state			Next state/Flip-flop inputs		
Q _A	Q _B	Q _C	Q _A	Q _B	Q _C
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	x	x	x
0	1	1	x	x	x
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	1	1

K-map simplification

For D_A

	Q _B Q _C	00	01	11	10
Q _A	0	1	0	X	X
	1	1	1	0	0

$D_A = Q_A \bar{Q}_B + \bar{Q}_B \bar{Q}_C$

For D_B

	Q _B Q _C	00	01	11	10
Q _A	0	0	0	X	X
	1	0	1	1	0

$D_B = Q_A Q_C$

For D_C

	Q _B Q _C	00	01	11	10
Q _A	0	0	0	X	X
	1	1	1	1	1

$D_C = Q_A$

The required sequence is generated at the output of flip-flop A.

Logic diagram

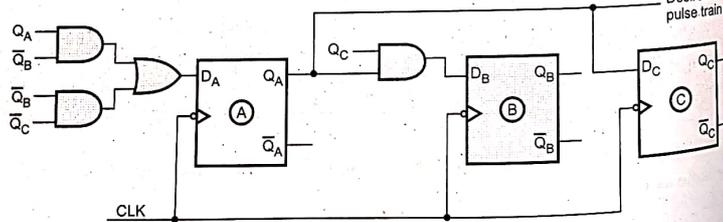


Fig. 5.11.13

Example 5.11.8 Design a non-sequential counter using J-K flip-flop, as per following state diagram.

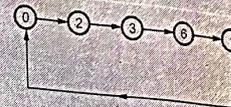


Fig. 5.11.14

Solution : Excitation table

Present state			Next state			Flip-flop inputs					
Q _A	Q _B	Q _C	Q _A	Q _B	Q _C	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	1	0	0	x	1	x	0	x
0	0	1	0	0	0	0	x	0	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	1	0	1	x	x	0	x	1
1	0	0	x	x	x	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	0	0	1	x	1	x	1	1	x
1	1	1	x	x	x	x	x	x	x	x	x

K-map simplification

For J_A

	Q _B Q _C	00	01	11	10
Q _A	0	0	0	1	0
	1	X	X	X	X

$J_A = Q_B Q_C$

For K_A

	Q _B Q _C	00	01	11	10
Q _A	0	X	X	X	X
	1	X	X	X	1

$K_A = 1$

For J_B

	Q _B Q _C	00	01	11	10
Q _A	0	1	0	X	X
	1	X	X	X	X

$J_B = \bar{Q}_C$

For K_B

	Q _B Q _C	00	01	11	10
Q _A	0	X	X	0	0
	1	X	X	X	1

$K_B = Q_A$

For J_C

	Q _B Q _C	00	01	11	10
Q _A	0	0	X	X	1
	1	X	X	X	1

$J_C = Q_B$

For K_C

	Q _B Q _C	00	01	11	10
Q _A	0	X	1	1	X
	1	X	X	X	X

$K_C = 1$

Logic diagram

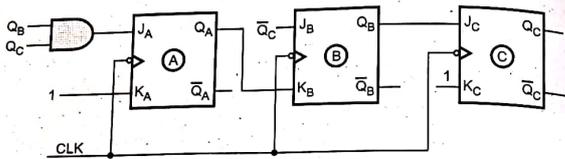


Fig. 5.11.14 (a)

Example 5.11.9 Design the circuit to generate the sequence :

0 → 2 → 5 → 4 → 7 → 3.

Solution : Excitation table

Present state			Next state			Flip-flop inputs					
Q _A	Q _B	Q _C	Q _{A+1}	Q _{B+1}	Q _{C+1}	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	1	1	1	X	0	1	X	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	0	1	1	X	1	X	0	X	0

K-map simplification

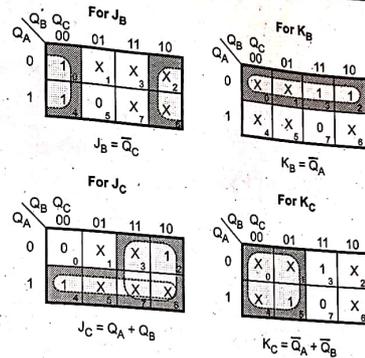
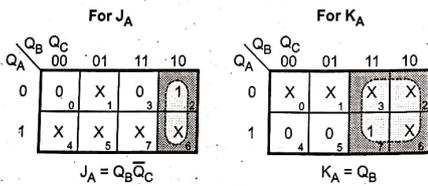


Fig. 5.11.15 (a)

Logic diagram

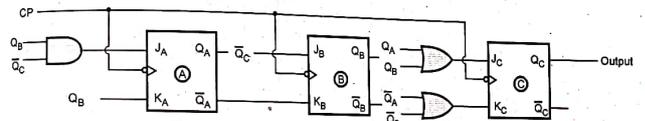


Fig. 5.11.15 (b)

Example 5.11.10 Design sequence generator to generate sequence 1-9-2-7-3-6 using JK flip-flop.

0 → 2 → 5 → 4 → 7 → 3.

Solution : Excitation table

Present state			Next state			Flip-flop inputs									
Q _A	Q _B	Q _C	Q _D	Q _{A+1}	Q _{B+1}	Q _{C+1}	Q _{D+1}	J _A	K _A	J _B	K _B	J _C	K _C	J _D	K _D
0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
0	0	0	1	1	0	0	1	1	X	0	X	0	X	X	0
0	0	1	0	0	1	1	1	0	X	1	X	X	0	1	X
0	0	1	1	0	1	1	1	0	X	1	X	X	0	1	X

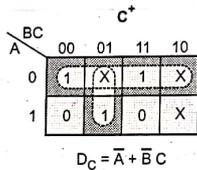
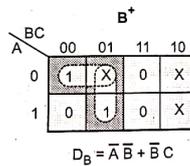
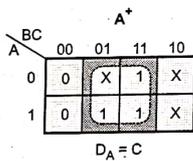
Example 5.11.11 Design a counter to generate the repetitive sequence 0, 3, 5, 7, 4 using DFF's. GTU : Summer-18 Marks 7

Solution : Step 1 : Determine the number of flip-flops needed we know that $2^n \geq N$. Here, $N = 7 \therefore n = 3$ i.e. 3 flip-flops needed.

Step 2 : Determine the excitable table for counter

Present State			Next State		
A	B	C	A ⁺	B ⁺	C ⁺
0	0	0	0	1	1
0	0	1	x	x	x
0	1	0	x	x	x
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	x	x	x
1	1	1	1	0	0

Step 3 : K-map simplification.



Step 4 : Draw logic diagram

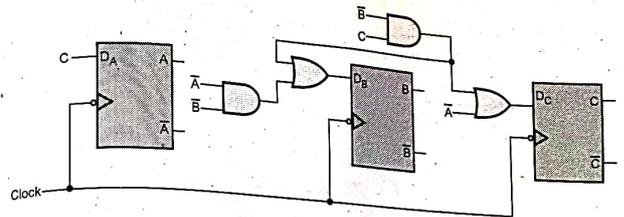


Fig. 5.11.17

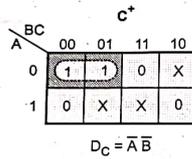
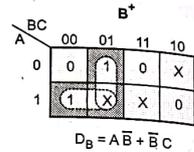
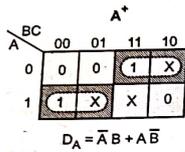
Example 5.11.12 Design a counter a for following binary sequence 0-1-3-4-6-0. GTU : Winter-18 Marks 7

Solution : Step 1 : Determine the number of flip-flops needed we know that $2^n \geq N$. Here $N = 6 \therefore n = 3$ i.e. 3 flip-flops needed.

Step 2 : Determine the excitation table for counter

Present State			Next state		
A	B	C	A ⁺	B ⁺	C ⁺
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	X	X	X
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	X	X	X
1	1	0	0	0	0
1	1	1	X	X	X

Step 3 : K-map simplification



Logic Diagram

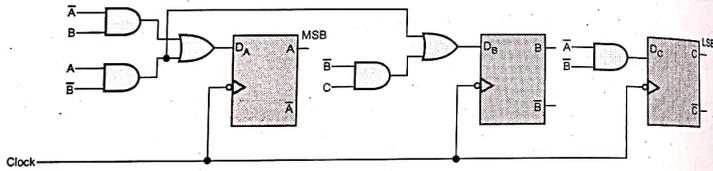


Fig. 5.11.18

5.11.2 Sequence Generator using Shift Register

- The simplest way of designing sequence generator using shift register is to take shift register of n-bits where n is equal to the length of sequence. Then load the bit sequence in the shift register by parallel load operation and apply the clock signal. The Fig. 5.11.19 illustrates the operation of such a sequence generator. Here, the sequence to be generated is 11001.
- Another design approach is used for sequence generator to reduce the required number of flip-flop stages in the shift register. In this approach a shift register with a next state decoder and preset logic is used. The Fig. 5.11.20 shows the block diagram of this approach. Here, the output of the next state decoder is a function of Q_A, Q_B, \dots, Q_n and it is used to determine the D_{in} input for the shift right

register. Initially, start button is pressed to activate parallel load operation. This loads initial value in the shift register. Then at each clock pulse shift register contents are shifted right by 1 bit position. The next state decoder circuit decodes Q_A generates the desired sequence.

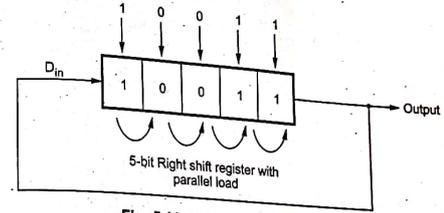


Fig. 5.11.19 (a) Sequence generator

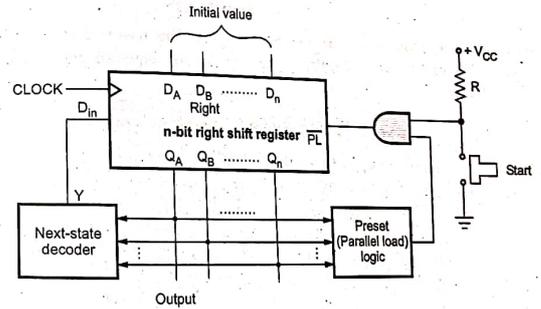


Fig. 5.11.19 (b) Sequence generator using shift register

After completion of one complete sequence, the register is again loaded with initial value to start the next train of sequence.

Examples with Solutions

Example 5.11.13 Design a sequence generator to generate the sequence 1101011 by shift register method.

Solution : In this approach, the minimum number of flip-flops n, required to generate a sequence of length N is given by

$$N \leq 2^n - 1$$

- In this example, $N = 7$, therefore, the minimum value of n , which may generate this sequence is 3. However, it is not guaranteed to lead to a solution. Let us try with 3 flip-flops. The Table 5.11.6 shows sequence generation with three flip-flops.

CP	Flip-flop outputs			D_{in}	States
	Q_A	Q_B	Q_C		
1	1	0	0	1	4
2	1	1	0	0	6
3	0	1	1	1	3
4	1	0	1	0	5
5	0	1	0	1	2
6	1	0	1	-	5
-	-	-	-	-	-

State is repeated →

Table 5.11.6

- As shown in the Table 5.11.7, the state 6 is repeated. This means that $n = 3$ is not sufficient. Let us try with 4 flip-flops. The table shows sequence generation with four flip-flops.

CP	Flip-flop outputs				D_{in}	Preset	States
	Q_A	Q_B	Q_C	Q_D			
Initial value	1	0	0	0	1	1	8
1	1	1	0	0	0	1	12
2	0	1	1	0	1	1	6
3	1	0	1	1	0	1	11
4	0	1	0	1	1	1	5
5	1	0	1	0	1	1	10
6	1	1	0	1	1	1	13
Preset flip-flop	1	1	1	0	X	0	14
1	1	0	0	0	1	1	8

Table 5.11.7

- As shown in the Table 5.11.7, states are not repeated. After completion of one complete sequence register is preset to value 1000 to start the next train of sequence. Fig. 5.11.20 (b) shows the logic diagram.

K-map simplification for D_{in}

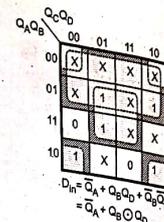


Fig. 5.11.20 (a)

Logic diagram

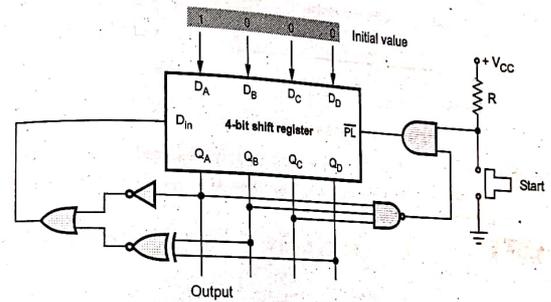


Fig. 5.11.20 (b)

Example 5.11.14 Design and implement the following sequence generator using shift register

... 1010 ...

Solution : Here the sequence is 10 and it is repeated. Thus the length of the sequence $N = 2$. Let the number of flip-flops required n be.

$$N \leq 2^n - 1$$

$$2 \leq 2^n - 1$$

$$n = 2$$

CP	Flip-flop outputs		D_{in}	States
	Q_A	Q_B		
1	1	0	0	2
2	0	1	1	1
1	1	0	0	2

K-map simplification for D_{in}

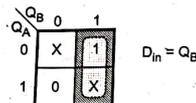


Fig. 5.11.21 (a)

Logic diagram

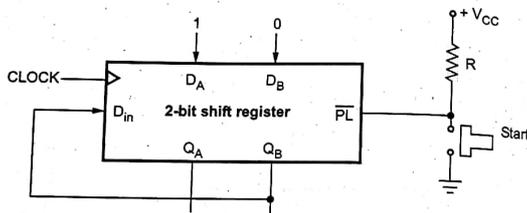


Fig. 5.11.21 (b)

In the above circuit preset/parallel load logic is only required to load the initial value. After completion of one sequence, the shift register have the same initial value and hence it is not required to reload again.

Example 5.11.15 Design a pulse train generator using shift register for the following pulse train.1 1 1 0 1 0

Solution : The minimum number of flip-flops n can be given as

$$N \leq 2^n - 1$$

Here $N = 6$, therefore $n = 3$. The Table 5.11.8 shows sequence generation with three flip-flops.

CP	Flip-flop outputs			D_{in}	Preset	States
	Q_A	Q_B	Q_C			
1	1	0	0	1	1	4
2	1	1	0	1	1	6
3	1	1	1	0	1	7
4	0	1	1	1	1	5
5	1	0	1	0	1	5

Preset flip-flop

	Q_B	Q_C	Q_A	Q_C	Q_B	Q_A	Q_C
6	0	1	0	0	1	2	
7	0	0	1	X	0	1	
1	1	0	0	0	1	1	

Table 5.11.8

K-map simplification for D_{in}

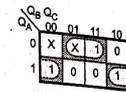


Fig. 5.11.22 (a)

$$D_{in} = \bar{Q}_A Q_C + Q_A \bar{Q}_C = Q_A \oplus Q_C$$

Logic diagram

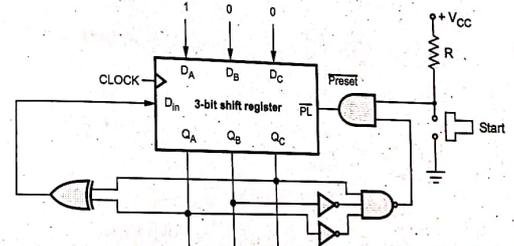


Fig. 5.11.22 (b)

Example 5.11.16 Design a pulse train generator circuit using shift register for the following pulse train.1 0 0 0 1 1 0.....

Solution : The minimum number of flip-flops n , required to generate sequence of length N is given by

$$N \leq 2^n - 1$$

Here, $N = 7$, therefore $n = 3$. The Table 5.11.9 (a) shows sequence generation with three flip-flops.

CP	Flip-flop outputs			D _{in}	States
	Q _A	Q _B	Q _C		
1	1	1	1	0	7
2	0	1	1	0	3
3	0	0	1	0	1
4	0	0	0	1	0
5	1	0	0	1	4
6	1	1	0	0	6
7	0	1	1	-	3

Table 5.11.9 (a)

As seventh state is repeated, n = 3 is not sufficient. Let us try with 4 flip-flops. The Table 5.11.9 (b) shows sequence generation with four flip-flops.

CP	Flip-flop outputs				D _{in}	Preset	States
	Q _A	Q _B	Q _C	Q _D			
1	1	1	1	1	0	1	15
2	0	1	1	1	0	1	7
3	0	0	1	1	0	1	3
4	0	0	0	1	1	1	1
5	1	0	0	1	1	1	9
6	1	1	0	0	0	1	12
7	0	1	1	0	1	1	6
Preset flip-flop	1	0	1	1	X	0	11
1	1	1	1	1	0	1	15

Table 5.11.9 (b)

K-map simplification for D_{in}

		Q _C Q _D			
		00	01	11	10
Q _A Q _B	00	X	1	0	X
	01	X	X	0	1
	11	0	X	0	X
	10	X	1	X	X

Fig. 5.11.23 (a)

$$D_{in} = \bar{Q}_A \bar{Q}_C + Q_A \bar{Q}_B + Q_C \bar{Q}_D$$

Logic diagram

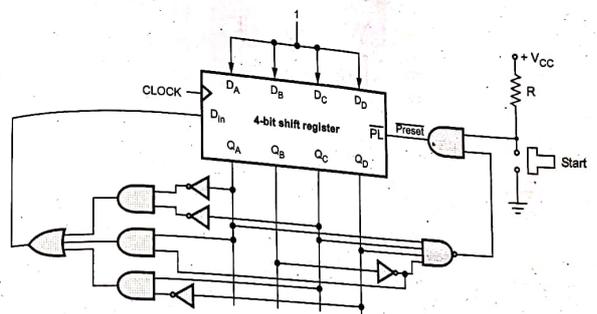


Fig. 5.11.23 (b)

Example 5.11.17 Design sequence generator using shift register to generate sequence 1101.

Solution : The minimum number of flip-flops n can be given as

$$N \leq 2^n - 1$$

Here N = 4, therefore n = 3. The Table 5.11.10 shows sequence generation with three flip-flops.

CP	Flip-flop inputs			D _{in}	PL	States
	Q _A	Q _B	Q _C			
1	1	0	0	1	1	4
2	1	1	0	0	1	6
3	0	1	1	1	1	3
4	1	0	1	0	1	5
5	0	1	0	X	0	2
Preset flip-flop	1	0	0	1	1	4

Table 5.11.10

K-map simplification for D_{in}

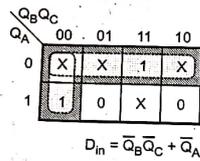


Fig. 5.11.24 (a)

Logic diagram

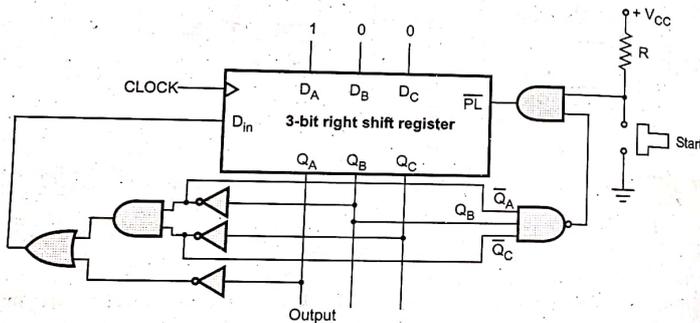


Fig. 5.11.24 (b)

5.12 Special Counter ICs

5.12.1 IC 7490 (Decade Binary Counter)

- IC 7490 is a decade binary counter. It consists of four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide by five.
 - Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.
1. **BCD Decade (8421) Counter** : The B input must be externally connected to the Q_A output and A input receives the incoming count and a BCD count sequence is produced.

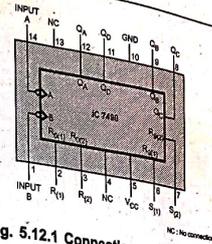


Fig. 5.12.1 Connection diagram for 7490

2. **Symmetrical Bi-quinary Divide-by-Ten Counter** : The Q_D output must be externally connected to the A input. The input count is then applied to the B input and a divide-by-ten square wave is obtained at output Q_A .
 3. **Divide-by-Two and Divide-by-Five Counter** : No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (A as the input and Q_A as the output). The B input is used to obtain binary divide-by-five operation at the Q_D output.
- Table 5.12.1 shows function tables and Fig. 5.12.2 shows logic diagram for IC7490. (See Fig. 5.12.2 on next page)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table 5.12.1 (a) BCD count sequences (Note 1)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

Table 5.12.1 (b) BCD Bi-quinary (5-2) (Note 2) sequences (Note 1)

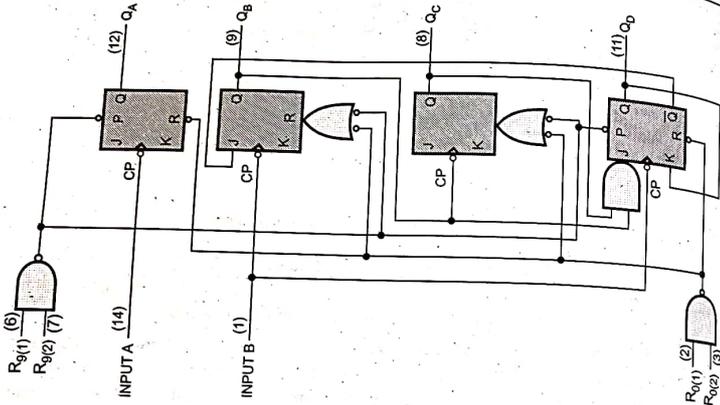


Fig. 5.12.2

Note 1 : Output Q_A is connected to input B for BCD count.

Note 2 : Output Q_D is connected to input A for bi-quinary count.

Example 5.12.1 Design a divide-by-96 counter using 7490 ICs.

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide by 100 counter. To get a divide-by-96 counter, the counter is reset as soon as it becomes 1001 0110. The diagram is shown in Fig. 5.12.3.

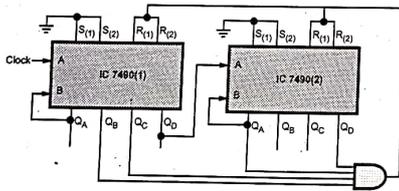


Fig. 5.12.3 Divide-by-96 counter

Example 5.12.2 Design MOD-78 counter using IC 7490.

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-78 or MOD-78 counter, the counter is reset as soon as it becomes 0111 1000 as shown in Fig. 5.12.4.

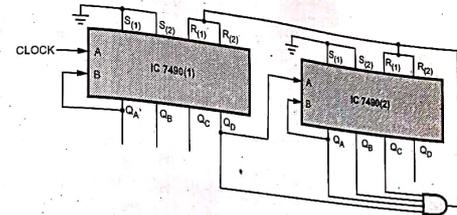


Fig. 5.12.4

Example 5.12.3 Design Mod 8 counter using 7490.

Solution : MOD 8 ripple counter using 7490 :

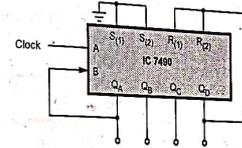


Fig. 5.12.5

Example 5.12.4 In 7490, if Q_D output is connected to A input and pulses at B input. Find count sequence and waveform of output Q_A .

Solution : If the Q_D output is connected to A input of 7490 IC and, input clock is applied to B input divide by ten square wave is obtained at output Q_A .

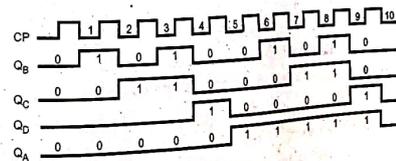


Fig. 5.12.6 Waveforms

Clock	Outputs			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Table 5.12.2

Example 5.12.5 Design a mod 25 counter using IC 7490.

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-25 counter, the counter is reset as soon as it becomes 0010 0101. The diagram is shown in Fig. 5.12.7.

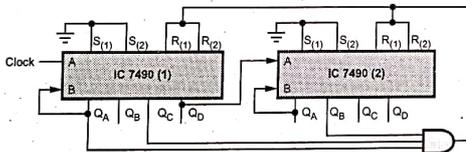


Fig. 5.12.7

5.12.2 IC 7493 (4-bit Ripple Counter)

- The 7493 is a high speed 4-bit ripple type counters partitioned into two sections. The counter has a divide-by-two section and divide-by-eight (7493) section which are triggered by a HIGH to LOW transition on the clock inputs. Each section can be used separately or tied together to form divide-by-sixteen counters.
- The 7493 is 4-bit binary counter. It consists of four master slave flip-flops which are internally connected to provide a divide-by-two section. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

Connection Diagram of 7493

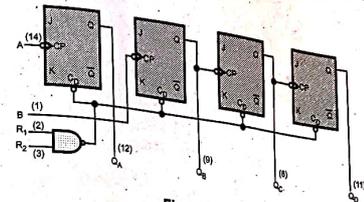


Fig. 5.12.8 (a)

Modes of 7493

1. 4-Bit Ripple Counter : The output Q_A must be externally connected to input B. The input count pulses are applied to the input A. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C and Q_D outputs as shown in the truth table.

Logic Diagram

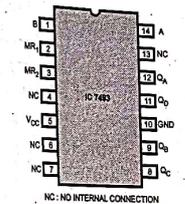


Fig. 5.12.8 (b)

2. 3-Bit Ripple Counter : The input count pulses are applied to input A. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_B, Q_C and Q_D outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple through counter.

- Table 5.12.3 shows the truth tables for 7493.

Count	Output			
	Q _A	Q _B	Q _C	Q _D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

Table 5.12.3 Truth table

Note Output Q_A is connected to input B.

Example 5.12.6 Design a divide-by-128 counter using 7493 ICs.

Solution : Since $128 = 16 \times 8$, a divide-by-16 counter followed by a divide-by-8 counter will become a divide-by-128 counter. IC 7493 is a 4-bit binary counter (i.e. mod-16 or divide-by-16), therefore, two IC packages will be required.

- The circuit diagram is as shown in the Fig. 5.12.9.

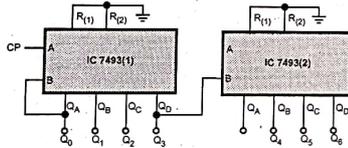


Fig. 5.12.9 Divide-by-128 counter

Example 5.12.7 Design divide-by-6 counter using IC 7493.

Solution : The Fig. 5.12.10 shows divide-by-6 (MOD 6) counter using 7493. As shown in the Fig. 5.12.10, the clock is applied to input B of IC 7493 and the output count sequence is taken from Q_D , Q_C and Q_B . As soon as count is 110, i.e. Q_D and $Q_C = 1$, the internal NAND gate output goes low and it resets the counter.

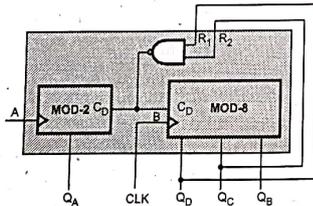


Fig. 5.12.10 Divide-by-6 counter using 7493

5.12.3 IC 74192/74193 (Up/Down - BCD/Binary Counters)

- The 74192 is an UP/DOWN BCD decade counter and the 74193 is an UP/DOWN modulo-16 binary counter. Separate count up and count down clocks are used and in either counting mode the circuits operate synchronously. The outputs change state in a synchronous manner with the inputs.
- Separate terminal count up and terminal count down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

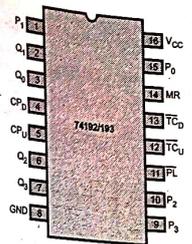


Fig. 5.12.11

Features :

- Low Power ... 95 mW Typical Dissipation
- High Speed ... 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High Speed Termination Effects
- Fig. 5.12.11 shows the pin diagram for 74192 and 74193.

PIN NAMES

- CP_U : Count Up Clock Pulse Input
- CP_D : Count Down Clock Pulse Input
- MR : Asynchronous Master Reset (Clear) Input
- \overline{PL} : Asynchronous Parallel Load (Active LOW) Input
- P_n : Parallel Data Inputs
- Q_n : Flip-Flop Outputs

\overline{TC}_D : Terminal Count Down (Borrow) Output
 \overline{TC}_U : Terminal Count Up (Carry) Output

State Equations for 74192 :

$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

State Equations for 74193 :

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

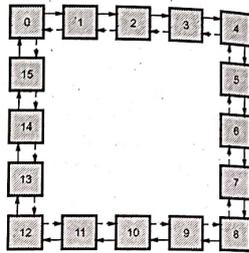
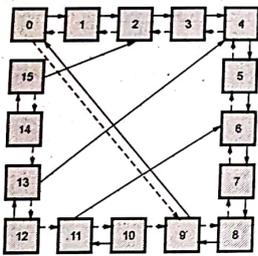


Fig. 5.12.12 (a) State diagram for 74192

Fig. 5.12.12 (b) State diagram for 74193

Functional Description

- The LS192 and LS193 are asynchronously presettable decade and 4-bit binary synchronous UP/DOWN (reversible) counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master-slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.
- Each flip-flop contains feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common count up line and a common count down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the count up input will advance the count by one; a similar transition on the count down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the

circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

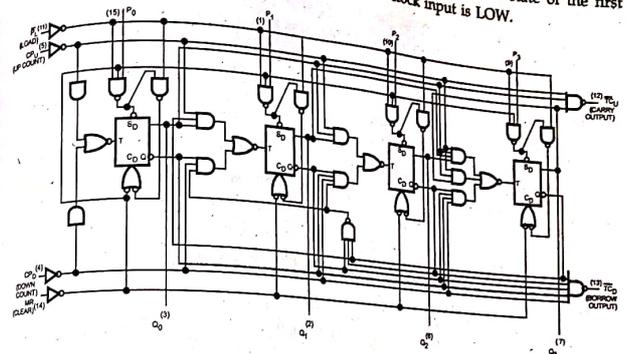


Fig. 5.12.13 Logic diagram for 74192

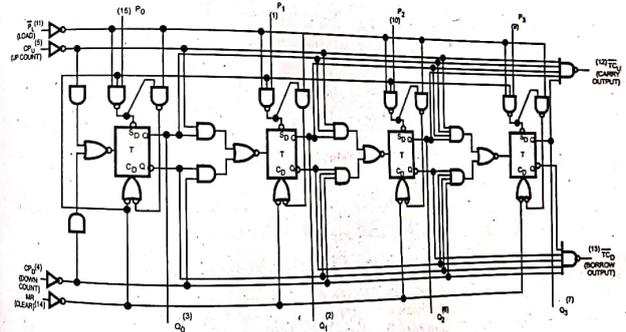


Fig. 5.12.14 Logic diagram for 74193

- The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the count up clock will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, thus

effectively repeating the count up clock, but delayed by two gate delays. Similarly, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the count down clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

- Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (\overline{PL}) and the Master Reset (\overline{MR}) inputs are LOW, information present on the parallel data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the master reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

MR	\overline{PL}	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No change
L	H	\uparrow	H	Count up
L	H	H	\uparrow	Count down

Table 5.12.4 Mode select table

L : Low voltage level
 H : High voltage level
 X : Don't care

Example 5.12.8 Design a divide-by-7 DOWN counter using 74192 IC. Make use of the borrow output.

Solution : For the DOWN counter, the clock pulses are applied at CP_D input. When the output becomes 0, the counter is loaded with preset inputs 0111 and the states will be : 0111, 0110, 0101, 0100, 0011, 0010, and 0001. The circuit is shown in Fig. 5.12.15.

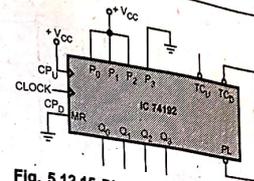


Fig. 5.12.15 Divide-by-7 down counter

Example 5.12.9 Design a mod-12 Up counter using 74193 IC.

Solution : This can be done in two ways :

1. Connect the circuit shown in Fig. 5.12.15. The Q_2 and Q_3 outputs are ANDed and are connected to clear input (with $PL = 1$). As soon as count becomes 1100, the counter is cleared.
2. Connect the circuit shown in Fig. 5.12.16. The Q_2 and Q_3 outputs are NANDed and are connected to load input (with $MR = 1, P_0 = P_1 = P_2 = P_3 = 0$). As soon as the count reaches 1100, the counter is loaded with P inputs.

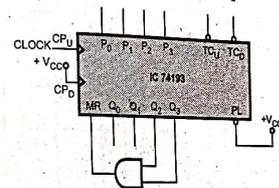


Fig. 5.12.16 Mod-12 up counter

Example 5.12.10 Draw the timing diagram for IC74193 showing all signals.

Solution : Fig. 5.12.17 shows the timing diagram for 74193.

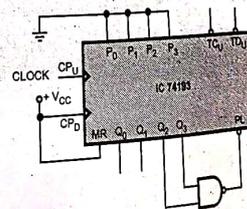


Fig. 5.12.17 Mod-12 up counter

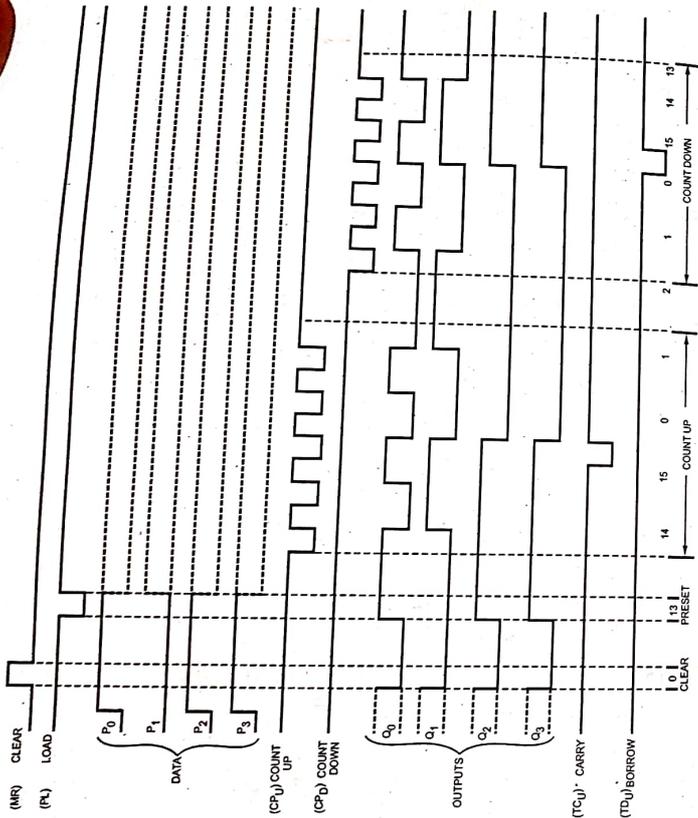


Fig. 5.12.18 Timing diagram

Note A : Clear overrides load, data, and count inputs.
 Note B : When counting up, countdown input must be HIGH; when counting down, countup input must be HIGH.

Oral Questions and Answers

Q.1 Define a sequential logic circuit. Give an example.
Ans. : The circuits in which the output variables depend not only on the present input but they also depend upon the past history of these input variables are known as sequential logic circuits. Flip-flops, counters, registers are the examples of sequential logic circuit.

Q.2 What are synchronous sequential circuits?
Ans. : Synchronous sequential circuits are those in which signals can affect the memory elements only at discrete instants of time. Clocked flip-flops are examples of synchronous sequential circuits.

Q.3 Differentiate between flip-flop and latch.
Ans. :

Sr. No.	Latch	Flip-flop
1.	A simple latch is the basis for flip-flop building.	Flip-flop is built by connecting some additional components around a latch.
2.	Latch is level triggered either positive level or negative level triggered.	Flip-flop is pulse or clock-edge triggered either positive edge or negative edge triggered.
3.	The latch output responds to inputs, until active level is maintained at the enable input.	Flip-flop output responds to inputs only at the specified (positive or negative) edges of clock pulse.

Q.4 Give the meaning for edge triggering in flip-flops.
Ans. : In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock pulse at the clock input. There are two types of edge triggering.

- **Positive edge triggering :** Here, the output responds to the changes in the input only at the positive edge of the clock pulse at the clock input.
- **Negative edge triggering :** Here, the output responds to the changes in the input only at the negative edge of the clock pulse at the clock input.

Q.5 What is the operation of D flip-flop?
Ans. : In D flip-flop during the occurrence of clock pulse if D = 1, the output Q is set and if D = 0, the output is reset.

Q.6 What is the operation of JK flip-flop?
Ans. :

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change.

- When both the inputs K and J are high the output toggle on the next positive clock edge.

Q.7 What is the operation of T flip-flop ?

Ans. : T flip-flop is also known as Toggle flip-flop.

- When T = 0 there is no change in the output.
- When T = 1 the output switch to the complement state (i.e.) the output toggles.

Q.8 What is a master-slave flip-flop ?

Ans. : A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave. The output of the master flip-flop is fed as an input to the slave flip-flop. The master flip-flop is triggered at the positive edge of the clock and slave flip-flop is triggered at the negative edge of the clock.

Q.9 Give the characteristic equation and state diagram of JK flip-flop.

Ans. :

• Characteristic equation : $Q_n + 1 = J \bar{Q}_n + K Q_n$

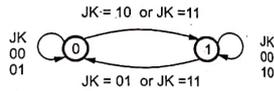


Fig. 5.1

Q.10 What is the minimum number of flip-flops needed to design a counter of modulus 60 ?

Ans. : $2^n \geq 60 \therefore n = 6$

Q.11 What is the minimum number of flip-flops required to implement a modulo 21 synchronous counter ?

Ans. : $2^n \geq 21 \therefore n = 5$

Q.12 What is meant by programmable counter ? Mention its application.

Ans. : A counter that divides an input frequency by a number which can be programmed, is called programmable counter.

Applications of programmable counter

1. Frequency division
2. Digital clock
3. Stop watch
4. Programmable logic controllers.

Q.13 Name two sequential switching circuits.

Ans. : Counter, shift register.

Q.14 Define synchronous counter.

Ans. : When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called synchronous counter.

Q.15 Define asynchronous counter.

Ans. : The counter in which the output of the current Flip-Flop drives the clock input of the next higher-order Flip-Flop is called asynchronous counter.

Q.16 Draw the state diagram of MOD-10 counter.

Ans. :

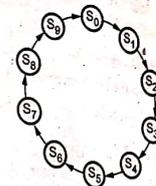


Fig. 5.2

Q.17 Define registers.

Ans. : A register is a group of flip-flops. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

Q.18 Define shift registers.

Ans. : The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

Q.19 What are the different types of shift type ? or Classify the registers with respect to serial and parallel input output.

Ans. : There are five types. They are,

- Serial In Serial Out Shift Register
- Serial In Parallel Out Shift Register
- Parallel In Serial Out Shift Register
- Parallel In Parallel Out Shift Register
- Bidirectional Shift Register

Q.20 What is the difference between serial and parallel transfer ? What type of register is used in each case ?

Ans. : When data is transferred one bit at a time, the process of transfer is known as serial transfer. When multiple bits of data are transferred at a time, the process is known as parallel transfer. For parallel transfer, we can use parallel in and parallel out register. For serial transfer we can use left shift or right shift register.

Q.21 If a serial-in-serial-out shift register has N stages and if the clock frequency is f, what will be time delay between input and output ?

Ans. : The time delay between input and output is $T_D = \frac{N}{f}$.

Q.22 Define universal shift register.

Ans. : The register which has both shifts (right-shift and left-shift) and parallel load capabilities is referred to as universal shift register.

Q.23 Mention applications of shift registers.

Ans. : 1. Delay line 2. Serial to parallel converter 3. Parallel to serial converter
4. Pseudo-random binary sequence generator 5. Sequence detector.

Q.24 What is shift register counter ?

Ans. : A shift register can also be used as a counter. A shift register with the serial output connected back to the serial input is called shift register counter.

□□□

6

A / D and D / A Converters

Contents

6.1	Introduction	
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6.7	Performance Parameters (Specifications of ADC) Winter-17, 18, Summer-18 · Marks 7
6.8	Types of A/D Converters Winter-16, Summer-15, 16, 18, Marks 7
6.9	A/D Converter using V/F Converter	
6.10	A/D Converter using V/T Conversion	
6.11	Example of A/D Converter IC	

6.1 Introduction

- Most of the information carrying signals such as voltage, current, charge, temperature, pressure and time are available in the analog form.
- However, for processing, transmission and storage purposes, it is often more convenient to express such signals in the digital form. When expressed in the digital form, they provide better accuracy and reduce noise.
- The development in the microprocessor technology has made it compulsory to process data in the digital form. Since digital systems such as microprocessor use a binary system of ones and zeros, we have to convert signal from analog form to digital form.
- The circuit that performs this conversion is called an analog to digital (A/D) converter.
- On the other hand, a digital to analog (D/A) converter is used when a binary output from a digital system must be converted to some equivalent analog voltage or current.
- For example, if in a particular system a computer is used as a controller, the controlling signal produced by the computer is always digital. The system to be controlled requires the analog signal. Hence in between the computer and the system to be controlled the digital to analog converter is must.
- Fig. 6.1.1 shows a typical A/D and D/A converter application. As shown in the Fig. 6.1.1, the analog signal is converted in digital form, which is then processed or perhaps just transmitted or recorded. Once processed, received or retrieved the signal is D-A converted to be reused in analog form.

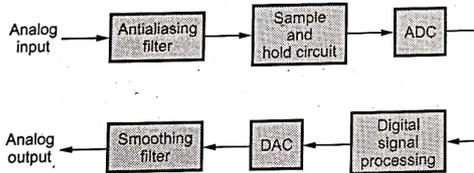


Fig. 6.1.1 Typical A/D and D/A converter application

Review Question

1. What is difference between A/D and D/A converters ?

6.2 D/A Converters

- A DAC (Digital to Analog Converter) accepts an n-bit input word $b_1, b_2, b_3, \dots, b_n$ in binary and produce an analog signal proportional to it.
- Fig. 6.2.1 (a) shows circuit symbol and input-output characteristics of a 4-bit DAC. There are four digital inputs, indicating 4-bit DAC. Each digital input requires an electrical signal representing either a logic 1 or a logic 0. The b_n is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB.
- Fig. 6.2.1 (b) shows analog output voltage V_o is plotted against all 16 possible digital input words.

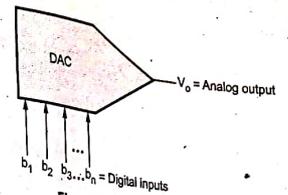


Fig. 6.2.1 (a) DAC circuit symbol

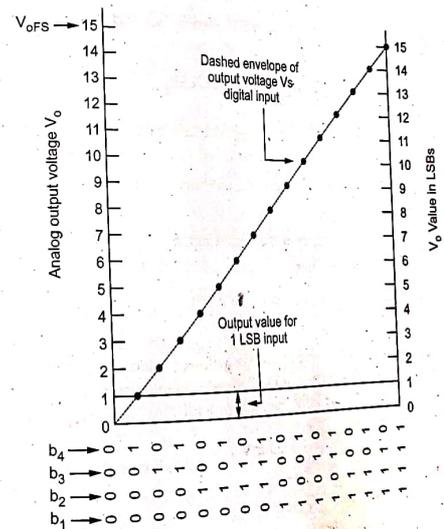


Fig. 6.2.1 (b)

6.2.1 Performance Parameters (Specifications) of DAC

Resolution

- Resolution is defined in two ways.
- Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC.

$$\text{Resolution} = 2^n \quad \dots (6.2.1)$$
- Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} \quad \dots (6.2.2)$$

where, V_{OFS} = Full scale output voltage

- From equation (6.2.1), we can say that, the resolution can be determined by the number of bits in the input binary word. For an 8-bit DAC resolution can be given as

$$\text{resolution} = 2^n = 2^8 = 256$$

- If the full scale output voltage is 10.2 V then by second definition the resolution for an 8-bit DAC can be given as

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{10.2}{2^8 - 1} = \frac{10.2}{255} = 40 \text{ mV/LSB}$$

Therefore, we can say that an input change of 1 LSB causes the output to change by 40 mV.

- From the resolution, we can obtain the input-output equation for a DAC.

$$\text{Thus } V_o = \text{Resolution} \times D$$

where, D = Decimal value of the digital input

and V_o = Output voltage

- The resolution takes care of changes in the input.

Accuracy

- It is a comparison of actual output voltage with expected output. It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst, $\pm \frac{1}{2}$ of its LSB. If the full scale output voltage is 10.2 V then for an 8-bit DAC accuracy can be given as

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n - 1) 2} = \frac{10.2}{255 \times 2} = 20 \text{ mV} \quad \dots (6.2.3)$$

Settling Time (Conversion Time)

- The operating conversion speed of a DAC is usually specified by giving its settling time. The settling time is the time required for the DAC output to 90 form zero to full scale as the binary input is changed from all 0s to all 1s.

- Actually, the settling time is measured as the time for the DAC output to settle within $\pm 1/2$ step size (1/2 LSB) of its final value.
- Typical values for settling time range from 50 ns to 10 μ s. It depends on word length, circuit technology and architecture.
- Generally, DAC's with a current output will have shorter settling times than those with voltage outputs.

Dynamic Range

- The dynamic range of DAC is defined as the ratio of the largest output to the smallest output, excluding zero. It is expressed in dB. For linear DACs it is given by,

$$\text{Dynamic range} = 20 \log 2^n \approx 6n.$$

- For companding type DAC, the dynamic range is more. It is typically 66 to 72 dB.

Offset Error

- The offset error is defined as the nonzero level of the output voltage when all inputs are zero.

- It adds a constant value to all output values, as shown in Fig. 6.2.2.

- It is due to the presence of offset voltage in op-amp and leakage currents in the current switches.

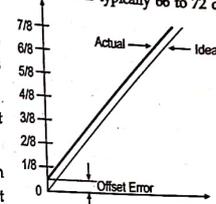


Fig. 6.2.2 Offset error in transfer characteristics of DAC

Gain Error

- The gain error is defined as the difference between the calculated gain of the current to voltage converter and the actual gain achieved. It is due to the errors in the feedback resistor on the current to voltage converter op-amp.

- Fig. 6.2.3 shows the gain error in transfer characteristics of DAC.

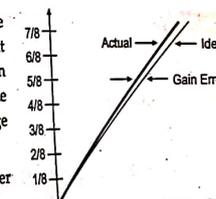


Fig. 6.2.3 Gain error in transfer characteristics of DAC

Non-Linearity (Linearity Error)

- An ideal DAC should be linear. For an ideal DAC, the output voltage would be a linear function of the input code. But it is fact that all DAC departs somewhat from the ideal linearity. The typical factors responsible for introducing non-linearity are :

- Non-exact value of resistors, and
- Non-ideal electronic switches that introduce extra resistance to the circuit.
- The non-linearity error is the amount by which the actual output differs from the ideal straight-line output. The different types of non-linearity are :
 - Integral non-linearity,
 - Differential non-linearity.

Stability

- The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

Example 6.2.1 An 8-bit DAC has an output voltage range of 0 - 2.55 V. Define its resolution in two ways.

Solution : For the given DAC,

$$n = \text{Number of bits} = 8$$

i) Resolution = $2^n = 2^8 = 256$

i.e. the output voltage can have 256 different values including zero.

ii) V_{oFS} = Full scale output voltage = 2.55 V

$$\therefore \text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{2.55}{2^8 - 1} = \frac{10 \text{ mV}}{1 \text{ LSB}}$$

Thus an input change of 1 LSB causes the output to change by 10 mV.

Example 6.2.2 An 8-bit D/A converter has resolution of 10 mV/bit. Find the analog output voltage for the following digital inputs :

- i) 10001010 ii) 00010000

Solution : i) 10001010

$$D = \text{Equivalent of } (10001010)_2 = 138$$

$$V_o = \text{Resolution} \times D = 10 \times 10^{-3} \times 138 = 1.38 \text{ V}$$

ii) 00010000

$$D = \text{Equivalent of } (00010000)_2 = 16$$

$$V_o = \text{Resolution} \times D = 10 \times 10^{-3} \times 16 = 0.16 \text{ V}$$

Example 6.2.3 An 8-bit DAC has resolution of 20 mV/LSB. Find V_{oFS} and V_o if the input is $(10000000)_2$.

Solution : Resolution = $\frac{V_{oFS}}{2^n - 1} \therefore 20 = \frac{V_{oFS}}{2^8 - 1}$

$$V_{oFS} = 5.1 \text{ V}$$

$$D = \text{Equivalent of } (10000000)_2 = 128$$

$$V_o = \text{Resolution} \times D = 20 \times 10^{-3} \times 128 = 2.56 \text{ V}$$

Example 6.2.4 Find out step size and analog output for 4-bit R/2R ladder DAC when input is $(1000)_2$ and $(1111)_2$. Assume $V_{ref} = +5 \text{ V}$.

Solution : For given DAC, $n = 4, V_{oFS} = +5 \text{ V}$

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{5}{2^4 - 1} = \frac{1}{3} \text{ V/LSB}$$

$$V_o = \text{Resolution} \times D$$

For $D = \text{Decimal of } (1000)_2 = 8$

$$V_o = \frac{1}{3} \times 8 = 2.6667 \text{ V}$$

For $D = \text{Decimal of } (1111)_2 = 15$

$$V_o = \frac{1}{3} \times 15 = 5 \text{ V}$$

Example 6.2.5 A 12-bit DAC has a step size of 8 mV. Determine the full scale output voltage and percentage resolution. Also find the output voltage for the input of $(010101101101)_2$.

Solution : For 12-bit DAC, step size is 8 mV.

$$V_{oFS} = 8 \text{ mV} \times 2^{12} - 1 = 32.76 \text{ V}$$

$$\% \text{ Resolution} = \frac{8 \text{ mV}}{32.76 \text{ V}} \times 100 = 0.02442$$

$$\text{The output voltage for the input } (010101101101)_2 \text{ is } 8 \text{ mV} \times (1389)_{10} = 11.112 \text{ V}$$

6.2.2 Basic Conversion Techniques

- There are mainly two techniques used for digital to analog conversion :
 - Binary weighted resistor D/A converter
 - R/2R ladder D/A converter

- In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called current driven DACs.

6.2.2.1 Binary Weighted Resistor D/A Converter

- The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors $2R, 4R, 8R, \dots, 2^n R$, as shown in the Fig. 6.2.4.

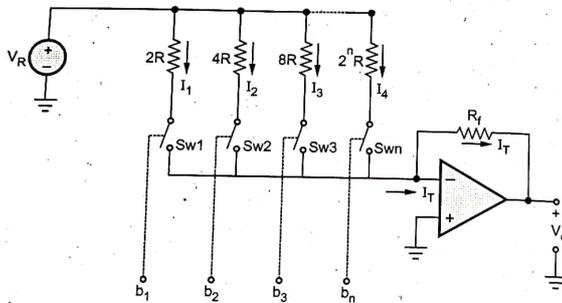


Fig. 6.2.4 Binary weighted resistor DAC

- As shown in the Fig. 6.2.4, switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage V_R ; otherwise it leaves resistor open. Therefore,

For ON-switch, $I = \frac{V_R}{R}$ and

For OFF-switch, $I = 0$

- The operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through R_f . Hence the total current through R_f can be given as

$$I_T = I_1 + I_2 + I_3 + \dots + I_n \quad \dots (6.2.4)$$

- The output voltage is the voltage across R_f and it is given as

$$V_o = -I_T R_f = -(I_1 + I_2 + I_3 + \dots + I_n) R_f \quad \dots (6.2.5)$$

$$= - \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right) R_f \quad \dots (6.2.6)$$

$$= - \frac{V_R}{R} R_f (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}) \quad \dots (6.2.7)$$

When $R_f = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}) \quad \dots (6.2.8)$$

- The equation (6.2.7) indicates that the analog output voltage is proportional to the input digital word.
- The simplicity of the binary weighted DAC is offset by drawbacks associated with it.

Drawbacks :

1. Wide range of resistor values are required. For 8-bit DAC, the resistors required are $2^1 R, 2^2 R, 2^3 R, \dots$ and $2^8 R$. Therefore, the largest resistor is 128 times the smallest one.
 2. This wide range of resistor values has restrictions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across such a large resistor due to the bias current also affects the accuracy. For smaller values of resistors, the loading effect may occur.
 3. The finite resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.
- All these drawbacks, especially the requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8-bits.

6.2.2.2 R/2R Ladder D/A Converter

Inverter R/2R Ladder (Current Steering Mode) D/A Converter

- R/2R ladder D/A converter uses only two resistor values. This avoids resistance spread drawback of binary weighted D/A converter.
- Fig. 6.2.5 shows R/2R ladder DAC. Like binary weighted resistor DAC, it also uses shunt resistors to generate n binary weighted currents; however it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC. Voltage scaling requires an additional set of voltage dropping series resistances between adjacent nodes, as shown in the Fig. 6.2.5.

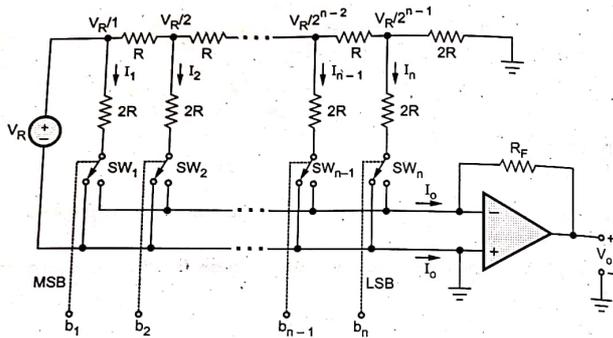


Fig. 6.2.5

- Here, each bit of the binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is at the virtual ground. Since both the positions of switches are at ground potential, the current flowing through resistances is constant and it is independent of switch position. These currents can be given as,

$$I_1 = \frac{V_R}{2R} \quad \dots (6.2.9)$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^{(n-1)}}{2R} = \frac{I_1}{2^{(n-1)}} \quad \dots (6.2.10)$$

- We know that, V_o is given as,

$$V_o = -I_T R_f \quad \dots (6.2.11)$$

$$\begin{aligned} V_o &= -R_f (I_1 + I_2 + I_3 + \dots + I_n) \\ &= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right) \\ &= \frac{-V_R R_f}{R} (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}) \quad \dots (6.2.12) \end{aligned}$$

- When $R_f = R$, V_o is given as,

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}) \quad \dots (6.2.13)$$
- Let us consider 4-bit binary DAC with binary input 1001 and $R_f = R$, as shown in the Fig. 6.2.6.

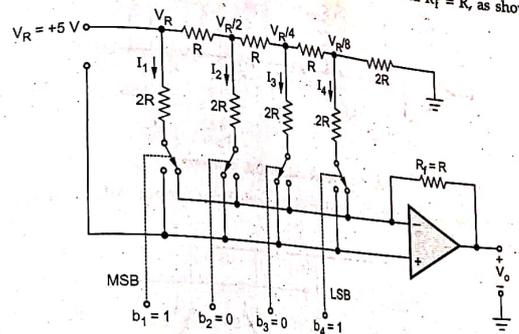


Fig. 6.2.6 Inverted 4-bit R/2R ladder DAC

- Here, output voltage is given as

$$\begin{aligned} V_o &= -V_R (1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}) \\ &= -V_R \left(\frac{1}{2} + 0 + 0 + \frac{1}{16} \right) = -0.5625 V_R = 2.8125 V \end{aligned}$$

- The inverting R/2R ladder DAC works on the principle of summing currents and it is also said to operate in the current steering mode.
- An important advantage of the current mode is that all ladder node voltages remain constant with changing input codes, thus avoiding any shutdown effects by stray capacitances.

R/2R Ladder (Voltage Switching Mode) D/A Converter

- In this type, reference voltage is applied to one of the switch positions, and other switch position is connected to ground, as shown in the Fig. 6.2.7.

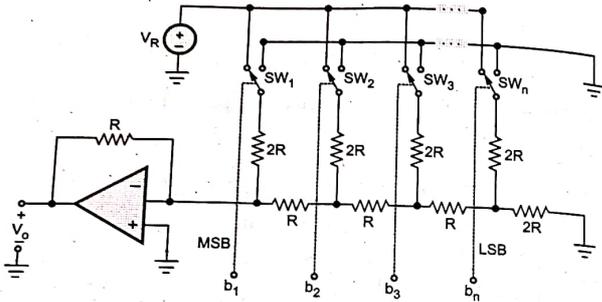


Fig. 6.2.7 R/2R ladder D/A converter

- Let us consider 3-bit R/2R ladder DAC with binary input 001, as shown in the Fig. 6.2.8.

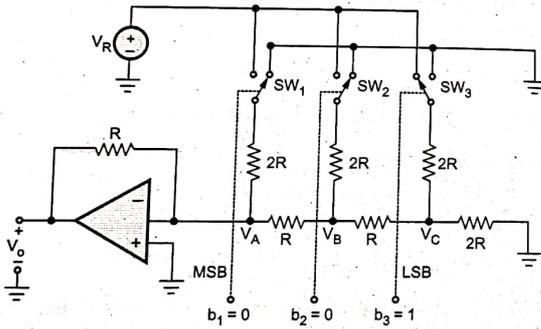


Fig. 6.2.8 3-bit R/2R ladder DAC

- Reducing above network to the left by Thevenin's theorem we get,

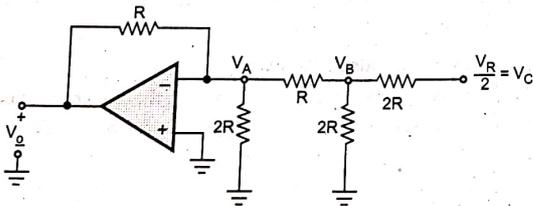


Fig. 6.2.9 (a)

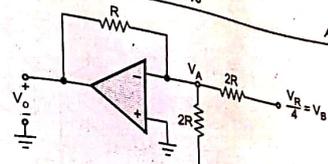


Fig. 6.2.9 (b)

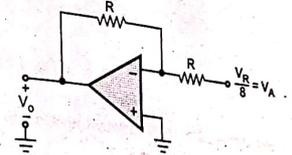


Fig. 6.2.9 (c)

- Therefore, the output voltage is $V_R/8$ which is equivalent to binary input 001.
- For binary input 100 the network can be reduced as follows :

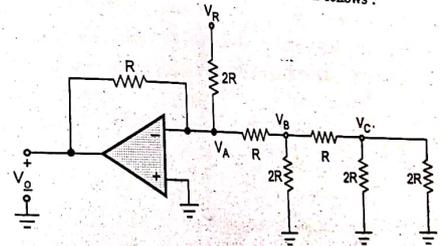


Fig. 6.2.10 (a)

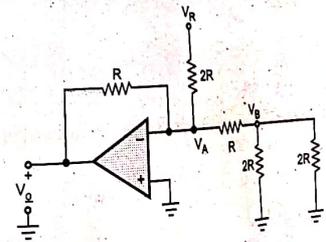


Fig. 6.2.10 (b)

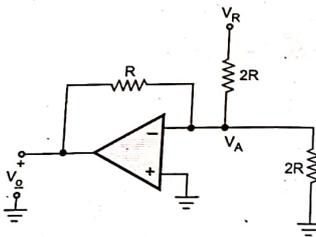


Fig. 6.2.10 (c)

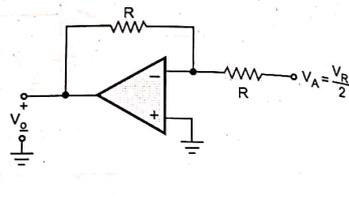


Fig. 6.2.10 (d)

Therefore, the output voltage is $V_R/2$, which is equivalent to binary input 100.

- In general, the voltage is given by,

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

Advantages of R/2R ladder DACs

- Easier to build accurately as only two precision metal film resistors are required.
- Number of bits can be expanded by adding more sections of same R/2R values.
- In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

Expression for output voltage

- The expression for V_o can be obtained as,

Let I_{out} = Output current

R_f = feedback resistance of op-amp

$$\therefore V_o = -I_{out} R_f$$

Now I_{out} = current resolution $\times D$

$$\therefore V_o = -(\text{current resolution} \times D) R_f$$

$$\therefore V_o = -(\text{current resolution} \times R_f) \times D \quad \dots (6.2.14)$$

- The coefficient of D is the voltage resolution and can be called simple resolution.

$$\therefore V_o = -\text{Resolution} \times D \quad \dots (6.2.15)$$

- In terms of actual circuit elements, output can be written as,

$$V_o = -\left(\frac{V_R}{R} \times \frac{1}{2^n} R_f\right) \times D \quad \dots (6.2.16)$$

Resolution

- The resolution of R/2R ladder type DAC with current output is,

$$\text{Resolution} = \frac{1}{2^n} \times \frac{V_R}{R} \quad \dots (6.2.17)$$

- while the resolution for R/2R ladder type DAC with voltage output is,

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f \quad \dots (6.2.18)$$

Example 6.2.6 Suggest the values of resistors and reference voltage if resolution required is 0.5 V for 4 bit R/2R ladder type DAC.

Solution : Resolution = $\left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f$

Let $V_R = 10 \text{ V}$, $n = 4$ and resolution = 0.5

$$\therefore 0.5 = \frac{1}{2^4} \times \frac{10}{R} \times R_f \quad \therefore \frac{R}{R_f} = 1.25$$

Choose $R_f = 10 \text{ k}\Omega$

$$\therefore R = 12.5 \text{ k}\Omega$$

Example 6.2.7 Calculate the output voltage and conversion resolution of 8-bit R-2R ladder DAC for the input data of 11011101 with reference voltage of 10 V.

Solution :

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{10}{2^8 - 1} = 0.0392$$

$$V_o = \text{Resolution} \times D$$

$$D = \text{Equivalent of } (11011101)_2 = (221)_{10}$$

$$\therefore V_o = 0.0392 \times 221 = 8.663$$

Example 6.2.8 A 5-bit R-2R ladder network with reference voltage of 10 V.

Find :

- Analog output due to LSB change
- Full scale output voltage
- Analog output for digital input 11001.

Solution : i) Analog output due to LSB change :

$$V_o = -V_R \left(\frac{1}{2^5}\right) = -10 \times \frac{1}{32} = -0.3125$$

ii) Full scale output voltage : $V_{oFS} = -9.6875 \text{ V}$

iii) Analog output for digital input 11001 :

$$(11001)_2 = 25$$

$$\therefore 25 \times -0.3125 = -7.8125 \text{ V}$$

Review Questions

1. What is D/A converter ? Explain any two types of D/A converters along with characteristic features.
2. Define the following terms for D/A converters : i) Resolution ii) Accuracy iii) Monotonicity iv) Conversion time.
3. Draw a 2-bit-D/A converter with R-2R resistors and explain its operation ? State its advantages ?
4. Explain the R/2R ladder techniques of D/A conversion.
5. Explain the binary weighted resistor technique of D/A conversion.
6. Explain the advantages of R/2R ladder technique over binary weighted resistor technique.
7. Draw the circuit diagram of voltage mode R-2R ladder DAC and explain its working.
8. List the various methods of D/A conversion, state the advantages and disadvantages of each.
9. State the specifications of DAC. Also explain the applications of DAC.
10. Explain the following with reference to DAC :
i) Linearity 2) Accuracy 3) Settling time.
11. List various specifications of DAC.

6.3 D/A Converter IC

- The 1408/DAC0808 is an 8-bit R/2R ladder type D/A converter compatible with TTL and CMOS logic. It is designed to use where the output current is linear product of an eight-bit digital word.
- Fig. 6.3.1 shows the pin diagram and block diagram for IC 1408/DAC0808.
- The IC 1408/DAC0808 consists of a reference current amplifier, an R/2R ladder and eight high speed current switches. It has eight

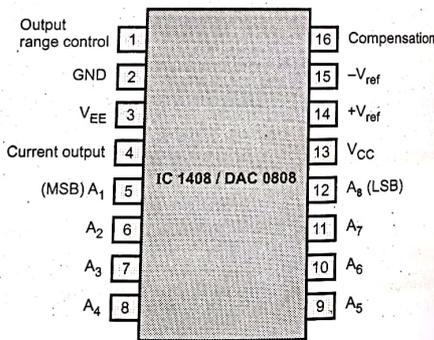


Fig. 6.3.1 (a) Pin diagram

input data lines A₁ (MSB) through A₈ (LSB) which control the positions of current switches.

- It requires 2 mA reference current for full scale input and two power supplies V_{CC} = +5 V and V_{EE} = -15 V (V_{EE} can range from -5 V to -15 V).

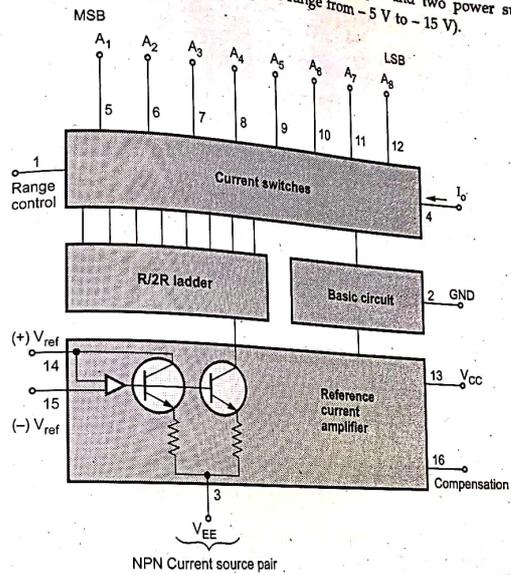


Fig. 6.3.1 (b) Block diagram

- The voltage V_{ref} and resistor R₁₄ determines the total reference current source and R₁₅ is generally equal to R₁₄ to match the input impedance of the reference current amplifier.
- Fig. 6.3.2 shows a typical circuit for IC 1408/DAC0808. The output current I_o can be given as,

$$I_o = \frac{V_{ref}}{R_{14}} \left(\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right) \dots(6.3.1)$$

Note Input A_1 through A_8 can be either 0 or 1. Therefore, for typical circuit full scale current can be given as,

$$I_o = \frac{5}{2.5\text{ K}} \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right) = \frac{2\text{ mA} \times 255}{256} = 1.992\text{ mA}$$

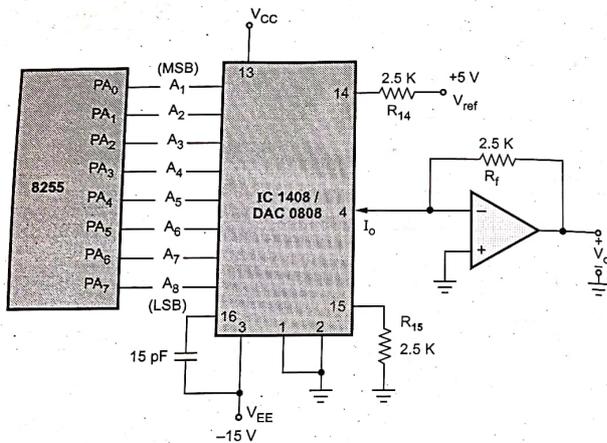


Fig. 6.3.2 Typical circuit for IC 1408/DAC0808

It shows that the full scale output current is always 1 LSB less than the reference current source of 2 mA. This output current is converted into voltage by I to V converter. The output voltage for full scale input can be given as,

$$V_o = 1.992 \times 2.5\text{ K} = 4.98\text{ V}$$

Note The arrow on the pin 4 shows the output current direction. It is inward. This means that IC 1408/DAC0808 sinks current. At $(0000\ 0000)_2$ binary input it sinks zero current and at $(1111\ 1111)_2$ binary input it sinks 1.992 mA.

- The circuit shown in the Fig. 6.3.3 gives output in the unipolar range. When digital input is 00H, the output voltage is 0 V and when digital input is FFH $(1111\ 1111)_2$, the output voltage is + 5 V. This circuit can be modified to give bipolar output.

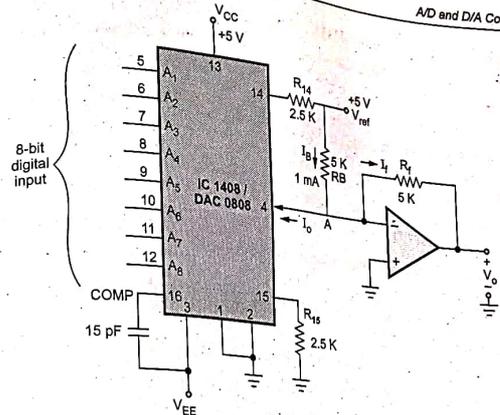


Fig. 6.3.3 Interfacing DAC in the bipolar range

- Fig. 6.3.3 shows the circuit for giving output in the bipolar range. Here, resistor R_B (5 K) is connected between V_{ref} and the output terminal of IC 1408/DAC0808. This gives a constant current source of 1 mA.

Operation

Condition 1 : For binary input 0000 0000 (00H)

When binary input is 00H, the output current I_o at pin 4 is zero. Due to this current flowing through R_B (1 mA) flows through R_f giving $V_o = -5\text{ V}$.

Condition 2 : For binary input 1000 0000 (80H).

When binary input is 80H, the output current I_o at pin 4 is 1 mA. By applying KCL at node A we get,

$$-I_B + I_o + I_f = 0$$

Substituting values of I_B and I_o we get,

$$-(1\text{ mA}) + (1\text{ mA}) + I_f = 0$$

$$I_f = 0$$

and therefore the output voltage is zero.

Condition 3 : For binary input 1111 1111 (FFH).

When binary input is FFH, the output current I_o at pin 4 is 2 mA. By applying KCL at node A we get,

$$-I_B + I_o + I_f = 0$$

Substituting values of I_B and I_o we get,

$$-(1 \text{ mA}) + (2 \text{ mA}) + I_f = 0$$

$$I_f = -1 \text{ mA}$$

Therefore, the output voltage is +5 V. In this way, circuit shown in the Fig. 6.3.2 gives output in the bipolar range.

Important electrical characteristics for IC 1408/DAC0808

- Reference current : 2 mA
- Supply voltage : +5 V V_{CC} and -15 V V_{EE}
- Setting time : 300 ns
- Full scale output current : 1.992 mA
- Accuracy : 0.19 %

Review Questions

1. Interface a typical 8 bit DAC with 8255.
2. Draw and explain the typical interfacing circuit for DAC 1408/0808.
3. Draw and explain the typical interfacing circuit for DAC 1408/0808 in the bipolar range.

6.4 Applications of DAC

- DACs are used with a Digital Signal Processor (DSP) to convert a single into analog for transmission in the mixer circuit.
- They are used in waveform generators.
- They are used in ADC converters.

Review Question

1. State the applications of DAC.

6.5 Sample and Hold Circuit

- The sample and hold (S/H) circuit samples the value of the input signal in response to a sampling command and hold it at the output until arrival of the next command.

- It samples an analog input voltage in a very short period, generally in the range of 1 to 10 μ s and holds the sampled voltage level for an extended period, which can range from a few millisecond to several seconds.
- The Fig. 6.5.1 shows input and output response of the sample and hold circuit.

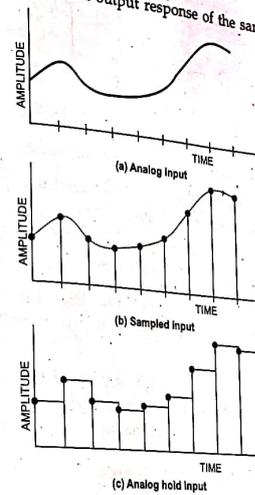


Fig. 6.5.1 Input and output response of sample and hold circuit

- The sample and hold circuit uses to basic components analog switch and capacitor.
- The Fig. 6.5.2 shows the basic sample and hold circuit.

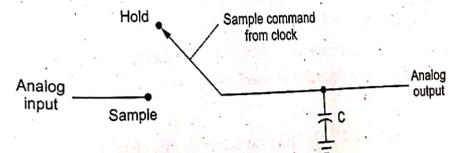


Fig. 6.5.2 Principle diagram for sample and hold circuit

- The circuit tracks the analog signal until the sample command causes the digital switch to isolate the capacitor from the signal and the capacitor holds this analog voltage during A/D conversion.

6.5.1 Basic Sample and Hold Circuit

- Fig. 6.5.3 shows the basic sample and hold circuit. Here, JFET is used as a switch.

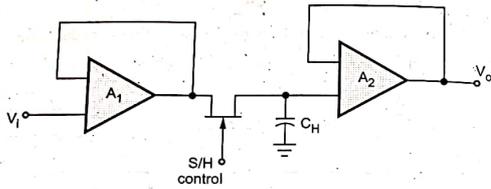


Fig. 6.5.3 Basic sample and hold circuits

- During the sampling time the JFET switch is turned on, and the holding capacitor charges up to the level of the analog input voltage.
- At the end of this short sampling period, the JFET switch is turned off. This isolates the holding capacitor C_H from the input signal.
- As a result, the voltage across capacitor C_H and hence the output voltage will remain essentially constant at the value of the input voltage at the end of the sampling time.
- However, there will be a small drop-off or drop of the capacitor voltage during the hold period due to the various leakage currents. To avoid this, input and output buffers (voltage follower) circuits are used.

6.5.2 Performance Parameters of S/H Circuits

- The S/H circuit performance can be characterised by specifications of the ordinary amplifier such as input offset voltage, gain error, nonlinearity etc.
- However, during the transitions from one mode to other (sample to hold or hold to sample), as well as in hold mode, circuit performance is characterised by specifications peculiar to S/H circuits.
- These specifications are explained below with the help of S/H circuit waveform shown in Fig. 6.5.4. (See Fig. 6.5.4 on next page)

1. Acquisition time (t_{ac})

- It is the time required for the holding capacitor C_H to charge up to a level close to the input voltage during sampling. It depends on three factors :
 - i) RC time constant
 - ii) Maximum output current of op-amp
 - iii) Slew rate of op-amp

2. Aperture time (t_{ap})

- Because of propagation delays through the driver and switch, V_o will keep tracking V_i some time after the inception of the hold command. This is the aperture time.
- To get the precise timing, it is necessary to advance hold command by this amount.

3. Aperture uncertainty (Δt_{ap})

- It is the variation in aperture time from sample to sample. Due to aperture uncertainty it is difficult to compensate aperture time by advancing hold command.

4. Hold mode settling time (t_s)

- After the application of hold command, it takes a certain amount of time for V_o to settle within a specified error band, such as 1 %, 0.1 % or 0.01 %. This is the hold mode settling time.

5. Hold step

- Because of the parasitic switch capacitances, at the time of switching between sample to hold mode, there is an unwanted transfer of charge between the switch driver and C_H .
- This changes the capacitor voltage and hence the output voltage, as shown in the Fig. 6.5.4.
- This changes in output voltage are referred to as hold step, pedestal error and sample to hold offset.

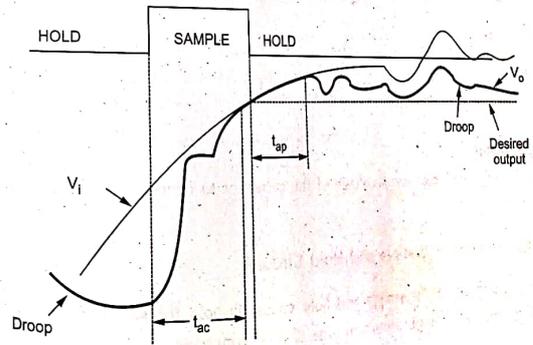


Fig. 6.5.4 S/H circuit waveforms

- The change in the output voltage can be related as given below,

$$\Delta V_o = \frac{\Delta Q}{C_H} \dots (6.5.1)$$

6. Feedthrough

- In the hold mode, because of stray capacitance across the switch, there is a small amount of ac coupling between V_o and V_i .
- This a.c. coupling causes output voltage to vary with variation in the input voltage.
- This is referred to as feedthrough and it is given as,

$$\Delta V_o \cong \frac{C_{ds}}{C_H} \Delta V_i \dots (6.5.2)$$

where C_{ds} is the stray capacitance between drain and source of JFET.

- Feedthrough is usually expressed in terms of the Feedthrough Rejection Ratio (FRR) and it is given as,

$$FRR = 20 \log_{10} \frac{\Delta V_i}{\Delta V_o} \dots (6.5.3)$$

Example 6.5.1 Calculate the change in the output voltage if input changes by 5 V with FRR for S/H circuit is 80 dB.

Solution : $FRR = 20 \log_{10} \frac{\Delta V_i}{\Delta V_o}$

$80 = 20 \log_{10} \frac{5}{\Delta V_o}$ i.e. $\Delta V_o = 0.5 \text{ mV}$

7. Voltage droop

- The leakage current causes voltage of the capacitor to drop down. This is referred to as droop.

6.5.3 Advantages of Sample and Hold Circuits

- The primary use of the sample and hold circuit to hold the sampled analog input voltage constant during conversion time of A/D converter.

- In case of multichannel ADCs, synchronization can be achieved by sampling signals from all channels at the same time.
- It also reduces the crosstalk in the multiplexer.

6.5.4 Applications of Sample and Hold circuits

- The applications of such sample and hold circuit are :
 - Digital interfacing.
 - Analog to digital converter circuits.
 - Pulse modulation systems.
 - In storage of outputs of a multiplexer between updates in data distribution systems.
 - In reset-stabilised op-amps.
 - In analog demultiplexers.

Review Questions

- What is sample and hold circuit ? Explain its operation with the help of circuit diagram.
- Define : i) Acquisition time ii) Aperture time.
- List and define the performance parameters of a sample and hold circuit.
- State the advantages and applications of sample and hold circuit.

6.6 A/D Converters

- The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word.
- The A/D converter is exactly opposite function that of the D/A converter.
- Fig. 6.6.1 shows symbol for A/D converter.

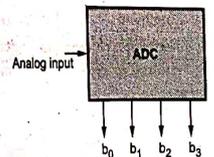


Fig. 6.6.1 Symbol for 4 bit ADC

Review Question

- What is A/D converter ?

6.7 Performance Parameters (Specifications of ADC)

GTU : Winter-17, 18, Summer-18

- The Fig. 6.7.1 shows the digital output of an ideal 3 bit ADC plotted against the analog input voltage.

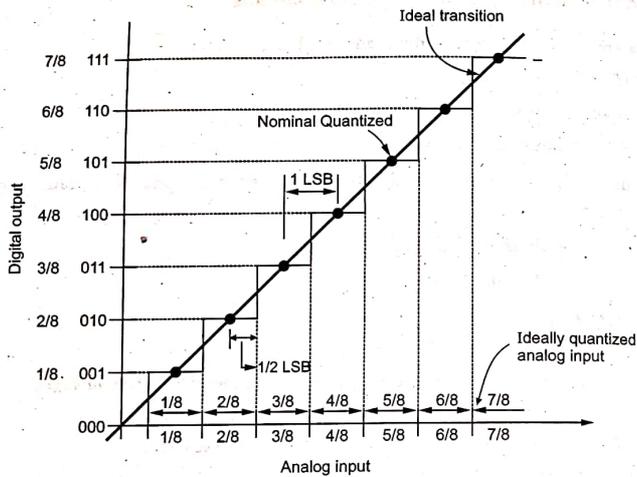


Fig. 6.7.1 Analog Input Vs digital output

Resolution

- Resolution is also defined as the ratio of a change in value of input voltage, V_i , needed to change the digital output by 1 LSB. If the full scale input voltage required to cause a digital output of all 1's is V_{IFS} , then resolution can be given as,

$$\text{Resolution} = \frac{V_{IFS}}{2^n - 1} \dots (6.7.1)$$

Quantization Error and Accuracy

- Fig. 6.7.1 shows that the binary output is 011 for all values of V_i between $\frac{1}{4}$ and $\frac{1}{2}$ V. There is an unavoidable uncertainty about the exact value of V_i when the output is 011. This uncertainty is specified as **quantization error**. Its value is $\pm \frac{1}{2}$ LSB.

- It is given as,

$$Q_E = \frac{V_{IFS}}{(2^n - 1) 2} \dots (6.7.2)$$

- Increasing the number of bits results in a finer resolution, a smaller quantization error and greater the accuracy. The quantization error can be observed by continuously sampling a time-varying analog signal. The quantization error can be observed by back to analog with a DAC, and taking the difference between the two. The resulting sawtooth-like signal, called **quantization noise**.
- The root mean square value of such signal, E_n can be given as,

$$E_n = \frac{V_{FS}}{2^n \sqrt{12}}$$

- This is related to the resolution of the system. For each additional bit of resolution E_n is cut in half, that is reduced by 6 dB.

Gain and Offset Errors

- The **offset error** is the difference between the actual and ideal first transition voltages. The term offset; however, implies that all conversions are off by an equal amount. On the other hand, the **gain error** is the difference between the actual full scale transition voltage and the ideal full-scale transition voltage. This is illustrated in Fig. 6.7.2.

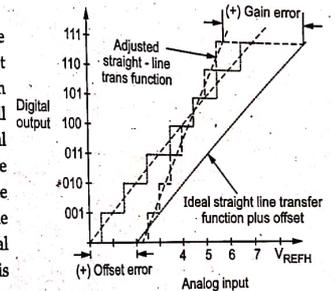


Fig. 6.7.2 Offset and gain error

Gain and Offset Drifts

- The **gain drift** is defined as a change in the full-scale transition voltage measured over the entire operating temperature range. It is usually expressed in parts per million per degree Celsius (ppm/°C).
- The **offset drift** is defined as a change due to temperature in the analog zero for an A/D converter operating in bipolar mode. It is also expressed in parts per million per degree Celsius (ppm/°C).

Sampling Frequency and Aliasing Phenomenon

- According to **sampling theorem**, the minimum rate at which the analog signal should be sampled twice the highest frequency in the analog signal. Thus

$$f_s \geq 2f_{max}$$

- With this frequency, it is possible to reproduce analog signal faithfully by using a suitable interpolation algorithm.
- If the sampling frequency is less than the Nyquist rate ($2 f_{max}$), then the faithful reproduction of original signal is not possible. However, in such cases, spurious signals called **aliases** are produced. The frequency of aliased signal is the difference between the signal frequency and the sampling frequency. This problem is called **aliasing** and it is removed in all practical A/D converters by using anti-aliasing filters.

Non Linearity or Integral Non-Linearity (INL)

- It is a measure of the maximum deviation of the actual ADC transfer function from a straight line drawn through the first and last code transition after correction for offset and gain errors. It gives a more pessimistic but useful estimation of the non-linearity than referring the linearity of the ADC characteristics to an arbitrary best fit curve drawn through the output codes.

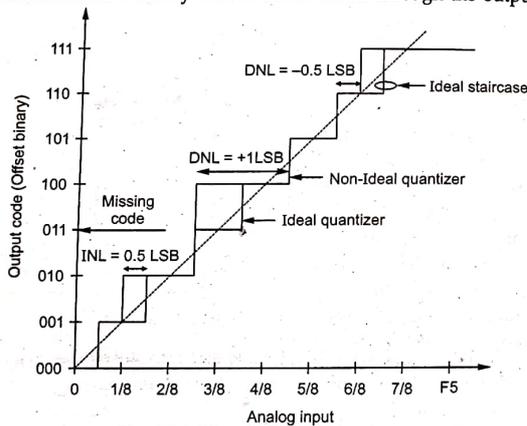


Fig. 6.7.3 INL and DNL analog input

Differential Non-Linearity (DNL)

- Differential Non-Linearity (DNL) is the maximum of the difference in the each conversion's Current Code Width (CCW) and the Ideal Code Width (ICW).
- DNL is the most critical of the measures of an ADC's performance for many control applications since it represents the ADC's ability to relate a small change in input voltage to the correct change in code conversion. DNL is defined as :

Code DNL = CCW - ICW

DNL = Max (Code DNL)

Conversion Time (Settling Time)

- It is an important parameter for ADC. It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used and the propagation delay of circuit components.

Aperture and Acquisition Times

- For accurate analog to digital conversion the analog input voltage should be held constant during the conversion cycle. If the analog input voltage changes by more than $\pm 1/2$ LSB an error can occur in the digital output code. To minimize the occurrence of these errors it is necessary to hold the value of the analog input this task. Aperture and acquisition times are the specifications of sample and hold circuits.
- These specifications are explained below with the help of S/H circuit waveform, shown in Fig. 6.7.4.

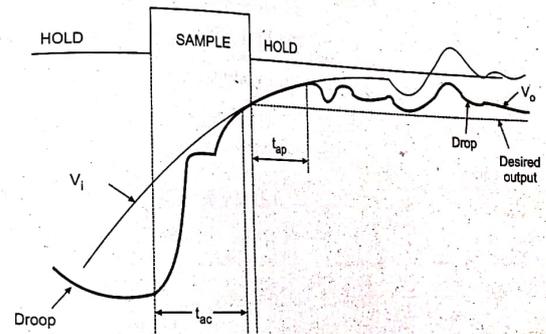


Fig. 6.7.4 S/H circuit waveforms

1. **Acquisition time (t_{ac})** : It is the time required for the holding capacitor C_H to charge up to a level close to the input voltage during sampling. It depends on three factors :
 - RC time constant
 - Maximum output current of op-amp
 - Slew rate of op-amp
2. **Aperture time (t_{ap})** : Because of propagation delays through the driver and switch, V_o will keep tracking V_i some time after the inception of the hold command. This is the aperture time. To get the precise timing, it is necessary to advance hold command by this amount.

3. Aperture uncertainty (Δt_{ap}): It is the variation in aperture time from sample to sample. Due to aperture uncertainty it is difficult to compensate aperture time by advancing hold command.

Code Width

- The code width is the change in input voltage that occurs between the output code transitions expressed in LSBs of full scale. Code width uncertainty is the dynamic variation or jitter in the code width causing noise.

Note: The specifications discussed above are to be considered for selection of ADC.

Example 6.7.1 An 8-bit ADC outputs all 1's when $V_i = 5.1$ V. Find its a) Resolution and b) Digital output when $V_i = 1.28$ V.

Solution:

From equation (6.7.1) we have,

$$\text{Resolution} = \frac{5.1 \text{ V}}{2^8 - 1} = 20 \text{ mV/LSB}$$

Therefore, we can say that to change output by 1 LSB we have to change input by 20 mV.

b) For 1.28 V analog input, digital output can be calculated as,

$$D = \frac{1.28 \text{ V}}{20 \text{ mV/LSB}} = 64 \text{ LSBs}$$

The binary equivalent of 64 is 0100 0000₂

Example 6.7.2 Calculate the quantizing error for 12-bit ADC with full scale input voltage 4.095 V.

Solution: From equation (6.7.2) we get

$$Q_E = \frac{4.095}{(2^{12} - 1) \times 2} = \frac{4.095}{(4096 - 1) \times 2} = 0.5 \text{ mV}$$

Review Questions

1. Explain the performance parameters of ADC.
2. Explain in detail specifications of ADCs.
3. State the specifications and errors associated with ADC. Also state the applications of ADC.
4. List various specifications of ADC.
5. Explain resolution and quantization error in reference to ADC. **GTU: Winter-17, Marks 4**
6. Give the points to be considered for selection of ADC. **GTU: Summer-18, Marks 3**
7. Define quantization error for ADC. **GTU: Summer-18, Marks 2**
8. Define following specification of ADC (i) Resolution (ii) Conversion time (iii) Quantization error. **GTU: Winter-18, Marks 3**

6.8 Types of A/D Converters

GTU: Winter-16, Summer-15, 16, 18

- Analog to digital converters are classified into two general groups based on the conversion techniques.
- One technique involves comparing a given analog signal with the internally generated reference voltages. This group includes successive approximation and flash type converters.
- The another technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. This group includes integrator converters and voltage-to-frequency converters.

6.8.1 Dual Slope ADC

- Dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator and then measured by a counter. The speed of this conversion is slow but the accuracy is high.
- Fig. 6.8.1 shows a typical dual slope converter circuit. It consists of integrator (ramp generator), comparator, binary counter, output latch and reference voltage.
- The ramp generator input is switched between the analog input voltage V_i and a negative reference voltage, $-V_{REF}$.
- The analog switch is controlled by the MSB of the counter. When the MSB is a logic 0, the voltage being measured is connected to the ramp generator input. When MSB is logic 1, the negative reference voltage is connected to the ramp generator.

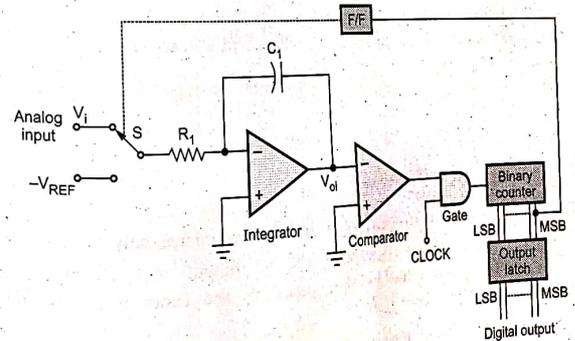


Fig. 6.8.1 Dual slope A/D converter

- At time $t = 0$, analog switch S is connected to the analog input voltage V_i , so that the analog input voltage integration begins. The output voltage of the integrator can be given as,

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t V_i dt = \frac{-V_i t}{R_1 C_1}$$

where $R_1 C_1$ is the integrator time constant and V_i is assumed constant over the integration time period.

- At the end of 2^N clock periods MSB of the counter goes high. As a result the output of the flip-flop goes high, which causes analog switch S to be switched from V_i to $-V_R$. At this very same time the binary counter which has gone through its entire count sequence is reset.

- The negative input voltage ($-V_R$) connected to the input of integrator causes the integrator output to ramp positive. When integrator output reaches zero, the comparator output voltage goes low, which disables the clock AND gate. This stops the clock pulses reaching the counter, so that the counter will be stopped at a count corresponding to the number of clock pulses in time t_2 .

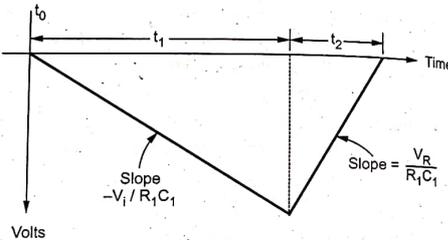


Fig. 6.8.2 Integrator output voltage

- The integrator output ramp down to a voltage V and get back upto 0. Therefore, the charge voltage is equal to discharge voltage and we can write,

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$V_i t_1 = V_R t_2$$

$$t_2 = \frac{V_i t_1}{V_R}$$

- The above equation shows that t_2 is directly proportional only to the V_i , since V_R and t_1 are constants. The binary digital output of the counter gives corresponding digital value for time period t_2 and hence it is also directly proportional to input signal V_i .
- The actual conversion of analog voltage V_{in} into a digital count occurs during t_2 . The control circuit connects the clock to the counter at the beginning of t_2 . The

clock is disconnected at the end of t_2 . Thus the counter contents is digital output. Hence we can write,

$$\text{Digital output} = \left(\frac{\text{counts}}{\text{second}} \right) t_2$$

But from equation of t_2 we can write,

$$\text{Digital output} = \left(\frac{\text{counts}}{\text{second}} \right) t_1 \left(\frac{V_i}{V_R} \right)$$

- The counter output can then be connected to an appropriate digital display.
- The advantages of dual slope ADC are
 - It is highly accurate.
 - Its cost is low.
 - It is immune to temperature caused variations in R_1 and C_1 .
 - The only disadvantage of this ADC is its speed which is low.

Example 6.8.1 For a particular dual slope ADC, t_1 is 83.33 ms and the reference voltage is 100 mV. Calculate t_2 if i) V_i is 100 mV and ii) 200 mV.

Solution : We know that,

$$t_2 = \left(\frac{V_i}{V_R} \right) t_1$$

i) $t_2 = \left(\frac{100}{100} \right) (83.33) = 83.33 \text{ ms}$

ii) $V_i = 200 \text{ mV}$

$$\therefore t_2 = \left(\frac{200}{100} \right) (83.33) = 166.6 \text{ ms}$$

Example 6.8.2 Find the digital output of an ADC having t_1 as 83.33 ms and V_R as 100 mV for an input voltage of + 100 mV. The clock frequency is 12 kHz.

Solution : The digital output is given as,

$$\text{Digital output} = \left(\frac{\text{counts}}{\text{second}} \right) t_1 \left(\frac{V_i}{V_R} \right)$$

Now clock frequency = 12 kHz

$$\text{i.e.} = 12000 \frac{\text{counts}}{\text{second}}$$

$$\therefore \text{Digital output} = 12000 \times 83.33 \times \left(\frac{100}{100} \right) \times 10^{-3} = 1000 \text{ counts}$$

6.8.2 Successive Approximation ADC

- In this technique, the basic idea is to adjust the DAC's input code such that its output is within $\pm \frac{1}{2}$ LSB of the analog input V_i to be A/D converted. The code that achieves this represents the desired ADC output.
- The successive approximation method uses very efficient code searching strategy called binary search. It completes searching process for n-bit conversion in just n clock periods.
- Fig. 6.8.3 shows the block diagram of successive approximation A/D converter. It consists of a DAC, a comparator and a successive approximation register (SAR).

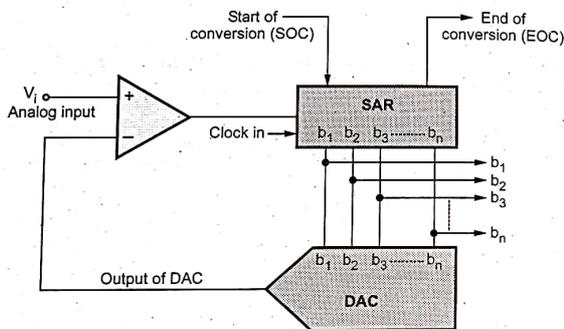


Fig. 6.8.3 Block diagram of successive approximation A/D converter

- The external clock input sets the internal timing parameters. The control signal start of conversion (SOC) initiates an A/D conversion process and end of conversion signal is activated when the conversion is completed.

Operation :

- The searching code process in successive approximation method is similar to weighing an unknown material with a balance scale and a set of standard weights.
- Let us assume that we have 1 kg, 2 kg and 4 kg weights (SAR) plus a balance scale (comparator and DAC). Now we will see the successive approximation analogy for 3-bit ADC.

- Refer Fig. 6.8.3 and 6.8.4. The analog voltage V_{in} is applied at one input of register sets 3-bit binary code 100₂ ($b_2 = 1$) as an input of DAC. This is similar process of placing the unknown weight on one platform of the balance and 4 kg weight on the other.

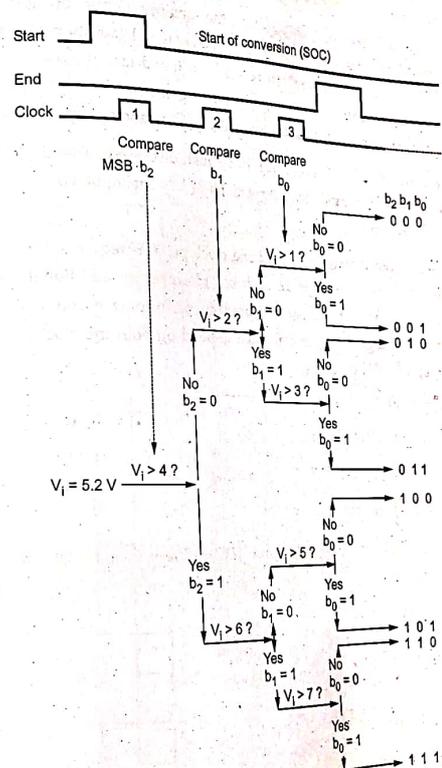


Fig. 6.8.4 Illustration of conversion process

- Fig. 6.8.5 shows 3-bit flash A/D converter. For this ADC, seven $(2^3 - 1)$ comparators are required. As shown in the Fig. 6.8.5, one input of each voltage level generated by the reference voltage divider. The reference voltage (V_{REF}) is equal to the full scale input signal voltage. The manner in which the flash A/D converter performs a quantization is relatively simple.
- The comparators give output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referred above the input signal, remain turned-off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The code resulting from this comparator is converted to a binary code by the encoder.
- The number of comparators required for n-bit resolution is,
Number of comparators = $2^n - 1$
- As seen earlier the quantization error is $\pm \frac{1}{2}$ LSB. Thus for an ADC, the maximum frequency for a sine wave V_{in} to be digitized within an accuracy of $\pm \frac{1}{2}$ LSB is,

$$f_{max} \cong \frac{1}{2\pi(T_c)2^n}$$

where f_{max} = Maximum input frequency

T_c = Conversion time

n = Number of bits

Example 6.8.4 For a particular 8-bit ADC, the conversion time is 9 μ s. Find the maximum frequency of an input sine wave that can be digitized.

Solution : The maximum frequency is given by,

$$f_{max} \cong \frac{1}{2\pi(T_c)2^n} \cong \frac{1}{2\pi \times 9 \times 10^{-6} \times 2^8} \cong 69.07 \text{ Hz}$$

6.8.4 Comparison between ADCs

- The comparison of ADCs is given in the tabular form as below.

Parameter	Flash (Parallel comparators)	Successive approximation	Dual slope
Speed	Fastest	Fast	Slow
Accuracy	Less	Medium	More

Resolution	Upto 2^8	Upto 2^{16}	2^{16} or even more
Input hold time	Very less	Depends on number of bits. It is more than flash A/D converter.	It is maximum, hence sample and hold circuit is required.
Cost	Very costly	Medium	Less
Applications	High speed fiber optic communication, digital storage oscilloscope, imaging and many more where high speed A/D conversion is required.	The successive approximation A/D converter has the disadvantage of requiring D/A converter, but it has the advantage of high speed with excellent resolution. Hence these are most popular and used in data acquisition systems.	These are used when high accuracy and resolution is required and speed is not the important criteria.

IC	Resolution	Conversion rate	IC	Resolution	Conversion rate	IC	Resolution	Conversion rate
AD6020KD	6	50 MHz	ADC1103	8	1 MHz	ADC141	14	25 Hz
AD9000SD	6	75 MHz	ADC80	10	470 kHz	7109	12	30 Hz
TM1070	7	15 MHz	ADC1103	12	300 kHz	ADB1200	12	28 Hz
TDC10193	9	25 MHz	ADC12	16	20 kHz	LF13300	12	28 Hz

6.8.5 Counter Type A/D Converter

- This ADC uses DAC for A to D conversion. The output of the DAC is continuously compared with the analog input to the ADC which is to be converted into digital output. When the output of the DAC becomes greater than this analog input, the corresponding digital input to the DAC is noted which represents the analog input to the ADC.
- Fig. 6.8.6 shows the circuit diagram of counter type ADC.
- As shown in the Fig. 6.8.6, the counter type ADC consists of a binary counter, DAC, comparator and AND gate. The operation of the circuit is explained below.
 - Initially, the counter is reset, i.e. its output is set to zero by applying a reset pulse. The output of the counter is given as digital input to DAC. Since input to DAC is zero, its output V_D is zero.
 - When the analog input voltage V_A is applied to ADC, it becomes greater than V_D . V_A acts as input voltage for noninverting terminal and V_D acts as input voltage for inverting terminal of the comparator. Since V_A is greater than V_D , the comparator output goes high.

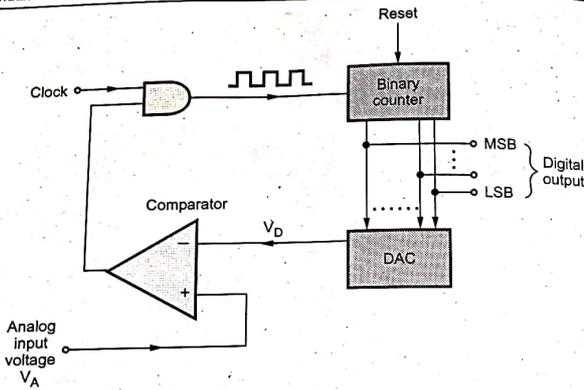


Fig. 6.8.6

- iii) For an AND gate, one input is clock pulses and another input is the output of the comparator. Because of the high output of the comparator, the clock pulses are allowed to pass through the AND gate.
- iv) The counter starts counting these clock pulses. According to the number of clock pulses, the output of the counter goes on increasing. This increases the output of the DAC.

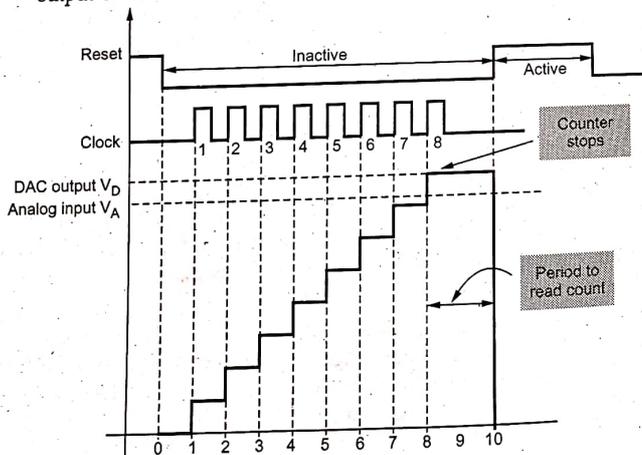


Fig. 6.8.7 Waveforms for counter type ADC

- v) The above steps are continued till V_D is less than V_A .
- vi) As soon as DAC output V_D becomes greater than V_A , the comparator output goes low. This disables AND gate. So the clock pulses are not allowed to pass through the AND gate. The counting process of the binary counter is stopped.
- vii) The output of the binary counter which is in digital form is noted which represents the digital equivalent of the analog input voltage V_A .
- viii) For the next A to D conversion, the input voltage to ADC, V_A changes. The binary counter is cleared by applying a second reset pulse and all the above steps are repeated to obtain the digital equivalent of V_A .

Disadvantages

- It is necessary to give enough time for DAC conversion and comparator to respond. Therefore, there is a limitation on the clock frequency. As clock frequency is low, the speed of conversion is less.
- Conversion time is not constant. It increases with increase in input voltage. In other words, we can say that conversion time is high at high input voltage.

6.8.6 Tracking Type Continuous A/D Conversion

- The tracking type converter is similar to counter type converter; however in this converter the counter starts counting from the most recent code rather than restarting from zero. Such an arrangement increases conversion speed, if signal changes in the input signal are minor since the last conversion. Increase in conversion speed is achieved because fewer counts are required for the DAC output to catch up with V_i when input changes are minor.
- The tracking type converter is also called servo converter or continuous A/D converter. The Fig. 6.8.8 shows the tracking type ADC. It consists of up/down counter, a comparator, DAC and the control circuitry. Here, comparator output controls the direction of count. Counting will be up or down depending on whether the DAC output is below or above V_i , i.e. comparator output is logic 0 or logic 1. Whenever, the DAC output crosses V_i , the comparator changes state and generates positive going or negative going edge at the output. This edge can be taken as EOC command, so that counter stops counting when comparator changes its state. The edge detection is achieved by using two D flip-flops. Flip-flop 1 is its state. The edge detection is achieved by using two D flip-flops. Flip-flop 1 is used to detect positive edge whereas flip-flop 2 is used to detect negative edge. Initially, with the activation of start of conversion (SOC) signal the output of both flip-flops are set to logic 1. Since, the D input of both the flip-flops is connected to logic 0, upon detection of the edge, the flip-flop output goes to logic 0 and logic 1, respectively. As a result, the counter stops counting. When comparator output goes from logic 1 to logic 0, negative edge is generated and it resets

flip-flop 2 whereas when comparator output goes from logic 0 to logic 1, positive edge is generated and it resets flip-flop 1. When either of the two flip-flop gets reset, the clock is disabled.

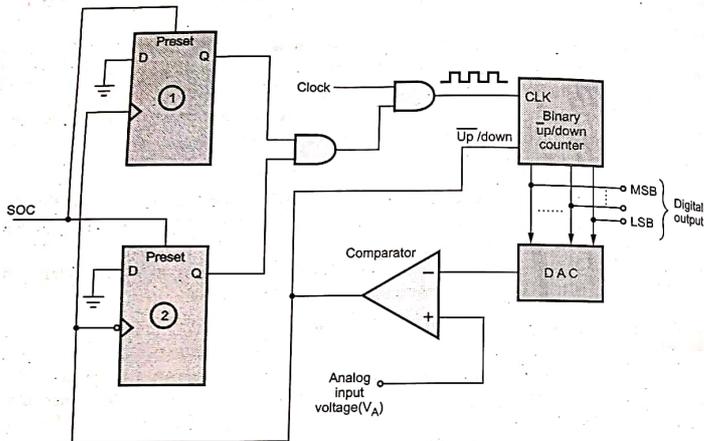


Fig. 6.8.8 Tracking type ADC

Review Questions

1. Which are different methods for A/D conversion.
2. Explain the dual slope A/D conversion technique with the help of block diagram.
3. Explain the operation of flash A/D converter.
4. Compare three A/D conversion techniques.
5. Write a note on counter type A/D converter.
6. Explain the tracking type continuous A/D converter.
7. Explain working of successive approximation type ADC.
8. Explain the working of analog to digital converter with necessary diagram.

GTU : Winter-16 Marks 4

GTU : Summer-18 Marks 7

GTU : Summer-15 Marks 7

GTU : Summer-16 Marks 7

6.9 A/D Converter using V/F Converter

- An A/D converter using the voltage to frequency is shown in Fig. 6.9.1. The voltage to frequency converter section consists of an integrator, a comparator and a monostable multivibrator. The analog input voltage is applied to the integrator whose output is applied to the inverting input terminal of the comparator.
- The comparator output activates a monostable multivibrator to produce a short pulse to control the active switch S of the integrator. The comparator generates a pulse train and whose frequency F can be defined as

$$F = \frac{1}{RC} \left(\frac{V_a}{V_r} \right)$$

- The equation shows that comparator output signal frequency F is proportional to the analog input voltage V_a .
- The output of the voltage to frequency converter is applied to the clock input of an N-bit binary counter through an AND gate. So we can apply the clock pulses to the binary counter for specific time period, say T_1 and the counter will count the number of pulses for that duration. If the number of pulses recorded at counter in time T_1 is n, then $T_1 \times F = n$

$$n = \frac{1}{RC} \frac{V_a}{V_r} \cdot T_1$$

- From above expression we can observe that number of pulses counted in the counter is proportional to the analog input voltage and thus we obtain the equivalent digital form of the analog voltage.

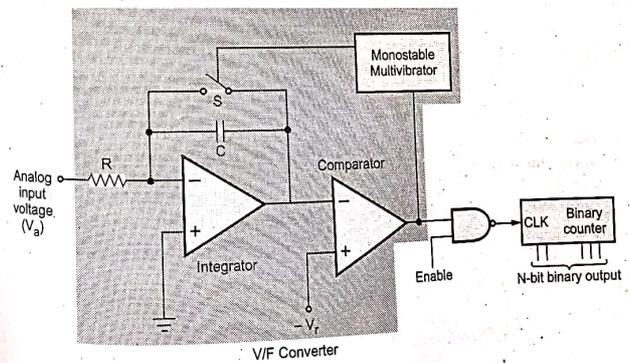


Fig. 6.9.1 A/D converter using V/F converter

Review Question

1. Explain the operation of A/D converter using V/F converter.

6.10 A/D Converter using V/T Conversion

- The concept of A/D converter using voltage to time conversion is very much similar to the A/D converter with voltage to frequency conversion, as the digital output for both the types of converter is derived by counting the number of pulses that is proportional to the analog input voltage. The difference is that on A/D converter using V/F conversion is based on the counting of pulses of variable frequency for fixed time duration, whereas the A/D converter using voltage to time conversion counts the pulses of fixed frequency but of variable time.
- Fig. 6.10.1 shows the schematic diagram of the A/D converter using voltage to time conversion.

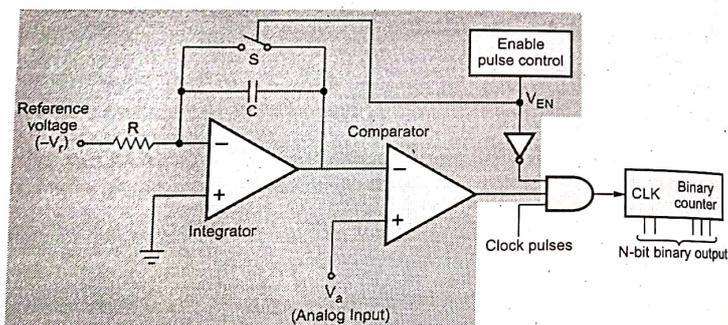


Fig. 6.10.1 A/D converter using voltage to time conversion

- The comparator output is applied to one of the inputs of a 3-input AND gate, where other two inputs of AND gates are complement of V_{EN} and clock pulses of time period T_c . As long as comparator output is high and V_{EN} is low, the clock pulses are applied to the binary counter for count operation.
- If the counter records the counting of n number of pulses with pulse time period is T_c , then $T = nT_c$

where
$$T = \frac{V_a RC}{V_r} \text{ s}$$

$$\therefore n = \frac{V_a RC}{V_r T_c}$$

- From this expression we can observe that the counter reading is proportional to the analog input voltage.

Review Question

1. Explain the working of A/D converter using voltage to time conversion.

6.11 Example of A/D Converter IC

- The ADC 0808 and ADC 0809 are monolithic CMOS devices with an 8-channel multiplexer.
- These devices are also designed to operate from common microprocessor control buses, with tri-state output latches driving the data bus.

6.11.1 Features

- 8-bit successive approximation ADC.
- 8-channel multiplexer with address logic.
- Conversion time 100 μs .
- It eliminates the need for external zero and full-scale adjustments.
- Easy to interface to all microprocessors.
- It operates on single 5 V power supply.
- Output meet TTL voltage level specifications.

6.11.2 Pin Diagram

Fig. 6.11.1 shows pin diagram of 0808/0809 ADC. (See Fig. 6.11.1 on next page)

6.11.3 Operation

- ADC 0808/0809 has eight input channels, so to select desired input channel, it is necessary to send 3-bit address on A, B and C inputs.
- The address of the desired channel is sent to the multiplexer address inputs through port pins. After atleast 50 ns, this address must be latched. This can be achieved by sending ALE signal. After another 2.5 μs , the start of conversion (SOC) signal must be sent high and then low to start the conversion process. To indicate end of conversion ADC 0808/0809 activates EOC signal.
- The microprocessor system can read converted digital word through data bus by enabling the output enable signal after EOC is activated. This is illustrated in Fig. 6.11.2.

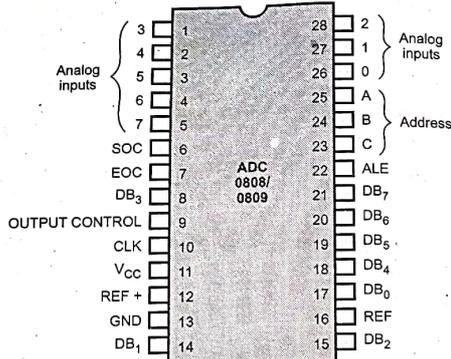


Fig. 6.11.1 Pin diagram of 0808/0809

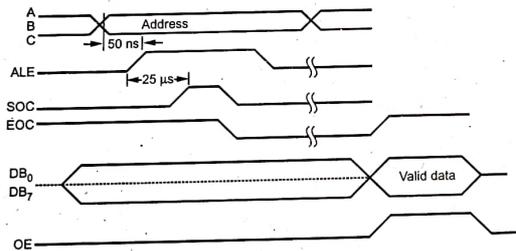


Fig. 6.11.2 Timing waveforms for ADC 0808

6.11.4 Interfacing

- Fig. 6.11.3 shows typical interfacing circuit for ADC 0808 with microprocessor system.
- The zener diode and LM 308 amplifier circuitry is used to produce a V_{CC} and $+V_{REF}$ of 5.12 V for the A/D converter. With this reference voltage the A/D converter will have 256 steps of 20 mV each.

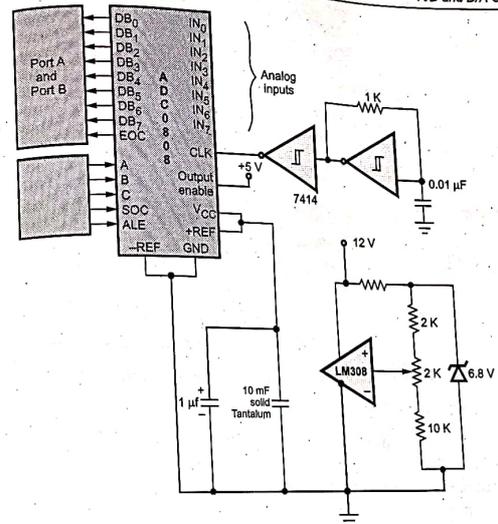


Fig. 6.11.3 Typical interface for 0808/0809

Example 6.11.1 An 8-bit digital ramp ADC with a 40 mV resolution uses a clock frequency of 2.5 MHz, a comparator with $V_T = 1$ mV. Determine the following values:

- The digital output for $V_{in} = 6.000$ V.
- The digital output for $V_{in} = 6.035$ V.
- The maximum and average conversion times for this ADC.

Solution : The digital output is given by,

$$\text{Count} = \frac{V_{in}}{\text{Resolution}}$$

i) $V_{in} = 6.000$ V

$$\text{Count} = \frac{6.000}{40 \times 10^{-3}} = 150$$

ii) $V_{in} = 6.035$ V

$$\therefore \text{Count} = \frac{6.035}{40 \times 10^{-3}} \approx 150$$

$$\text{iii) } (T_c)_{\text{max}} = (\text{Maximum count}) \times T$$

$$= (2^n - 1) \times \frac{1}{f} = \frac{(255)}{2.5 \times 10^6} = 102 \mu\text{s}$$

$$(T_c)_{\text{average}} = \frac{(T_c)_{\text{max}}}{2} = 51 \mu\text{s}$$

Example 6.11.2 Use successive approximation type ADC to convert the analog voltage 7.28 V to 8-bit binary. If $V_R = 10$ V, determine the final binary answer and the error present. Show the timing waveforms that would occur in the successive approximation ADC process.

Note: V_R = Full scale input voltage to the DAC.

Solution: The reference voltage V_R is full scale input voltage to the DAC.

Hence the 10 V reference corresponds to 2^8 levels i.e. $2^8 = 256$ levels.

Hence one level corresponds to,

$$= \frac{10}{256} = 0.03906 \text{ V}$$

This is nothing but the resolution of the ADC.

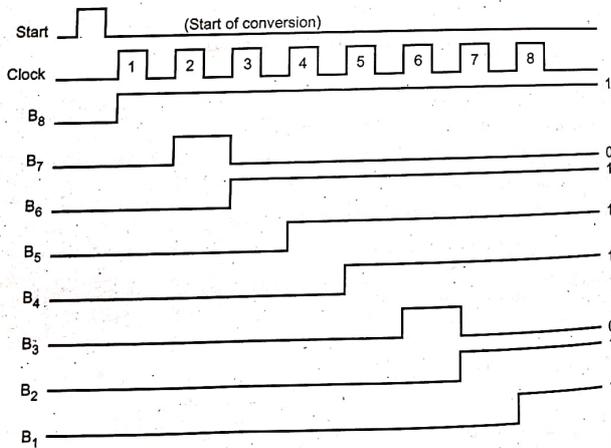


Fig. 6.11.4

The timing waveforms are shown in the Fig. 6.11.4.

Hence the final binary number is,

$$= (10111011)_2$$

Hence the total output count is,

$$= (1 \times 128) + (0 \times 64) + (1 \times 32) + (1 \times 16) + (1 \times 8) + (0 \times 4) + (1 \times 2) + (1 \times 1)$$

$$= 187$$

$$\therefore \text{Actual output} = \text{Count} \times \text{Resolution} = 187 \times 0.03906 = 7.3046 \text{ V}$$

$$\text{Exact value} = 7.28 \text{ V}$$

$$\text{Error} = 7.3046 - 7.28 = 0.024 \text{ V}$$

Review Questions

1. List the features of ADC 0808.
2. Explain the interfacing of ADC 0808 to the microprocessor.



Notes

7

Semiconductor Memories and Programmable Logic Devices

Contents

7.1	Introduction	Summer-16,	Marks 7
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7.8	Expanding Memory Size		
7.9	Content Addressable Memory (CAM)		
7.10	Charge - Coupled Devices (CCD) Memory		
7.11	Programmable Logic Devices		
7.12	ROM / PROM as a PLD	Winter-15, 18, Summer-18,	Marks 7
7.13	Programmable Logic Array (PLA)	Dec.-12, May-13,	
		Winter-16	Marks 7
7.14	Programmable Array Logic (PAL)		
7.15	Comparison between PROM, PLA and PAL		
7.16	Complex Programmable Logic Devices (CPLDs)		
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	Oral Questions and Answers		

(7 - 1)

7.1 Introduction

GTU : Summer-16

- Memories are made up of registers. Each register in the memory is one storage location also called **memory location**. Each memory location is identified by an **address**. The number of storage locations can vary from a few in some memories to hundreds of thousand in others. Each location can accommodate one or more bits. Generally, the total number of bits that a memory can store is its **capacity**. Most of the types the capacity is specified in terms of bytes (group of eight bits).
- Each register consists of storage elements (flip-flops or capacitors in semiconductor memories and magnetic domain in magnetic storage), each of which stores one bit of data. A storage element is called a **cell**.
- The data stored in a memory by a process called **writing** and are retrieved from the memory by a process called **reading**. Fig. 7.1.1 illustrates in a very simplified way the concept of write, read, address and storage capacity for a generalized memory.
- As shown in the Fig. 7.1.1 a memory unit stores binary information in groups of bits called **words**. A word in memory is an entity of bits that moves in and out of storage as a unit. A word having group of 8-bits is called a **byte**. Most computer memories use words that are multiples of eight bits in length. Thus, a 16-bit word contains two bytes, and a 32-bit word is made of 4-bytes.

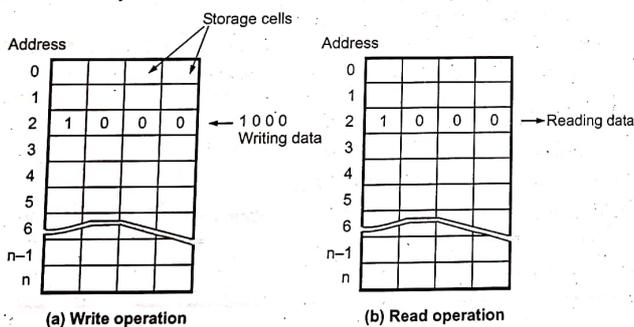


Fig. 7.1.1

- The communication between a memory and its environment is achieved through data lines, address selection lines, and control lines that specify the direction of transfer. The Fig. 7.1.2 shows the block diagram of memory unit. Then data lines provide the information to be stored in memory and the k address lines specify the particular word chosen among the many available. The two control inputs specify the direction transfer.

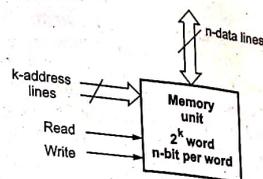


Fig. 7.1.2 Block diagram of memory unit

When there are k address lines we can access 2^k memory words. For example, if $k = 10$ we can access $2^{10} = 1024$ memory words.

Illustrative Examples

Example 7.1.1 A bipolar RAM chip is arranged as 16 words. How many bits are stored in the chip?

Solution : $16 \times 8 = 128$ bits \therefore one word = 8 bits.

Example 7.1.2 How many address bits are needed to operate a $2K \times 8$ ROM?

Solution : $2K$ memory locations = 2048 locations
Since $2^{11} = 2048$, we need 11 address lines.

Example 7.1.3 How many locations are addressed using 18 address bits?

Solution : The number of locations addressed = $2^{18} = 262144$.

Example 7.1.4 How many words a 16×8 memory can store? **GTU : Summer-16, Mark 1**

Solution : 16×8 memory can store sixteen eight bit words.

7.1.1 Computer Memory

Memory is internal storage areas in the computer system. It is used to store data and instructions. Computer memory is the storage space in the computer, where data is to be processed and instructions required for processing are stored. The memory is divided into large number of small parts called cells. Each location or cell has a unique address, which varies from zero to memory size minus one. For example, if the computer has 64K words, then this memory unit has $64 \times 1024 = 65536$ memory locations. The address of these locations varies from 0 to 65535.

Memory is primarily of three types :

- Primary memory/Main memory
- Cache memory

- Secondary memory
- **Primary memory (main memory)** : Primary memory holds only those data and instructions on which the computer is currently working. It has a limited capacity and data is lost when power is switched off (i.e. it is volatile memory). It is generally made up of semiconductor device. These memories are not as fast as registers. The data and instruction required to be processed resides in the main memory. It is divided into two subcategories RAM and ROM.
- **Cache memory** : Cache memory is a very high speed semiconductor memory which can speed up the CPU. It acts as a buffer between the CPU and the main memory. It is used to hold those parts of data and program which are most frequently used by the CPU. The parts of data and programs are transferred from the disk to cache memory by the operating system, from where the CPU can access them.
- **Secondary memory** : This type of memory is also known as external memory or non-volatile. It is slower than the main memory. These are used for storing data/information permanently. CPU directly does not access these memories, instead they are accessed via input-output routines. The contents of secondary memories are first transferred to the main memory and then the CPU can access it. For example, disk, CD-ROM, DVD, etc.

Review Questions

1. Define a memory cell. Give an example.
2. Define a 'memory location' and a 'cell'.
3. Write a descriptive note on memories.
4. What is the memory capacity of random access memory if it has 10 bit address lines ?
5. Write a short note on memory.

GTU : Summer-16, Marks 7

7.2 Characteristics of Memories

Location :	CPU Internal (main) External (Secondary)
Capacity :	Word size Number of words
Unit of transfer :	Word Block

- Access method :** Sequential access
Direct access
Random access
Associative access
- Performance :** Access time, Cycle time, Transfer rate
- Physical type :** Semiconductor Magnetic surface
- Physical characteristics :** Volatile / non-volatile
- Organization :** Erasable / Non-erasable

Table 7.2.1

Location :	The computer memory is placed in three different locations:
CPU	It is in the form of CPU registers and its internal cache memory (16 kbytes in case of Pentium)
Internal	It is the main memory of the system which CPU can access directly.
External	It is in the form of secondary storage devices such as magnetic disk, tapes etc. The CPU accesses this memory with the help of I/O controllers.
Capacity :	It is expressed using two terms : Word size and number of words.
Word size	It is expressed in bytes (8-bit). The common word sizes are 8, 16 and 32-bits.
Number of word	This term specifies the number of words available in the particular memory device. For example, if memory capacity is 4 K × 8, then its word size is 8 and number of words are 4 K = 4096.
Unit of transfer :	It is the maximum number of bits that can be read or written into the memory at a time. In case of main memory, most of the times it is equal to word size. In case of external memory, unit of transfer is not limited to word size, it is often larger than a word and it is referred to as blocks.
Access methods :	There are two different methods generally used for memory access.

- Sequential access** Here, memory is organized into units of data, called *records*. If current record is 1, then in order to read record N, it is necessary to read physical records 1 through N - 1. A tape drive is an example of sequential access memory.
- Random access** Here, each addressable location in memory has a unique address. It is possible to access any memory location at random.
- Performance :** The performance of the memory system is determined using three parameters :
- Access time** In case of random access memory, it is the time taken by memory to complete read/write operation from the instant that an address is sent to the memory. On the other hand, for non-random access memory, access time is the time it takes to position the read-write mechanism at the desired location.
- Memory cycle time** This term is used only in concern with random access memory and it is defined as access time plus additional time required before a second access can commence.
- Transfer rate** It is defined as the rate at which data can be transferred into or out of a memory unit.
- Physical type :** Two most common physical types used today are *semiconductor memory* and *magnetic surface memory*.

Physical characteristics :

Volatile / Non-volatile If memory can hold data even if power is turned off, it is called as non-volatile memory; otherwise it is called as volatile memory.

Erasable / Non-erasable The memories in which data is once programmed cannot be erased are called as non-erasable memories. On the other hand, if data in the memory is erasable then memory is called as erasable memory.

Review Question

1. List the different characteristics of memories.

7.3 Classification of Memories

- The Table 7.3.1 shows the classification of semiconductor memory devices. The semiconductor memory devices can be categorized in several ways according to their functional and architectural characteristics.

Classification of semiconductor memories			
Non-volatile memory		Volatile memory	
Read Only Memory (ROM)	Read/Write Memory (NVRAM)	Read/Write Memory (RWM)	
• Mask-Programmable ROM	• EPROM	Random Access	Non-Random Access
• Programmable ROM	• EEROM		
	• FLASH	• SRAM	• FIFO
		• DRAM	• LIFO
			• Shift Register

Note :

- ROM : Read Only Memory
- PROM : Programmable ROM
- EPROM : Erasable PROM
- EEPROM : Electrically Erasable PROM
- SRAM : Static Random Access Memory
- DRAM : Dynamic Random Access Memory
- FIFO : First-in First-out
- LIFO : Last-in First-out

Table 7.3.1 Classification of semiconductor memories

- Boardly semiconductor memories are classified as volatile memories and non-volatile memories. Volatile memories can retain their state as long as power is applied. On the other hand, non-volatile memories can hold data even if power is turned off. Read/Write Memories (RWMs) are those memories, which allows both read and write operations. They are used in applications where data has to change continuously. They are also used for temporary storage of data. ROM memories allow only read operation. They are used to store monitor programs and constants used in the program.
- The volatile memories which can hold data as long as power is ON are called static RAMs (SRAMs). Dynamic RAMs (DRAMs) stores the data as a charge on the capacitor and they need refreshing of charge on the capacitor after every few milliseconds to hold the data even if power is ON.
- EPROM and EEPROM are erasable memories in which the stored data can be erased and new data can be stored.

- The semiconductor memories are also classified as Bipolar and MOS memories depending upon the type of transistors used to construct the individual cell.

Review Questions

- Describe the classification of semiconductor memories.
- Which memory is called volatile? Why?
- What is meant by 'static' and 'dynamic' memories?
- Explain static memory.
- Discuss the classification of ROM and RAM memories.

7.4 Serial (Sequential) Random Access Memories

The Table 7.4.1 shows the comparison between serial and random access memories.

Sr. No.	Serial access memories	Random access memories
1.	Use serial access method.	Use random access method.
2.	Memory is organized into units of data, called records. Records are accessed sequentially. If current record is 1, then in order to read record N, it is necessary to read physical records 1 through N-1.	Each storage location in the memory has an unique address and it can be accessed independently of the other locations.
3.	Memory access time is dependent on the position of storage location.	Memory access time is independent of storage location being accessed.
4.	The time required to bring the desired location into correspondence with a read-write head increases effective access time, so serial access tends to be slower than random access.	Memory access time is less.
5.	Cheaper than random access memories.	Random access memories are comparatively costly.
6.	Nonvolatile memories.	May be volatile or nonvolatile depending on physical characteristics.
7.	Magnetic tape is an example of serial access memories.	Semiconductor memories are random access memories.

Table 7.4.1 Comparison between serial and random access memories

Review Question

- Give the comparison between serial access and random access memories.

7.5 Read Only Memory (ROM)

GTU : Winter-14, 18

- We can't write data in read only memories. It is non-volatile memory i.e. it can hold data even if power is turned off. Generally, ROM is used to store the binary codes for the sequence of instructions you want the computer to carry out and change. This is because this type of information does not change.
- It is important to note that although we give the name RAM to static and dynamic read/write memory devices, that does not mean that the ROMs that we are using are also not random access devices. In fact, most ROMs are accessed randomly with unique addresses.
- The Fig. 7.5.1 shows the typical configuration of a ROM cell. It consists of a transistor T and switch P. The transistor T is driven by the word line. The contents of cell can be read from the cell when word line is logic 1. A logic value 0 is read if the transistor is connected to ground through switch P. If switch P is open, a logic value 1 is read. The bit line is connected through a resistor to the power supply. A sense circuit at the end of the bit line generates the proper output value. Data is stored into a ROM when it is manufactured.

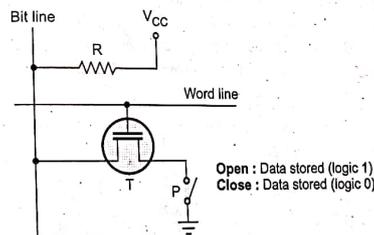


Fig. 7.5.1 ROM cell

- There are four types of ROM : Masked ROM, PROM, EPROM and EEPROM or E²PROM.

7.5.1 PROM (Programmable Read Only Memory)

- PROMs are programmed by user. To provide the programming facility, each address select and data line intersection has its own fused MOSFET or transistor. When the fuse is intact, the memory cell is configured as a logic 1 and when fuse is blown (open circuit), the memory cell is logical 0. Logical 0s are programmed by selecting the appropriate select line and then driving the vertical data line with a pulse of high current. The Fig. 7.5.2 shows a PROM fused MOSFET memory cell.

- Fig. 7.5.3 shows four byte PROM. It has diodes in every bit position; therefore, the output is initially all 0s. Each diode, however has a fusible link in series with it. By addressing bit and applying proper current pulse at the corresponding output, we can blow out the fuse, storing logic 1 at that bit position. The fuse uses material like nichrome and polycrystalline. For blowing the fuse it is necessary to pass around 20 to 50 mA of current for period 5 to 20 μ s.

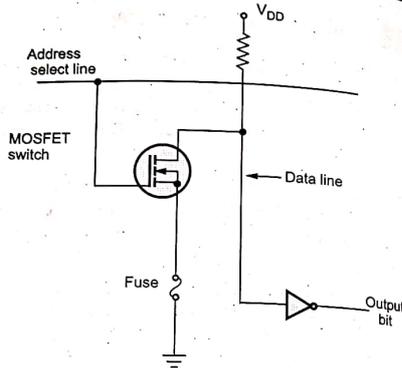


Fig. 7.5.2 Single fused PROM cell

The blowing of fuses according to the truth table is called programming of ROM. The user can program PROMs with special PROM programmer. The PROM programmer selectively burns the fuses according to the bit pattern to be stored. This process is also known as burning of PROM. The PROMs are one time programmable. Once programmed, the information stored is permanent.

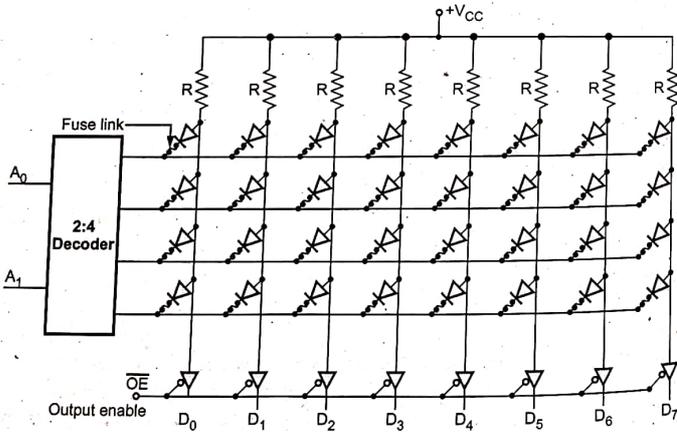


Fig. 7.5.3 Four byte PROM

7.5.2 EPROM (Erasable Programmable Read Only Memory)

- Erasable programmable ROMs use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. EPROMs can be programmed by the user with a special EPROM programmer. The important point is that we can erase the stored data in the EPROMs by exposing the chip to ultraviolet light through its quartz window for 15 to 20 minutes, as shown in the Fig. 7.5.4.

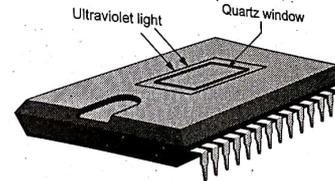


Fig. 7.5.4 EPROM

- It is not possible to erase selective information, when erased the entire information is lost. The chip can be reprogrammed. This memory is ideally suitable for product development, experimental projects and college laboratories, since this chip can be reused many times, over.

EPROM Programming :

- When erased each cell in the EPROM contains 1. Data is introduced by selectively programming 0's into the desired bit locations. Although only 0's will be programmed, both 1's and 0's can be presented in the data.
- During programming address and data are applied to address and data pins of the EPROM. When the address and data are stable, program pulse is applied to the program input of the EPROM. The program pulse duration is around 50 ms and its amplitude depends on EPROM IC. It is typically 5.5 V to 25 V. In EPROM, it is possible to program any location at any time - either individually, sequentially, or at random.

7.5.3 EEPROM (Electrically Erasable Programmable Read Only Memory)

- Electrically erasable programmable ROMs also use MOS circuitry very similar to that of EPROM. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. The insulating layer is made very thin ($< 200 \text{ \AA}$). Therefore, a voltage as low as 20 to 25 V can be used to move charges across the thin barrier in either direction for programming or erasing. EEPROM allows selective erasing at the register level rather than erasing all the information

since the information can be changed by using electrical signals. The EEPROM memory also has a special chip erase mode by which entire chip can be erased in 10 ms. This time is quite small as compared to time required to erase EPROM and it can be erased and reprogrammed with device right in the circuit. However, EEPROMs are most expensive and the least dense ROMs.

7.5.4 EAPROM

- EAPROM is an acronym for Electrically Alterable Programmable Read - Only Memory. It is a non-volatile read only memory. It is a form of PROM in which the contents of selected memory locations can be changed by applying suitable electrical signals without removing the EAPROM from the printed circuit board.

Advantages of EAPROM

- We can selectively program or can selectively erase EAPROM.
- Erasing time is 5 to 10 ms and programming time is 250 μ s to 1 ms for a particular location. This time is quite low.

Disadvantages of EAPROM

- It is expensive.
- It is not available from a variety of source.
- It is not popular as this technology is still not matured.

Review Questions

1. Write note on ROM technologies.
2. Give the features of a ROM cell.
3. Briefly explain any four nonvolatile memory in detail.
4. Write a note on ROM.
5. Explain EPROM.
6. Write a note on EEPROM.
7. Mention the two types of erasable PROM.
8. How is individual location in a EEPROM programmed or erased?
9. Elaborate the single fused PROM cell with clear sketch.
10. Write the advantages of EPROM over PROM.
11. Whether ROM is classified as nonvolatile storage device? Why?
12. Write a note on types of ROMs.
13. Explain the various ROM organizations and give the uses for each type.
14. Write a note on EEPROM.
15. Briefly explain the EPROM and EEPROM technology.
16. Write short note on EAPROM.

17. Define the followings : EPROM

18. List down the various types of ROMs and discuss any two of them.

GTU : Winter-14, Mark 1

GTU : Winter-14, 18, Marks 4

7.6 Read and Write Memory (RAM)

There are two types of RAMs :

- Static RAM
- Dynamic RAM

GTU : Winter-14

7.6.1 Static RAM (SRAM)

- Memories that consists of circuits capable of retaining their state as long as power is applied are known as static memories. These are random access memory (RAM) and hence combinably called static RAM memories.

7.6.1.1 Static RAM Cell

- The Fig. 7.6.1 shows the implementation of static RAM cell. It consists of two cross-coupled inverters as a latch and two transistors T_1 and T_2 which act as a switches.

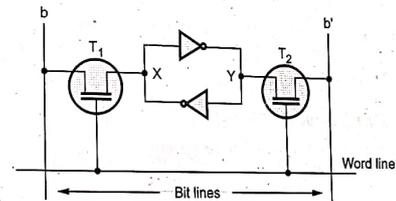


Fig. 7.6.1 Static RAM Cell

- The latch is connected to two bit lines by transistors T_1 and T_2 . The word line controls the opening and closing of transistors T_1 and T_2 . When word line is at logic 0 level (Ground level), the transistors are off and the latch retains its state.

Read operation

- For read operation, word line is made logic 1 (high) so that both transistors are ON. Now if the cell is in state 1, the signal on bit line b is high and the signal on bit line b' is low. The opposite is true if the cell is in state 0. The b and b' are complements of each other. The sense/write circuits connected to the bit lines monitor the states of b and b' and set the output accordingly.

Write operation

For write operation, the state to be set is placed on the line b and its complement is placed on line b' and then the word line is activated. This action forces the cell into the corresponding state and write operation is completed.

7.6.2 Dynamic RAM (DRAM)

7.6.2.1 Dynamic RAM Cell

Dynamic RAM stores the data as a charge on the capacitor. Fig. 7.6.2 shows the dynamic RAM cell. A dynamic RAM contains thousands of such memory cells. When COLUMN (Sense) and ROW (Control) lines go high, the MOSFET conducts and charges the capacitor. When the COLUMN and ROW lines go low, the MOSFET opens and the capacitor retains its charge. In this way, it stores 1 bit. Since only a single MOSFET and capacitor are needed, the dynamic RAM contains more memory cells as compared to static RAM per unit area.

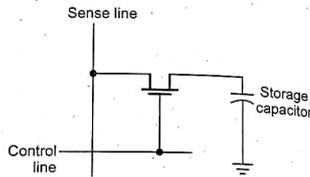


Fig. 7.6.2 Dynamic RAM

The disadvantage of dynamic RAM is that it needs refreshing of charge on the capacitor after every few milliseconds. This complicates the system design, since it requires the extra hardware to control refreshing of dynamic RAMs.

7.6.2.2 Comparison between SRAM and DRAM

Sr. No.	Static RAM	Dynamic RAM
1.	Static RAM contains less memory cells per unit area.	Dynamic RAM contains more memory cells as compared to static RAM per unit area.
2.	It has less access time hence faster memories.	Its access time is greater than static RAMs.
3.	Static RAM consists of number of flip-flops. Each flip-flop stores one bit.	Dynamic RAM stores the data as a charge on the capacitor. It consists of MOSFET and the capacitor for each cell.
4.	Refreshing circuitry is not required.	Refreshing circuitry is required to maintain the charge on the capacitors after every few milliseconds. Extra hardware is required to control refreshing. This makes system design complicated.
5.	Cost is more.	Cost is less.

7.6.3 Comparison between RAM and ROM

Parameter	RAM	ROM
Definition	It is a read / write memory.	It is a read only memory.
Volatility	It is a volatile memory, its contents are lost when the power is turned off.	It is a non-volatile memory; its contents are retained even after the power is switched off.
Types	The two main types of RAM are static RAM and dynamic RAM.	The types of ROM include PROM, EPROM and EEPROM.
Speed	Ram chips can read data faster than ROM.	Data retrieve speed is slower than RAM chips.
Use	RAM allows the computer to read data quickly to run applications. It also allows to store temporary data and intermediate results.	Since it is a read only memory it is used to store program / code and constants. In computers, it is used to store program necessary to boot the computer.

Review Questions

1. Draw a RAM cell and explain its working.
2. Draw the basic dynamic memory cell.
3. Write a note on dynamic RAM cell.
4. What is RAM ?
5. Compare static RAMs and dynamic RAMs.
6. What are the advantages of static RAM compared to dynamic RAM ?
7. Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle.
8. Compare RAM and ROM.

GTU - Winter-14, Marks 7

7.7 Memory Organization

- Memory cells are organized in the form of an array, in which each cell is capable of storing one bit of information. Let us see the organization of memory chip using single decoder and using two dimensional decoding.

Organization using single decoder

- The Fig. 7.7.1 shows the organization of 16 x 8 (16 words of 8-bit each) memory. Here, the organization is shown with detail connections of address lines, data lines. The data input and the data output of each sense/write circuit are connected to a single bidirectional data line that can be connected to the data

bus of a computer. Two control lines, R/\overline{W} and \overline{CS} , are provided in addition to address and data lines. The R/\overline{W} (Read/Write) input specifies the required operation and the \overline{CS} input selects a given chip in a multi chip memory system.

- As shown in the Fig. 7.7.1 there are 16 words of 8-bits each. A memory with 16 words needs four address lines. The four address inputs go through a 4×16 decoder to select one of the sixteen words. The decoder is enabled with a memory enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory select at 1, one of the sixteen words is selected, dictated by the value in the four address lines. Once a word has been selected, the read/write input determines the operation. During write operation, the data available in the input lines are transferred into the eight memory cells of the selected word. The memory cells that are not selected are disabled and their previous binary values remain unchanged.

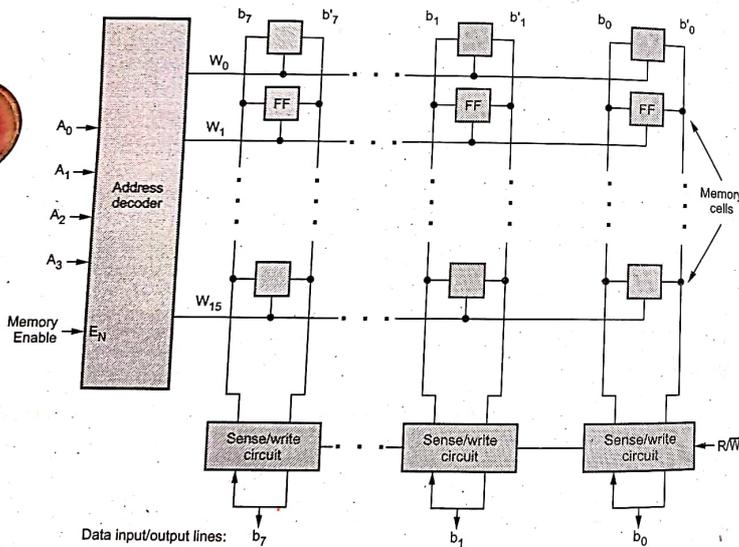


Fig. 7.7.1 Organization of bit calls in a memory chip

Organization using Two dimensional decoding

- A decoder with k inputs and $2k$ outputs requires $2k$ AND gates with k inputs per gate. We can reduce the total number of gates and the number of inputs per gate by employing two decoders in a two-dimensional selection scheme. The Fig. 7.7.2 shows the two dimensional decoding scheme. Here, two $k/2$ input decoders are used instead of one k -input decoder. One decoder performs the row selection and the other the column selection in a two dimensional matrix configuration.

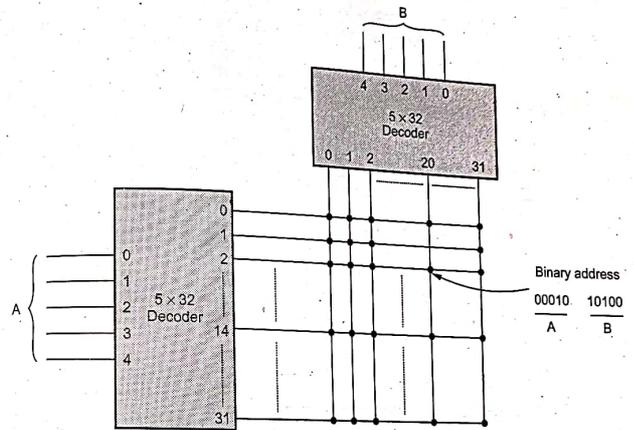


Fig. 7.7.2 Two dimensional decoding scheme

- The two-dimensional selection pattern shown in Fig. 7.7.2 has $k = 10$, i.e. 10 decoder inputs. These decoder inputs are divided by 2 to get individual decoder inputs, i.e. 5 input for each decoder. Therefore, here instead of using a single 10×1024 decoder, we use two 5×32 decoders. With a single decoder we would need 1024 AND gates with 10 inputs in each. In the two - decoder case, we need 64 AND gates with five inputs in each. The five most significant bits of the address go to input A and the five least significant bits go to input B. Each word within the memory array is selected by the coincidence of one A and one B line. Thus, the memory array is selected by the coincidence between 1 of 32 rows and 1 of 32 columns for a total of 1024 words.

Review Question

1. Write a note on memory organization.

7.8 Expanding Memory Size

- It is possible to expand word size of memory by connecting two or more ICs together. The word size of memory IC can be increased by connecting two memory ICs in such a way that their data bus is in series and address bus in parallel. Both memory ICs are selected simultaneously by common chip select signal to access entire expanded word at a time. The example 7.8.1 illustrates method of word expansion.

Example 7.8.1 Design 1 K × 8 RAM using two 2114 ICs.

Solution :

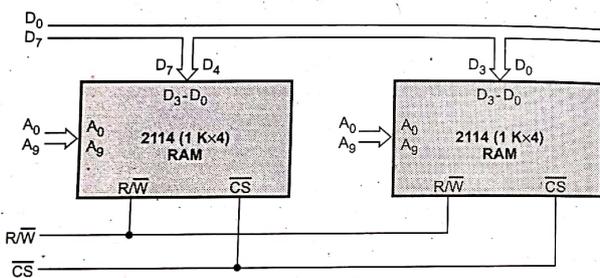


Fig. 7.8.1 Expanding word size

- The memory capacity can be increased by connecting two or more memory ICs in parallel. This means that the address, data and control lines are connected in parallel to all memory ICs. Each IC is selected by the separate chip select signal generated by the address decoder. This is illustrated by the following example.

Memory Map

A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Memory address
0	0	0	0	0	0	0	0	0	0	Starting address
1	1	1	1	1	1	1	1	1	1	End address

Example 7.8.2 Design 2 K × 4 RAM using two 2114 ICs.

Solution :

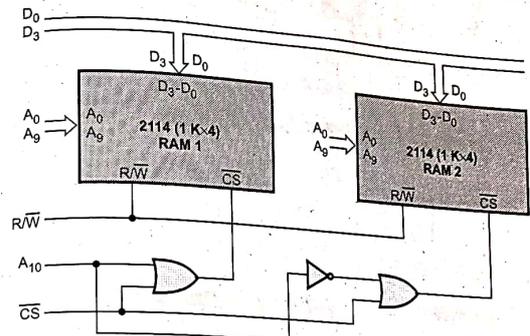


Fig. 7.8.2

Memory Map

A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Memory ICs
0	0	0	0	0	0	0	0	0	0	0	RAM1
0	1	1	1	1	1	1	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	RAM2
1	1	1	1	1	1	1	1	1	1	1	

Example 7.8.3 Implementation of 2M words of 32-bit each using 512 K × 8 static memory chips.

Solution : The Fig. 7.8.3 shows the implementation of 2 M words of 32-bit each using 512 K × 8 static memory chip. In this implementation, we have expand word size as well as capacity of the memory. Since each memory chip has byte organization, we have to use 4 chips in each row to get the word size of 32 bits (8 × 4). Similarly, to increase memory capacity up to 2 M we have to use 4 memory chips of capacity 512 K in each column.

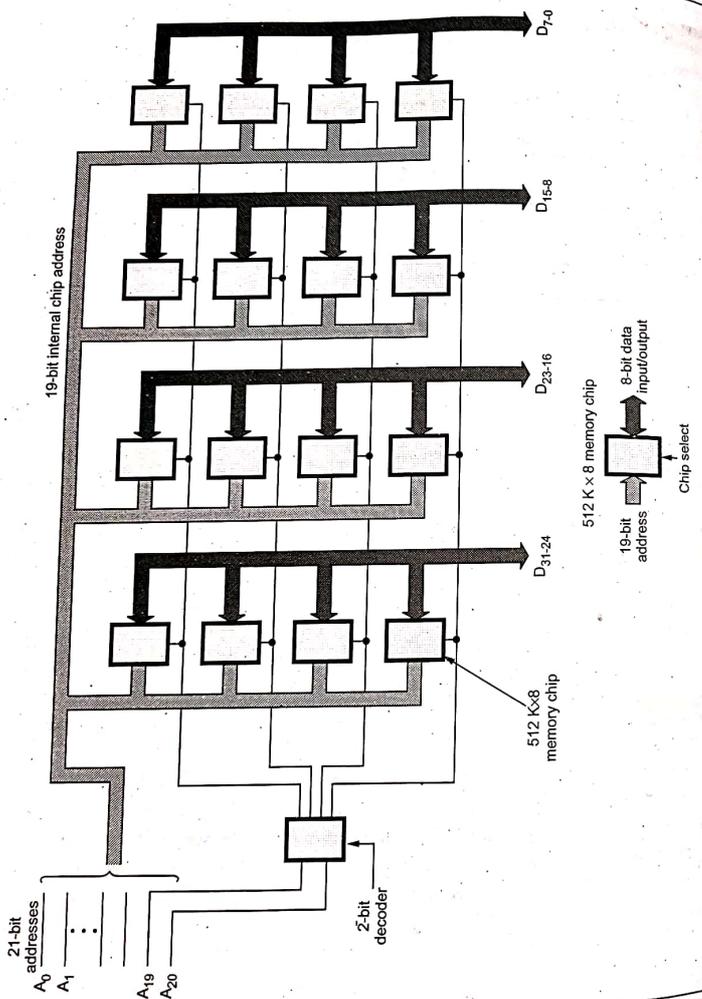


Fig. 7.8.3

Example 7.8.4 For a 32 K memory, obtain memory map to interface memory to 16-bit processor.

Solution :

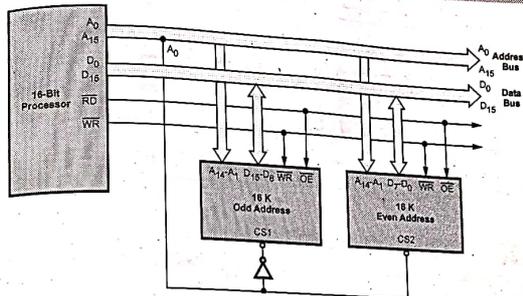


Fig. 7.8.4

Memory Map :

Memory	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Address
Even Address	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
Odd Address	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	7FFEH
Even Address	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H
Odd Address	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7FFEH

Note A₁₅ is considered logic 0.

Example 7.8.5 How many 128 × 8 memory chips are needed to provide a memory capacity of 4096 × 16.

$$\text{Solution : Number of chips required} = \frac{\text{Required RAM size}}{\text{Available chip capacity}} = \frac{4096 \times 16}{128 \times 8} = 64$$

Hence, 64 chips of 128 × 8 size are needed to provide a memory capacity of 4096 × 16.

Example 7.8.6 Given a 32 × 8 size ROM chip with an enable input. Show the external connections necessary to construct a 128 × 8 ROM with four chips and decoder.

$$\text{Solution : Address bus width} = \log_2 128 = \log_2 2^7 = 7\text{-bits} = A_6 - A_0$$

$$\text{Data bus width} = 8\text{-bits} = D_7 - D_0$$

$$\text{Address lines required for } 32 \times 8 \text{ ROM} = \log_2 3^2 = \log_2 2^5 = 5 \text{ bits} = A_4 - A_0$$

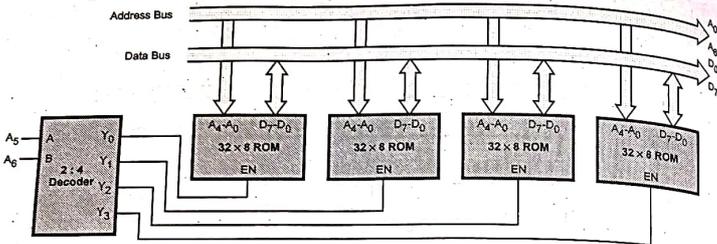


Fig. 7.8.5

Example 7.8.7 A microprocessor uses RAM chips of 1024×1 capacity.

- i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
- ii) How many chips are needed to provide a memory capacity of 16 kbytes? Explain in words how the chips are to be connected to the address bus.

Solution : i) Eight chips are needed with address lines connected in parallel as shown in the Fig. 7.8.6.

ii)
$$\text{Number of chips needed} = \frac{\text{Required memory capacity}}{\text{Chip size}}$$

$$= \frac{16 \text{ K} \times 8}{1 \text{ K} \times 1} = 128 \text{ chips}$$

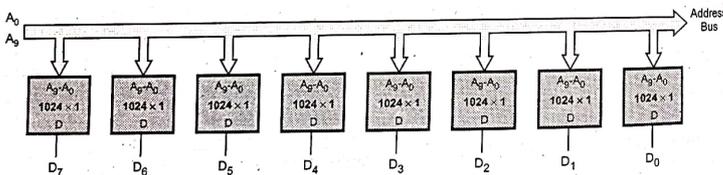


Fig. 7.8.6

- The address lines $A_9 - A_0$ from the address bus are connected in parallel to all the chips. In all there are 128 chips. These 128 chips are divided into 16 groups consists of 8 chips in each group. The address lines $A_{13} - A_{10}$ are decoded to generate 16 chip select signals one for each group so that at a time all chips from one group will be selected when corresponding chip select signal is activated.

Review Questions

1. Explain how to expand memory word size with the help of example.
2. Explain how to expand memory capacity with the help of example.

7.9 Content Addressable Memory (CAM)

- Many data-processing applications require the search of items in a table stored in or numbered object within a memory space. For example, an account number may be searched in a file to determine the holder's name and account status. To search an object, the number of accesses to memory depends on the location of the object and the efficiency of the search algorithm.
- The time required to find an object stored in memory can be reduced considerably if objects are selected based on their contents, not on their locations. A memory unit accessed by the content is called an associative memory or Content Addressable Memory (CAM). This type of memory is accessed simultaneously and in parallel on the basis of data content rather than by specific address or location.

7.9.1 Hardware Organization

- The Fig. 7.9.1 shows the block diagram of an associative memory. It consists of memory array with match logic for m n -bit words and associated registers. The argument register (A) and key register (K) each have n -bits per word. Each word in memory is compared in parallel with the contents of the argument register. The

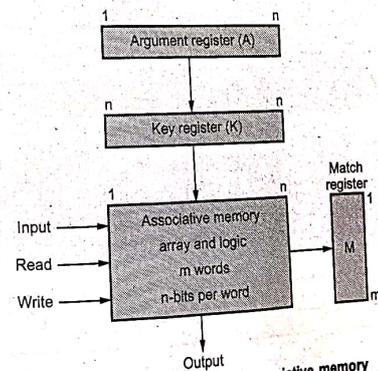


Fig. 7.9.1 Block diagram of associative memory

words that match with the word stored in the argument register set a corresponding bits in the match register. Therefore, reading can be accomplished by a sequential access to memory for those words whose corresponding bits in the match register have been set.

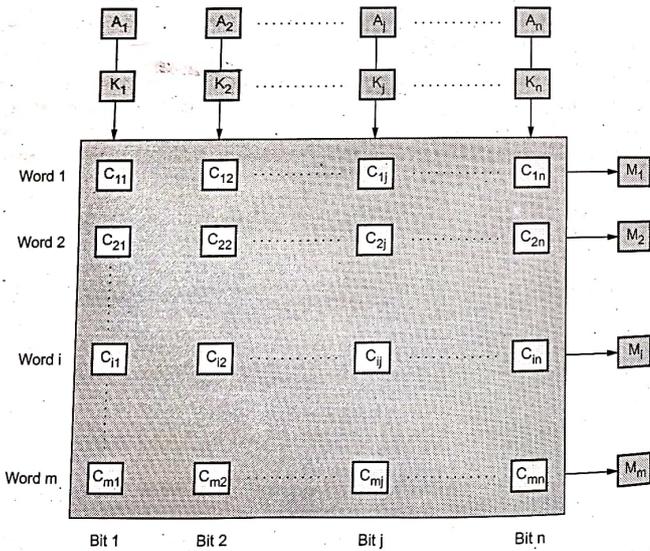
- The key register provides a mask for choosing a particular field or bits in the argument word. Only those bits in the argument register having 1's in their corresponding position of the key register are compared. For example, if argument register A and the key register K have the bit configuration shown below. Only the three rightmost bits of A are compared with memory words because K has 1's in these positions.

A 1 1 0 1 1 0 1 0
 K 0 0 0 0 0 1 1 1

Word 1 0 1 0 1 0 0 1 0 match

Word 2 1 1 0 1 1 1 0 0 no match

- The Fig. 7.9.2 shows the associated memory with cells of each register. The cells in the memory array are marked by the letter C with two subscripts. The first subscript gives the word number and the second subscript gives the bit position in the word.



7.9.2 Associated memory showing cells of each register

- The Fig. 7.9.3 shows the internal organization of a typical cell. It consists of RS flip-flop as a storage element and the circuit for reading, writing and matching into the storage cell. To carry-out read operation read signal is made logic 1. The match logic compares the bit in the storage cell with the corresponding unmasked corresponding bit in the match register.

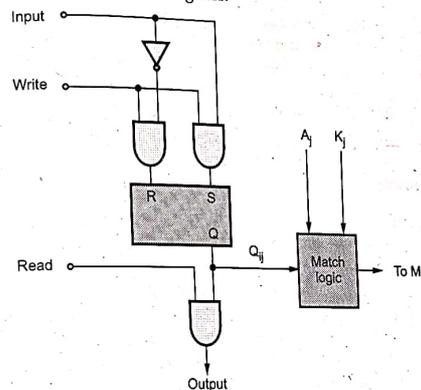


Fig. 7.9.3 Internal organization of typical cell of associative memory

- The Fig. 7.9.4 shows the match logic for each word. The cell bit (Q_{ij}) is compared with the corresponding argument bit with EX-NOR gate. EX-NOR gate gives output logic 1 only when its inputs are same. The output of EX-NOR gate is valid only when the corresponding bit in key register is logic 1. This condition is

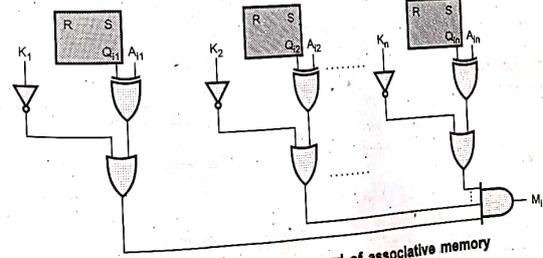


Fig. 7.9.4 Match logic for one word of associative memory

implemented using 2-input OR gate. When corresponding bit in key register is logic 1, the inverter gives output 0 which forces the output of OR gate to follow the second input, i.e. the comparison output; otherwise output of OR-gate is logic 1. The outputs of all OR-gates are then ANDed with n-input AND gate to check whether all bits in the word are matched with the bits in the argument register.

7.9.2 Read Operation

- In the read operation, all matched words are read in sequence by applying a read signal to each word line whose corresponding M_i bit is a logic 1. In applications where no two identical items are stored in the memory, only one word may match the unmasked argument field. In such case, we can use M_i output directly as a read signal for the corresponding word. The contents of the matched word will be presented automatically at the output lines and no special read signal is needed.

7.9.3 Write Operation

- In write operation, we consider two separate cases : 1. It is necessary to load entire memory with new information 2. It is necessary to replace one word with new information. The entire memory can be loaded with new information by addressing each location in sequence. This will make the memory device a random access memory for writing and a content addressable memory for reading. Here, the address for the input can be decoded as in a random access memory. Thus instead of having m address lines, one for each word, the number of address lines can be reduced by the use of decoder to d lines, where $m = 2^d$.
- To implement the write operation in the second case the tag register is used. This register has as many bits as there are words in the memory for every active (valid) word stored in the memory, the corresponding bit in the tag register is set to 1. When word is deleted from the memory the corresponding tag bit is cleared, i.e. it is set to logic 0. The word is then stored in the memory by scanning the tag register until the first 0 bit is encountered. This gives the first available inactive word and a position for writing a new word. After the new word is stored in the memory it is made active by setting the corresponding tag bit in the tag register.

Review Questions

- Write a short note on associative memory.
- Describe by means of block diagram how multiple matched words can be read out from an associative memory.
- What is CAM ? Explain it with block diagram.
- Explain associative memory with its hardware organization. Explain how the data is read and write in the associative memory.

7.10 Charge - Coupled Devices (CCD) Memory

- Charge - coupled device (CCD) memory is a type of dynamic memory in which packets of charge are continuously transferred from one MOS device to another. The structure of a MOS charge-coupled device is quite simple, as shown in the Fig. 7.10.1 . It consists simply of a P substrate, an insulating oxide layer, and isolated gates

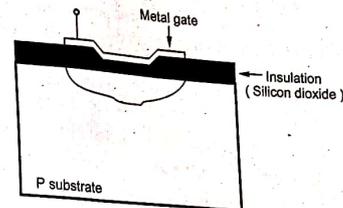


Fig. 7.10.1 MOS charge-coupled device structure

- When a high voltage is applied to the metal gate, holes are repelled from a region beneath the gate in the P-type substrate. This region, called a potential well, is then capable of accepting a packet of negative charged electrons. Therefore, data is stored in a CCD as charge, and it is transferred from one device to an adjacent one by clocking their gates.
- The charge-coupled devices are built as a serial-in, serial-out MOS shift registers, each shift register being a line of charge-coupled devices. By controlling the timing of the clock signals applied to the shift registers, data can be accessed one bit at a time from a single register or several bits at a time from multiple registers.
- The main advantage of CCD is that its simple cell structure. It makes it possible to construct large-capacity memories at low cost. Since CCDs are dynamic in nature, they must be periodically refreshed, and must be driven by rather complex, multi phase clock signals. Another disadvantage of CCDs is due to serial data storage. Serial data storage has a longer access times in comparison to semiconductor RAM memory. It is on the order of 100 μ s.
- CCDs can be used for digital or analog delay, and as serial data memories. Another exciting application of CCDs is as the light sensitive image sensor in television cameras.

Review Question

- Write a note on charged coupled device memories.

7.11 Programmable Logic Devices

- Various digital ICs for performing basic digital operations and other functions, such as adders, comparators, arithmetic logic unit, multiplexers, demultiplexers, code converters, shift registers, counters etc. are known as **fixed function ICs** due to their fix function.
- These ICs are designed by their manufacturers and produced in large quantities to satisfy the needs of a wide variety of applic.
- We have seen the design of digital circuits using fixed function ICs.
- There are two more approaches for the design of digital circuits.
 - Use of Application Specific Integrated Circuits (ASICs)
 - Use of Programmable Logic Devices (PLDs)
- In the fixed function IC approach, we have to use various fixed function ICs to implement different functional blocks in the digital circuit.
- In ASIC, a single IC is designed and manufactured to implement the entire circuit.
- In the third approach programmable logic devices are used to implement logic functions. The main advantage of PLD approach is that PLDs can be easily configurable by the individual user for specific applications.
- The Table 7.11.1 shows the comparison between these three design approaches.

Comparison parameter	Fixed-function IC approach	ASIC approach	PLD approach
Development cost	Low	High	Low
Space required	Large	Minimum	Less
Power required	Large	Less	Less
Reliability	Less compared to other two approaches.	Highest	High
Circuit testing	Easy	Specialized testing methods are required which may increase cost and effort.	Easy
Design flexibility	Less	No	More
Modification in design	Possible with change in circuit and/or with change in components.	No	May be possible without any circuit or component changes but only by reconfiguring the device.
Design security	Lack of security i.e. circuit can easily be copied by others.	High	High
Design time	Less	More	Less

Table 7.11.1 Comparison between design approaches

- PLDs can be reprogrammed in few seconds and hence give more flexibility to experiment with designs. Reprogramming feature of PLDs also make it possible to accept changes/modifications in the previously design circuits. These two main advantages and others discussed in Table 7.11.1 make PLDs very popular in digital design.
- According to architecture, complexity and flexibility in programming PLDs are classified as
 1. PROMs : Programmable Read Only Memories
 2. PLAs : Programmable Logic Arrays
 3. PAL : Programmable Array Logic
 4. FPGAs : Field Programmable Gate Arrays
 5. CPLDs : Complex Programmable Logic Devices

7.12 ROM / PROM as a PLD

GTU : Winter-15, 18, Summer-18

- ROM stands for Read Only Memory and PROM stands for Programmable Read Only Memory. The only difference in ROM and PROM is that ROM is programmed by manufacturer while PROM is user programmable.
- Fig. 7.12.1 shows the block diagram of PROM.
- It consists of n-input lines and m-output lines.
- Each bit combination of the input variables is called an **address**.
- Each bit combination that comes out of the output lines is called a **word**.
- The number of bits per word is equal to the number of output lines, m.
- The address specified in binary number denotes one of the minterms of n variables.
- The number of distinct addresses possible with n-input variables is 2^n .
- An output word can be selected by a unique address and since there are 2^n distinct addresses in PROM, there are 2^n distinct words in the PROM.
- The word available on the output lines at any given time depends on the address value applied to the input lines.
- Let us consider 64×4 PROM.
- The PROM consists of 64 words of 4-bits each. This means that there are four output lines and particular word from 64 words presently available on the output lines is determined from the six input lines.

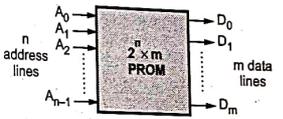


Fig. 7.12.1

- There are only six inputs in a 64×4 PROM because $2^6 = 64$ and with six variables, we can specify 64 addresses or minterms. For each address input, there is a unique selected word. Thus, if the input address is 000000, word number 0 is selected and applied to the output lines. If the input address is 111111, word number 63 is selected and applied to the output lines.
- The Fig. 7.12.2 shows the internal logic construction of a 64×4 PROM. The six input variables are decoded in 64 lines by means of 64 AND gates and 6 inverters.

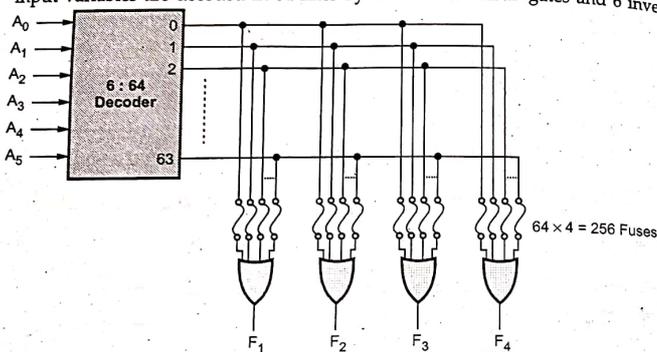


Fig. 7.12.2 Logic construction of 64×4 PROM

- Each output of the decoder represents one of the minterms of a function of six variables.
- The 64 outputs of the decoder are connected through fuses to each OR gate.
- Only four of these fuses are shown in the diagram, but actually each

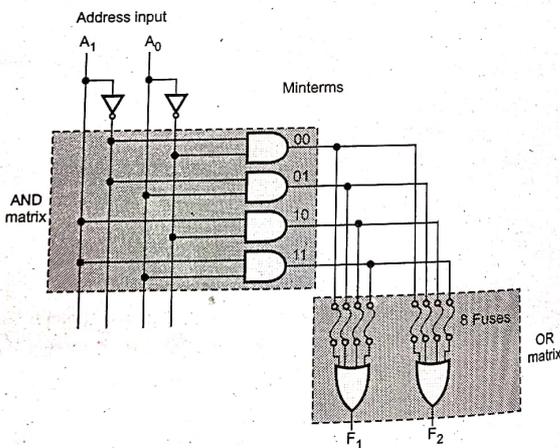


Fig. 7.12.3 (a) 4×2 PROM with AND-OR gates

OR gate has 64 inputs and each input goes through a fuse that can be blown as desired.

- The PROM is a two level implementation in sum of minterms form. Let us see AND-OR and AND-OR-INVERTER implementation of PROM. Fig. 7.12.3 shows the 4×2 PROM with AND-OR and AND-OR-INVERTER implementations.

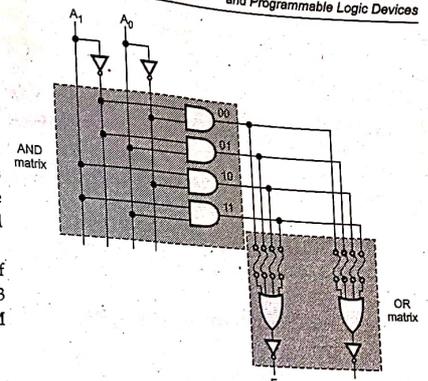


Fig. 7.12.3 (b) 4×2 PROM with AND-OR-INVERTER gates

7.12.1 AND Matrix

- Fig. 7.12.4 shows the AND matrix. It is used to form product terms. It has m AND gates with $2n$ -inputs and m -outputs, one for each AND gate.

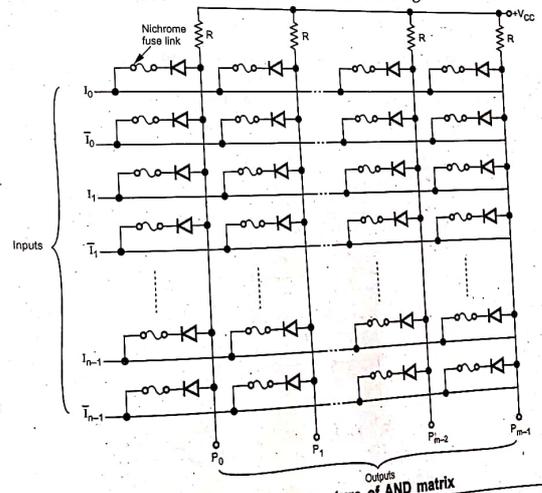


Fig. 7.12.4 Internal structure of AND matrix

- Fig. 7.12.4 shows the AND gates formed by diodes and resistors structure. Each AND gate has all the input variables in complemented and uncomplemented form.
- There is a nichrome fuse link in series with each diode which can be burn out to disconnect particular input for that AND gate. Before programming, all fuse links are intact and the product term for each AND gate is given by

$$P = I_0 \cdot \bar{I}_0 \cdot I_1 \cdot \bar{I}_1 \dots I_{n-1} \cdot \bar{I}_{n-1}$$

- Fig. 7.12.5 shows the simplified and equivalent representation of input connections for one AND gate.
- The array logic symbol shown in Fig. 7.12.5 (b) uses a single horizontal line connected to the gate input and multiple vertical lines to indicate the individual inputs.
- Each intersection between horizontal line and vertical line indicates the fuse connection.

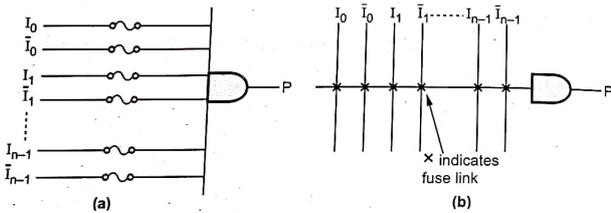


Fig. 7.12.5 Equivalent representation of AND gate

- Fig. 7.12.6 shows the simplified representation of AND matrix with input buffer.

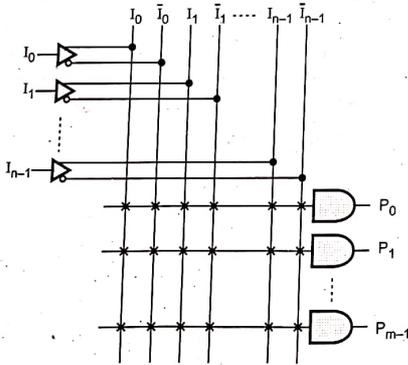


Fig. 7.12.6 Simplified representation of AND matrix with input buffer

7.12.2 OR Matrix

- OR matrix is provided to produce the logical sum of the product term outputs of the AND matrix.
- Fig. 7.12.7 shows the OR gates formed by diodes and resistors structure.

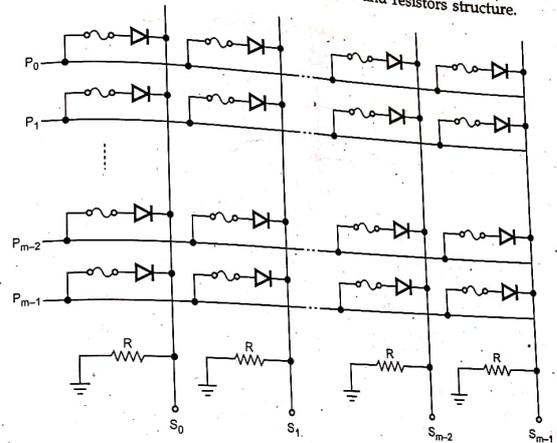


Fig. 7.12.7

- Each OR gate has all the product terms as input variables.
- There is a nichrome fuse link in series with each diode which can be burn out to disconnect particular product term for that OR gate.
- Before programming, all fuse link in OR matrix are also intact and the sum term for each OR gate is given by,

$$S = P_0 + P_1 + \dots + P_{m-2} + P_{m-1}$$

- Fig. 7.12.8 shows the simplified and equivalent representation of input connections for one OR gate.
- Fig. 7.12.9 shows the simplified representation of OR matrix.

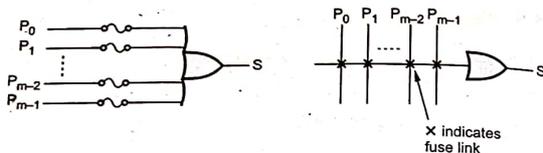


Fig. 7.12.8 Equivalent representation of OR gate

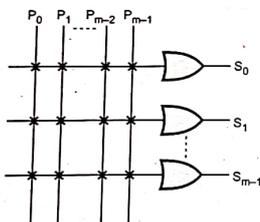


Fig. 7.12.9 Simplified representation of OR matrix

7.12.3 Invert / Non-invert Matrix

- Invert/Non-invert matrix provides output in the complement or uncomplemented form.
- The user can program the output in either complement or uncomplement form as per design requirements.

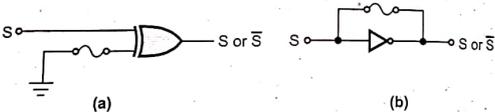


Fig. 7.12.10 Inverting and non-inverting circuits

- The typical circuits for invert/non-invert matrix is as shown in Fig. 7.12.10. In both the cases if fuse is intact the output is in its uncomplemented form; otherwise output is in the complemented form.

7.12.4 Combinational Logic Implementation using PROM

- Looking at the logic diagram of the PROM, we can realize that each output provides the sum of all the minterms of n-input variables.
- Any Boolean function can be expressed in sum of minterms form.
- By breaking the links of those minterms not included in the function, each PROM output can be made to represent the Boolean function of one of the output variables in the combinational circuit.
- For an n-input, m-output combinational circuit, we need a $2^n \times m$ PROM.

Illustrative Examples

Example 7.12.1 Using PROM realize the following expressions.

$$F_1(a, b, c) = \sum m(0, 1, 3, 5, 7)$$

$$F_2(a, b, c) = \sum m(1, 2, 5, 6)$$

Solution : The given functions have three inputs. They generate $2^3 = 8$ minterms and since there are two functions, there are two outputs. The functions can be realized as shown in Fig. 7.12.11.

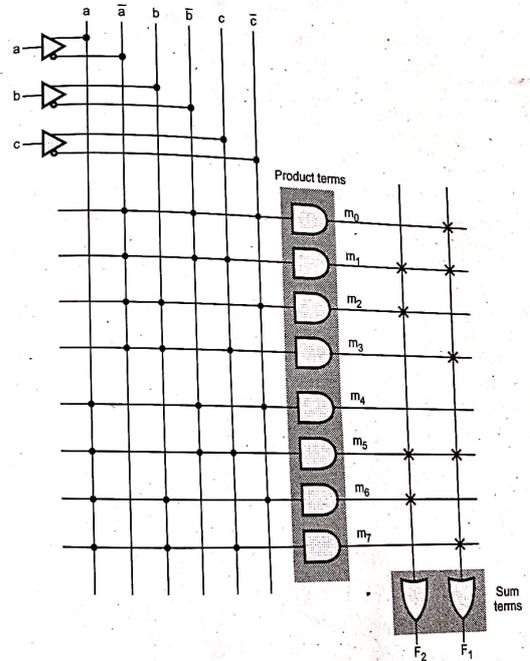
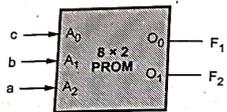


Fig. 7.12.11

- The Fig. 7.12.12 shows the block diagram and truth table of PROM.



(a) Block diagram

A ₂	A ₁	A ₀	F ₂	F ₁
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

(b) PROM truth table

Fig. 7.12.12

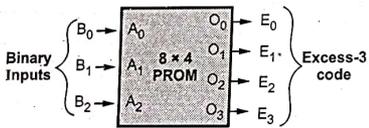
Example 7.12.2 Design a combinational circuit using a PROM. The circuit accepts 3-bit binary number and generates its equivalent Excess-3 code.

Solution : Let us derive the truth table for the given combination circuit. Table 7.12.1 shows the truth table.

Inputs			Outputs			
B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	0	1	0	1

Table 7.12.1 Truth table for 3-bit binary to excess-3 converter

In practice when we are designing combinational circuits with PROM, it is not necessary to show the internal gate connections of fuses inside the unit, as shown in the Fig. 7.12.13. (Refer Fig. 7.12.13 on next page). This was shown for demonstration purpose only. The designer has to only specify the PROM (inputs and outputs) and its truth table, as shown in the Fig. 7.12.14.



(a) Block diagram

A ₂	A ₁	A ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

(b) PROM truth table

Fig. 7.12.14

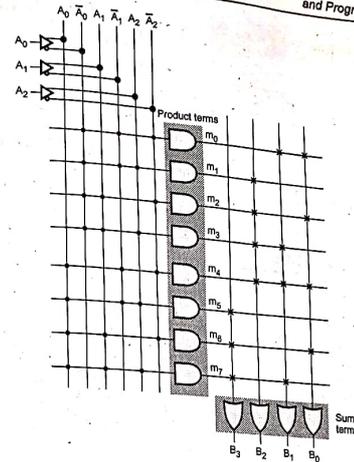
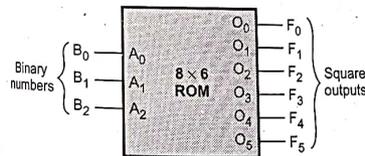


Fig. 7.12.13

Example 7.12.3 Design a combinational circuit using ROM. The circuit accepts 3-bit number and generates an output binary number equal to square of input number.

Solution :



(a) Block diagram

Binary input on address lines			Square of number on data lines					
B ₂	B ₁	B ₀	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

(b) ROM truth table

Fig. 7.12.15

Example 7.12.4 Implement binary to excess 3 code converter using ROM.

Solution :

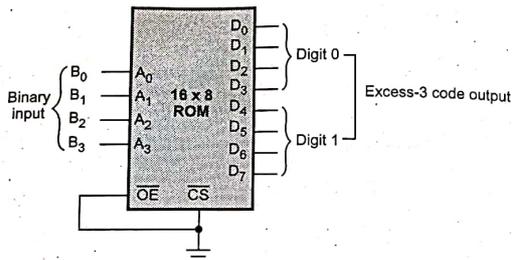


Fig. 7.12.16

Address				Memory contents							
A ₃	A ₂	A ₁	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	1	0	0	1	1	0	1	0	0
0	0	1	0	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	1	0
0	1	0	0	0	0	1	1	0	1	1	1
0	1	0	1	0	0	1	1	1	0	0	0
0	1	1	0	0	0	1	1	1	0	0	1
0	1	1	1	0	0	1	1	1	0	1	0
1	0	0	0	0	0	1	1	1	0	1	1
1	0	0	1	0	0	1	1	1	1	0	0
1	0	1	0	0	1	0	0	0	0	1	1
1	0	1	1	0	1	0	0	0	1	0	0
1	1	0	0	0	1	0	0	0	1	0	1
1	1	0	1	0	1	0	0	0	1	1	0
1	1	1	0	0	1	0	0	0	1	1	1
1	1	1	1	0	1	0	0	1	0	0	0

Table 7.12.2 ROM contents

Example 7.12.5 Implement following functions using ROM.

$$F_1 = \sum m(1, 3, 4, 6), F_2 = \sum m(2, 4, 5, 7), F_3 = \sum m(0, 1, 5, 7), F_4 = \sum m(1, 2, 3, 4).$$

GTU - Winter-15, Marks 7

Solution :

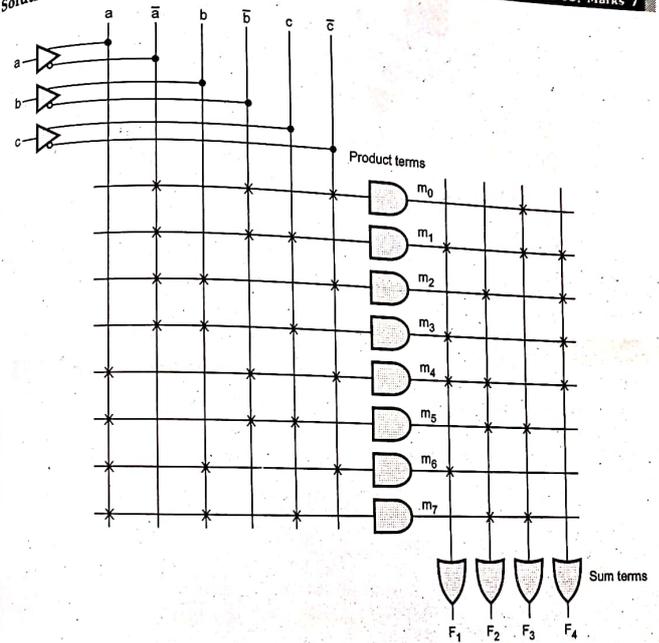


Fig. 7.12.17

Example 7.12.6 Using 8x4 ROM, realize the expression $F_1 = AB'C + ABC' + A'BC$, $F_2 = A'B'C' + A'BC' + AB'C'$, $F_3 = A'B'C' + ABC$. Show the contents of all locations.

GTU - Summer-18, Marks 7

Solution :

$$F_1 = A\bar{B}C + AB\bar{C} + \bar{A}BC = \sum m(5, 6, 3)$$

$$F_2 = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} = \sum m(1, 2, 4)$$

$$F_3 = \bar{A}\bar{B}\bar{C} + ABC = \sum m(0, 7)$$

Location			4 - Memory contents			
Address			D ₃	D ₂	D ₁	D ₀
A	B	C	(x)	(F ₃)	(F ₂)	(F ₁)
0	0	0	1	1	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	1	0	0	1
1	0	0	1	0	1	0
1	0	1	1	0	0	1
1	1	0	1	0	0	1
1	1	1	1	1	0	0
Unused						

Example 7.12.7 Design a 3-bit gray to binary code converter. Implement it using suitable PROM. Draw the necessary diagrams and tables.

GTU : Winter-18, Marks 3

Solution : Step 1 : Truth table for 3-bit Gray to binary code converter

	Gray Code			Binary Code		
	G ₂	G ₁	G ₀	B ₂	B ₁	B ₀
m ₀	0	0	0	0	0	0
m ₁	0	0	1	0	0	1
m ₃	0	1	1	0	1	0
m ₂	0	1	0	0	1	1
m ₅	1	1	0	1	0	0
m ₇	1	1	1	1	0	1
m ₆	1	0	1	1	1	0
m ₄	1	0	0	1	1	1

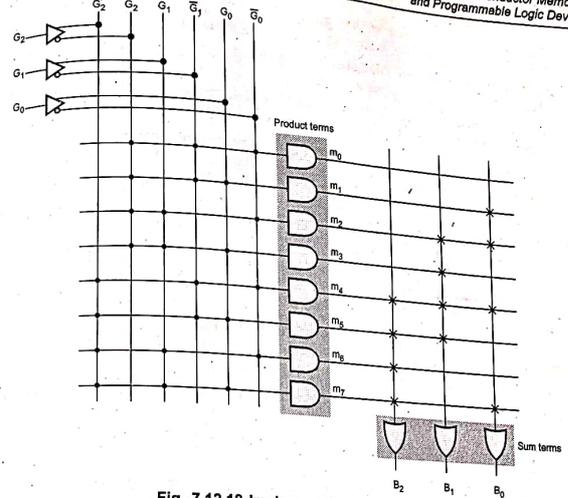


Fig. 7.12.18 Implementation using PROM

Examples for Practice

Example 7.12.8 : Design a switching circuit that converts a 4-bit binary code into a 4-bit Gray code using ROM array.

Example 7.12.9 : Design a PROM which will convert BCD numbers into Gray code.

7.13 Programmable Logic Array (PLA)

GTU : Dec.-12, May-13, Winter-16

- The combinational circuit do not use all the minterms every time. Occasionally, they have don't care conditions. Don't care condition when implemented with a PROM becomes an address input that will never occur. The result is that not all the bit patterns available in the PROM are used, which may be considered a waste of available equipment.
- For cases where the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a Programmable Logic Array (PLA).
- A PLA is similar to a PROM in concept; however it does not provide full decoding of the variables and does not generate all the minterms as in the PROM.

- The PLA replaces decoder by group of AND gates, each of which can be programmed to generate a product term of the input variables.
- In PLA, both AND and OR gates have fuses at the inputs, therefore in PLA both AND and OR gates are programmable.
- Fig. 7.13.1 shows the block diagram of PLA. It consists of n-inputs, output buffer with m outputs, m product terms, m sum terms, input and output buffers.

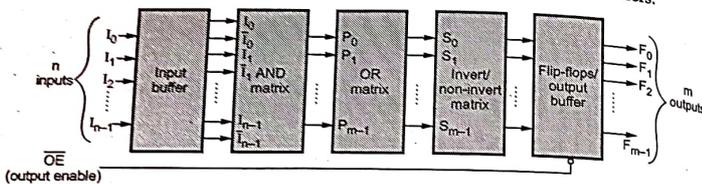


Fig. 7.13.1 Block diagram of a PLA

- The product terms constitute a group of m AND gates and the sum terms constitute a group of m OR gates, called OR matrix.
- Fuses are inserted between all n-inputs and their complement values to each of the AND gates.
- Fuses are also provided between the outputs of the AND gates and the inputs of the OR gates.
- The third set of fuses in the output inverters allows the output function to be generated either in the AND-OR form or in the AND-OR-INVERT form.
- When inverter is bypassed by link we get AND-OR implementation.
- To get AND-OR-INVERTER implementation inverter link has to be disconnected.

7.13.1 Input Buffer

- Input buffers are provided in the PLA to limit loading of the sources that drive the inputs.
- They also provide inverted and non-inverted form of inputs at its output.
- The Fig. 7.13.2 shows two ways of representing input buffer for single input.

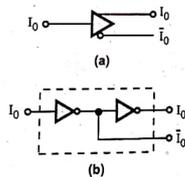


Fig. 7.13.2 Input buffer for single input line

7.13.2 Output Buffer

- The driving capacity of PLA is increased by providing buffers at the output. They are usually TTL compatible.
- The Fig. 7.13.3 shows the tri-state, TTL compatible output buffer.

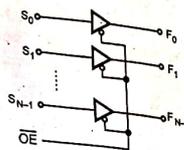


Fig. 7.13.3 Output buffers

- The output buffer may provide totem-pole, open collector or tri-state output.

7.13.3 Output through Flip-Flops

- For the implementation of sequential circuits we need memory elements, flip-flops and combinational circuitry for deriving the flip-flop inputs.
- To satisfy both the needs some PLAs are provided with flip-flop at each output, as shown in the Fig. 7.13.4.

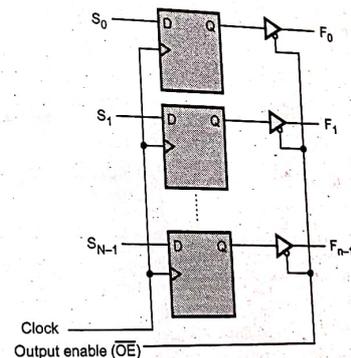


Fig. 7.13.4 PLA with flip-flop at the output

7.13.4 Implementation of Combination Logic Circuit using PLA

- Like ROM, PLA can be mask-programmable or field-programmable.
- With a mask-programmable PLA, the user must submit a PLA program table to the manufacturer. This table is used by the vendor to produce a user-made PLA that has the required internal paths between inputs and outputs.

- A second type of PLA available is called a field-programmable logic array or FPLA. The FPLA can be programmed by the user by means of certain recommended procedures. FPLAs can be programmed with commercially available programmer units.

Illustrative Examples

Example 7.13.1 A combinational circuit is defined by the functions :

$$F_1 = \sum m(3, 5, 7), F_2 = \sum m(4, 5, 7)$$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

Solution :

Step 1 : Simplify the given Boolean functions.

- The Boolean functions are simplified, as shown in the Fig. 7.13.5. The simplified functions in sum of products are obtained from the maps are :

$$F_1 = AC + BC, F_2 = A\bar{B} + AC$$

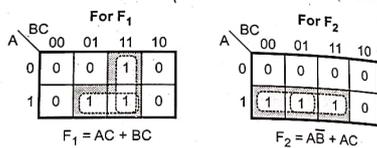


Fig. 7.13.5

Step 2 : Write PLA program table.

- Therefore, there are three distinct product terms : AC, BC and A \bar{B} , and two sum terms. The PLA program table shown in Table 7.13.1 consists of three columns specifying product terms, inputs and outputs. The first column gives the lists of product terms numerically.

Product term	Inputs			Outputs	
	A	B	C	F ₁	F ₂
AC	1	1	-	1	1
BC	2	-	1	1	-
A \bar{B}	3	1	0	-	1
	T	T		T/C	

Table 7.13.1 PLA program table

The second column specifies the required paths between inputs and AND gates. The third column specifies the required paths between the AND gates and the OR gates. Under each output variable, we write a T (for true) if the output inverter is to be bypassed, and C (for complement) if the function is to be complemented with the output inverter. The product terms listed on the left of first column are not the part of PLA program table they are included for reference only.

Step 3 : Implementation

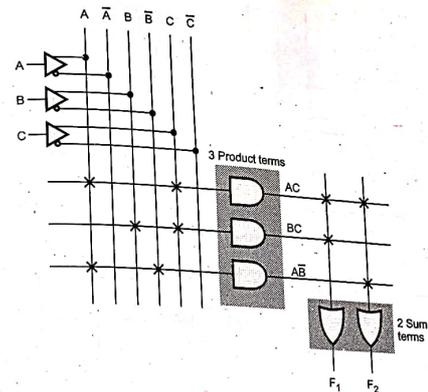


Fig. 7.13.6

Example 7.13.2 Draw a PLA circuit to implement the logic functions

$$\bar{A}BC + A\bar{B}C + AC\bar{C} + \bar{A}\bar{B}C + BC.$$

Solution :

Step 1 : Simplify the Boolean functions

$$\begin{aligned} \bar{A}BC + A\bar{B}C + AC\bar{C} &= \bar{A}BC + A(\bar{B}C + \bar{C}) \\ &= \bar{A}BC + A(\bar{B} + \bar{C}) \quad \because A + \bar{A}B = A + B \\ &= \bar{A}BC + A\bar{B} + AC \end{aligned}$$

Note The second Boolean function is in simplified form.

Step 2 : Implementation (see Fig. 7.13.7 on next page)

Example 7.13.3 Implement the following multiboolen function using 3 × 4 × 2 PLA PLD.

$$f_1(a_2, a_1, a_0) = \sum m(0, 1, 3, 5) \text{ and } f_2(a_2, a_1, a_0) = \sum m(3, 5, 7)$$

Solution :

Step 1 : Simplify the Boolean functions.

$$f_1 = \bar{a}_2 \bar{a}_1 + \bar{a}_2 a_0 + \bar{a}_1 a_0$$

$$f_2 = a_2 a_0 + a_1 a_0$$

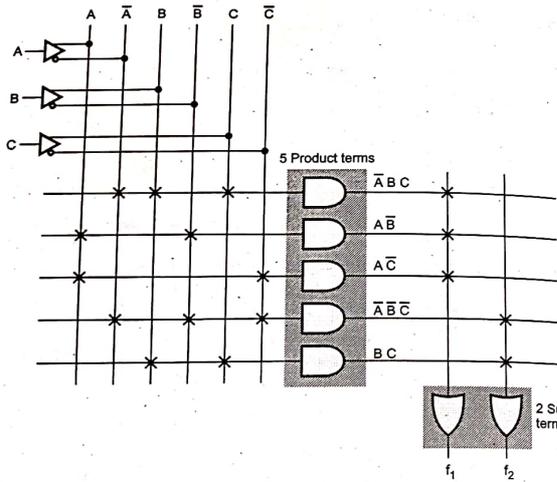


Fig. 7.13.7

To implement functions f_1 and f_2 we require $3 \times 5 \times 2$ PLA and we have to implement them using $3 \times 4 \times 2$ PLA. Therefore, we have to examine product terms by grouping 0s instead of 1. That is product terms for complement of a function.

$\therefore \bar{f}_1 = a_2 \bar{a}_0 + a_1 \bar{a}_0 + a_2 a_1$
 $\bar{f}_2 = \bar{a}_2 \bar{a}_1 + a_1 \bar{a}_0 + a_2 \bar{a}_0$

Step 2 : Implementation

Looking at function outputs we can realize that product terms $a_2 \bar{a}_0$ and $a_1 \bar{a}_0$ are common in both functions. Therefore, we need only 4 product terms and functions

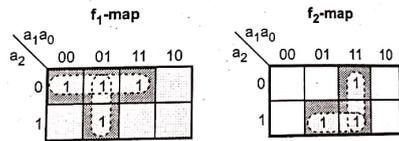


Fig. 7.13.8 K-map simplification

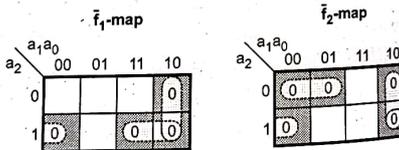


Fig. 7.13.9

can be implemented using a $3 \times 4 \times 2$ PLA as shown in Table 7.13.2 and Fig. 7.13.10.

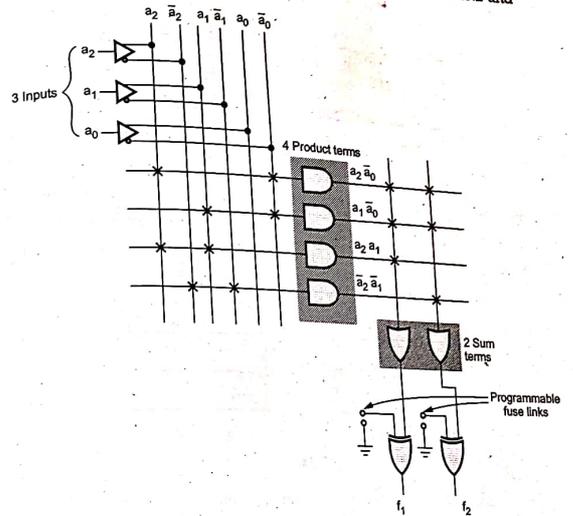


Fig. 7.13.10 Logic diagram

PLA

Product terms	Inputs			Outputs	
	a_2	a_1	a_0	f_1	f_2
$a_2 \bar{a}_0$	1	-	0	1	1
$a_1 \bar{a}_0$	-	1	0	1	1
$a_2 a_1$	1	1	-	-	-
$\bar{a}_2 \bar{a}_1$	0	0	-	-	1
				C	C

Table 7.13.2

As shown in the Fig. 7.13.10 exclusive-OR gate is programmed to invert the function to get the desired function outputs.

Example 7.13.4 A combinational circuit is defined by the functions

$F_1 = \sum m(1, 3, 5), F_2 = \sum m(5, 6, 7)$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

Solution : K-map simplification

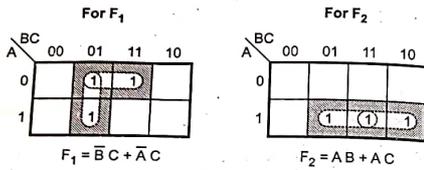


Fig. 7.13.11

- To implement functions F_1 and F_2 we require $3 \times 4 \times 2$ PLA and we have to implement them using $3 \times 3 \times 2$ PLA. Therefore we have to examine product terms by grouping 0s instead of 1. That is product terms for complement of a function.

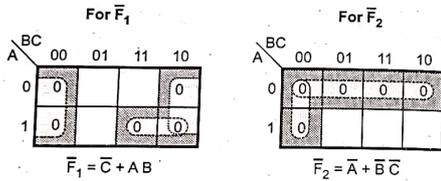


Fig. 7.13.12

- Looking at function outputs, functions \bar{F}_1 and F_2 have one common product term. Thus they have total 3 product terms and can be implemented using $3 \times 3 \times 2$ PLA.

PLA program table

Product terms	Inputs			Outputs	
	A	B	C	F_1	F_2
\bar{C}	-	-	0	1	-
AB	1	1	-	1	1
AC	1	-	1	-	1

Table 7.13.3

Implementation

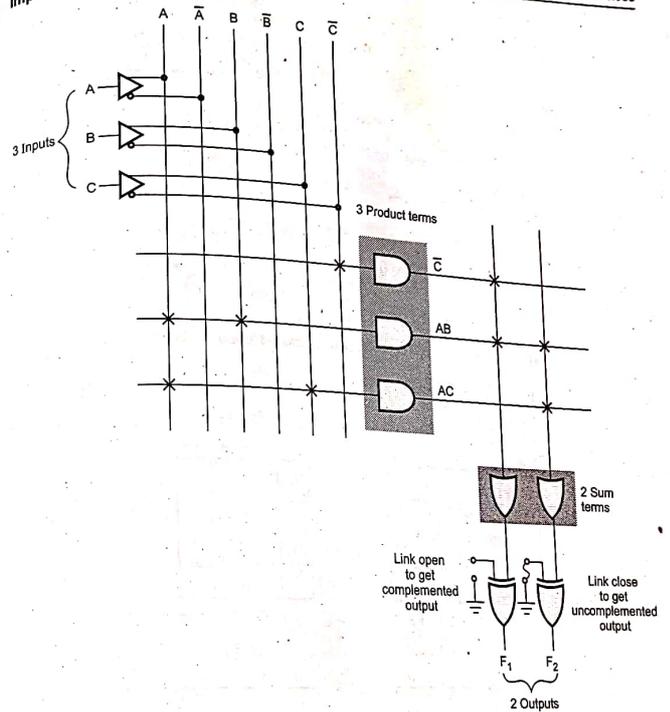


Fig. 7.13.13

Example 7.13.5 Design a BCD to Excess-3 code converter and implement using suitable PLA.

Solution :

Step 1 : Derive the truth table of BCD to Excess-3 converter

Decimal	BCD code				Excess-3 code			
	B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 7.13.4 Truth table for BCD to Excess-3 code converter

Step 2 : Simplify the Boolean functions for Excess-3 code

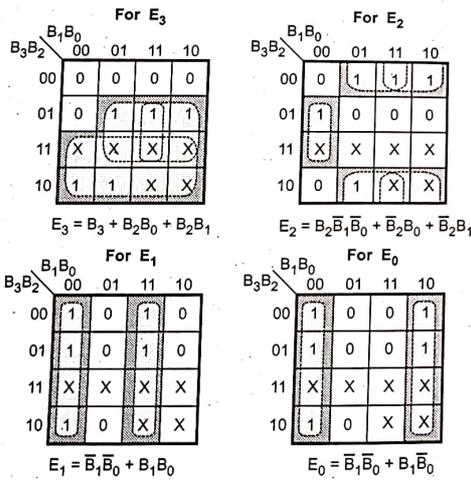


Fig. 7.13.14

Step 3 : Write PLA program table

Product terms	Inputs				Outputs			
	B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
B ₃	1	-	-	-	1	-	-	-
B ₂ B ₀	-	1	-	1	1	-	-	-
B ₂ B ₁	-	1	1	-	1	-	-	-
B ₂ B ₁ B ₀	-	1	0	0	-	1	-	-
B ₂ B ₀	-	0	-	1	-	1	-	-
B ₂ B ₁	-	0	1	-	-	1	-	-
B ₁ B ₀	-	-	0	0	-	-	1	1
B ₁ B ₀	-	-	1	1	-	-	1	1
B ₁ B ₀	-	-	1	0	-	-	-	1

Table 7.13.5 PLA program table

Step 4 : Implementation

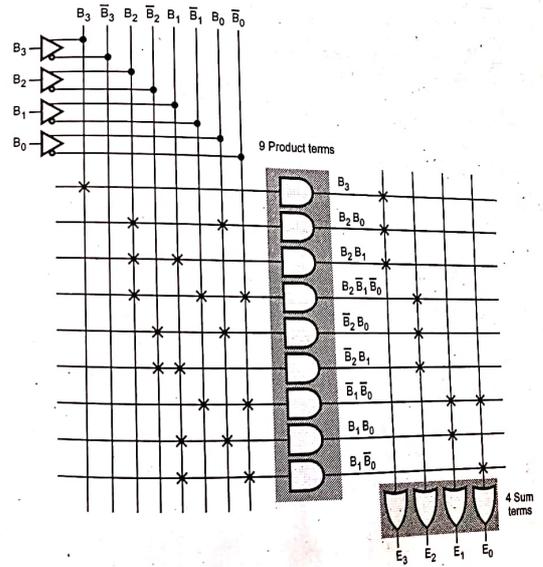


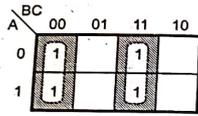
Fig. 7.13.15

Example 7.13.6 Implement the following function using PLA :

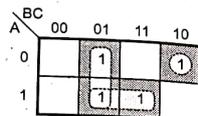
$$f_1 = \sum m(0, 3, 4, 7)$$

$$f_2 = \sum m(1, 2, 5, 7)$$

Solution : K-map simplification



$$f_1 = \overline{B}\overline{C} + BC$$



$$f_2 = \overline{B}C + AC + \overline{A}B\overline{C}$$

Fig. 7.13.16

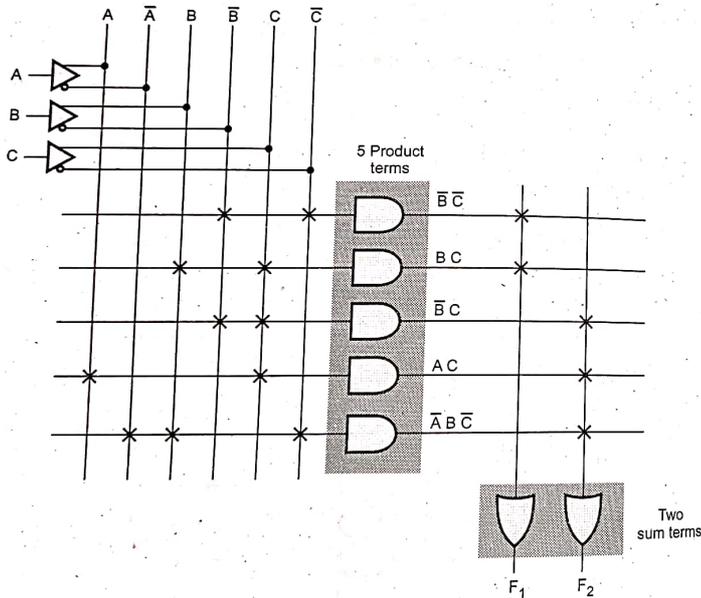


Fig. 7.13.17

Example 7.13.7 Design using PLD a 3 : 8 decoder.

Solution : The Fig. 7.13.18 shows 3 : 8 decoder using PLD.

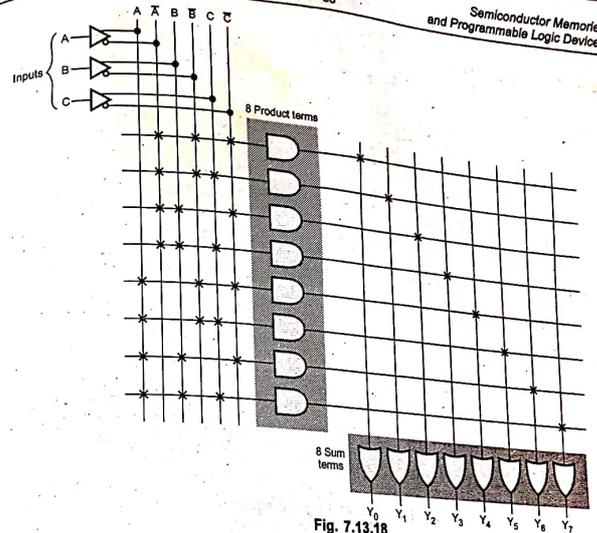
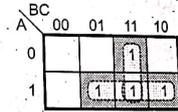


Fig. 7.13.18

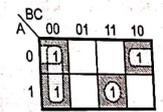
Example 7.13.8 A combinational logic circuit is defined by the functions : $F_1 = \sum (3, 5, 6, 7)$ and $F_2 = \sum (0, 2, 4, 7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs.

GTU : Winter-16, Marks 7

Solution : Step 1 : Simplify the Boolean functions



$$F_1 = AC + AB + BC$$

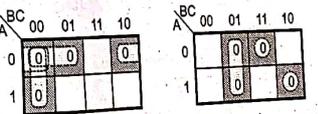


$$F_2 = \overline{B}\overline{C} + \overline{A}\overline{C} + ABC$$

Fig. 7.13.19 K-map simplification

Here, we have 6 product terms so we check for complement functions.

If we take \overline{F}_1 and \overline{F}_2 outputs of two functions, we need only four product terms since product terms $\overline{B}\overline{C}$ and $\overline{A}\overline{C}$ are common between them.



$$\overline{F}_1 = \overline{B}\overline{C} + \overline{A}\overline{C} + \overline{A}\overline{B}$$

$$\overline{F}_2 = \overline{B}C + \overline{A}B + AB\overline{C}$$

Fig. 7.13.20

Step 2 : Implementation

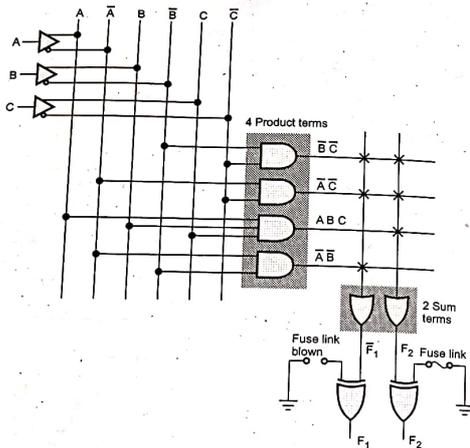


Fig. 7.13.21 Logic diagram

Review Questions

1. Explain PLA in detail.
2. Explain PLA with necessary diagrams.

GTU : May-13, Marks 7

GTU : Dec.-12, Marks 7

7.14 Programmable Array Logic (PAL)

- PAL programmable array logic is a programmable logic device with a fixed OR array and a programmable AND array.
- Because only AND gates are programmable, the PAL is easier to program, but is not as flexible as the PLA.
- Fig. 7.14.1 shows the array logic of a typical PAL.
- It has four inputs and four outputs.
- Each input has buffer and an inverter gate.
- Two gates are shown with one composite graphic symbol with normal and complement outputs.
- There are four sections. Each section has three programmable AND gates and one fixed OR gate.

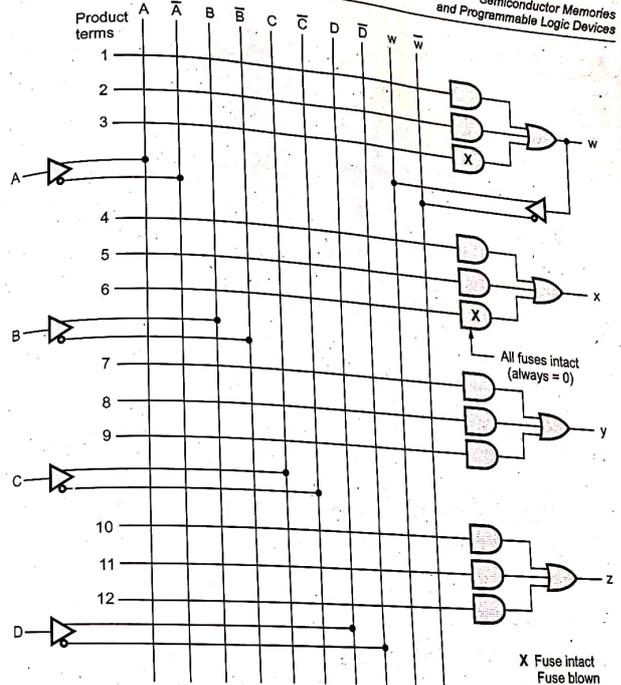


Fig. 7.14.1 Array logic for typical PAL

- The output of section 1 is connected to a buffer-inverter gate and then fed back into the inputs of the AND gates, through fuses. This allows the logic designer to feed an output function back as an input variable to create a new function. Such PALs are referred to as Programmable I/O PALs.
- The commercial PAL devices has more gates than the one shown in Fig. 7.14.1.
- A typical PAL integrated circuit may have eight inputs, eight outputs, and eight sections, each consisting of an eight wide AND-OR array.

7.14.1 Implementation of Combinational Logic Circuit using PAL

- Let us see the implementation of a combinational circuit using PAL with the help of examples.

Illustrative Examples

Example 7.14.1 Implement the following Boolean functions using PAL.

$$w(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13)$$

$$x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$$

$$y(A, B, C, D) = \sum m(2, 3, 8, 9, 10, 12, 13)$$

$$z(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 12, 14)$$

Solution :

Step 1 : Simplify the four functions

- Note that function x has four product terms. Three of them are equal to w. Therefore we can write $x = w + BCD$.

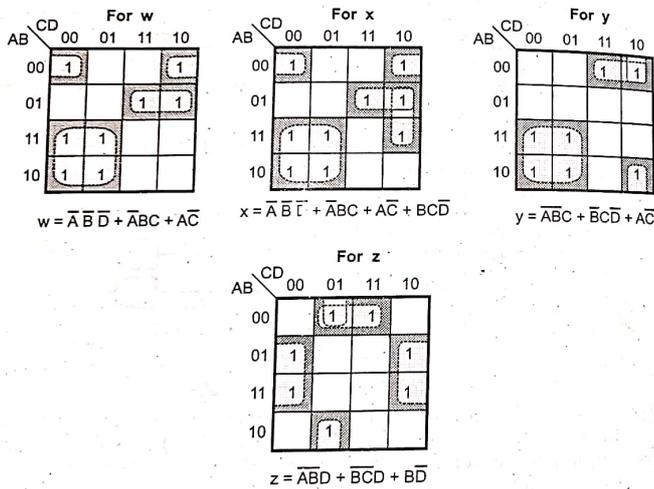


Fig. 7.14.2 K-map simplification

Step 2 : Implementation

- In the last section we have seen the PLA program table. The program table for PAL is similar to PLA program table. Table 7.14.1 shows PAL program table with product terms, AND inputs and outputs.

Product term	AND Inputs				w	Outputs
	A	B	C	D		
1	0	0	-	0	-	$w = \overline{A}\overline{B}\overline{D} + \overline{A}BC + A\overline{C}$
2	0	1	1	-	-	
3	1	-	0	-	-	
4	-	-	-	-	1	$x = w + BCD$
5	-	1	1	0	-	
6	-	-	-	-	-	$y = \overline{A}BC + \overline{B}CD + A\overline{C}$
7	0	0	1	-	-	
8	-	0	1	0	-	
9	1	-	0	-	-	$z = \overline{A}BD + \overline{B}CD + B\overline{D}$
10	0	0	-	1	-	
11	-	0	0	1	-	
12	-	1	-	0	-	

Table 7.14.1 PAL program table

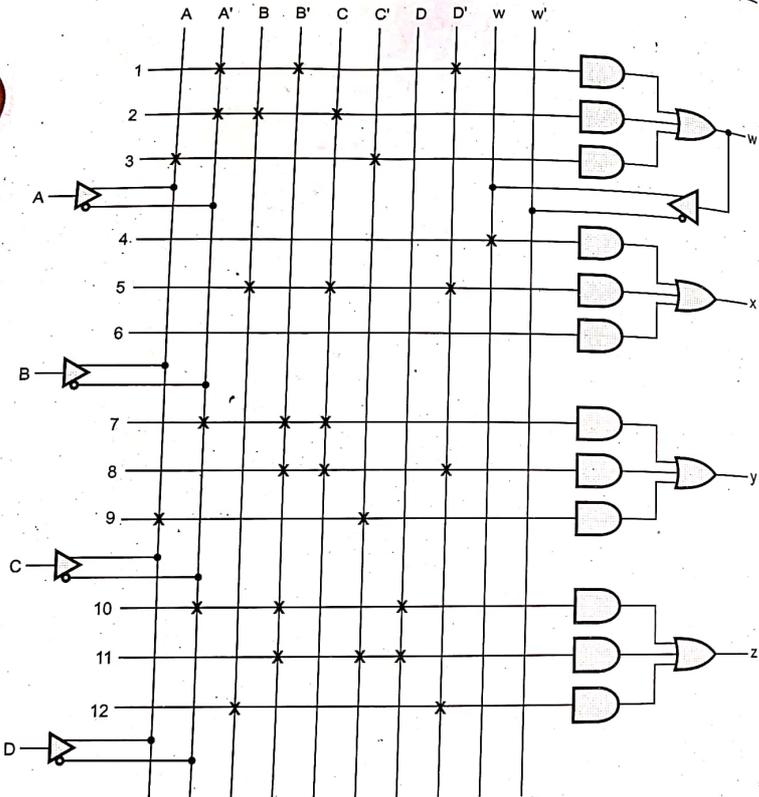


Fig. 7.14.3 Logic diagram

Example 7.14.2 Design BCD to Excess-3 converter using PAL.

Solution :

Step 1 : Derive the truth table of BCD to Excess-3 converter

Decimal	BCD code				Excess-3 code			
	B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	1	0	0
3	0	0	1	1	0	1	0	1
4	0	1	0	0	0	1	1	0
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 7.14.2 Truth table for BCD to Excess-3 code converter

Step 2 : Simplify the Boolean functions for Excess-3 code outputs.

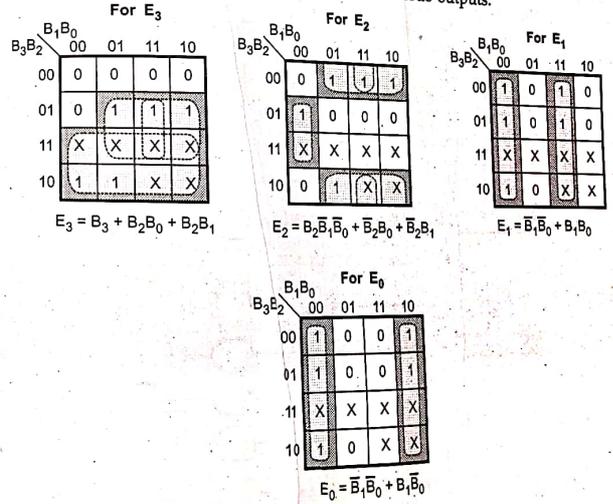


Fig. 7.14.4 K-map simplification

Step 3 : Implementation

Product terms	Inputs				Outputs			
	B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
B ₃	1	-	-	-	1	-	-	-
B ₂ B ₀	-	1	-	1	1	-	-	-
B ₂ B ₁	-	1	1	-	1	-	-	-
B ₂ B ₁ B ₀	-	1	0	0	-	1	-	-
B ₂ B ₀	-	0	-	1	-	1	-	-
B ₂ B ₁	-	0	1	-	-	1	-	-
B ₁ B ₀	-	-	0	0	-	-	1	1
B ₁ B ₀	-	-	1	1	-	-	1	-
B ₁ B ₀	-	-	1	0	-	-	-	1
					T	T	T	T
								T/C

Table 7.14.3 PAL program table

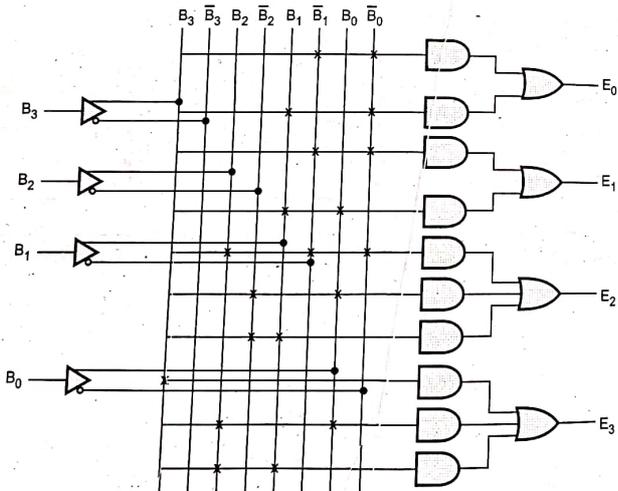


Fig. 7.14.5 Logic diagram

Example 7.14.3 Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs.
 $Y_3 = \bar{A}BCD + \bar{A}BC\bar{D} + A\bar{B}C\bar{D}$, $Y_2 = \bar{A}BCD + \bar{A}BC\bar{D} + ABCD$
 $Y_1 = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$, $Y_0 = ABCD$

Solution :

Step 1 : Simplify the Boolean functions

$$Y_3 = \bar{A}BCD + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} = (\bar{A} + A)B\bar{C}D + \bar{A}BC\bar{D}$$

$$= B\bar{C}D + \bar{A}BC\bar{D}$$

$$Y_2 = \bar{A}BCD + \bar{A}BC\bar{D} + ABCD = \bar{A}BC(\bar{D} + D) + (\bar{A} + A)(BCD)$$

$$= \bar{A}BC + BCD$$

$$Y_1 = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

$$= \bar{A}B(\bar{C} + C) + A\bar{B}C + (\bar{A} + A)B\bar{C} = \bar{A}B + A\bar{B}C + B\bar{C}$$

$$Y_0 = ABCD$$

Step 2 : Implementation

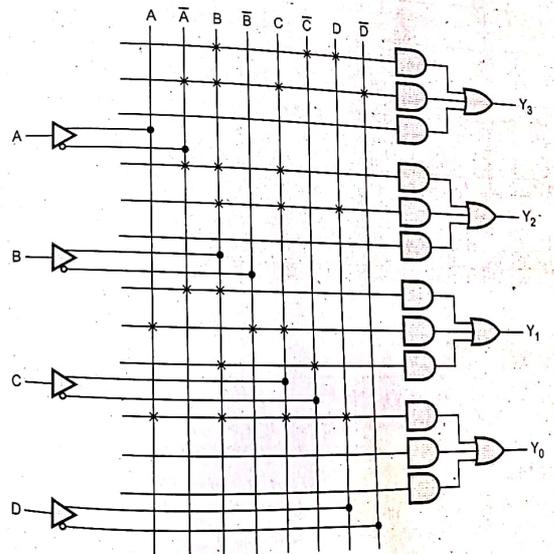


Fig. 7.14.6 Logic diagram

Example 7.14.4 Implement 4 : 1 multiplexer using PAL.

Solution : Refer section 4.10.2. The Boolean function for 4 : 1 multiplexer is

$$Y = ES_1\bar{S}_0D_0 + ES_1S_0D_1 + ES_1\bar{S}_0D_2 + ES_1S_0D_3$$

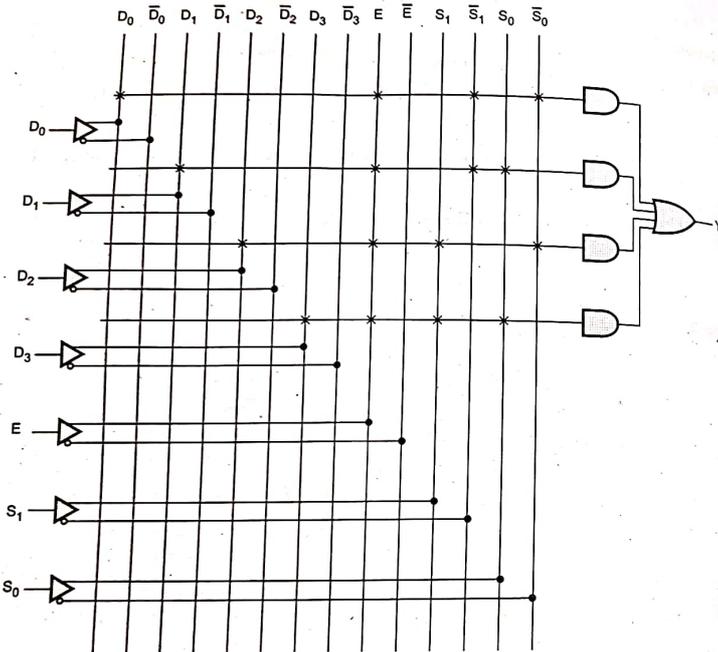


Fig. 7.14.7

Examples for Practice

Example 7.14.5 : A combinational logic circuit is defined by the following function.
 $f_1(a, b, c) = \Sigma m(0, 1, 6, 7)$, $f_2(a, b, c) = \Sigma m(2, 3, 5, 7)$. Implement the circuit with a PAL having three inputs, three product terms and two outputs.

Example 7.14.6 : Use 5 input, 3 product, 4 output PAL to realize following 3 functions.

$$F_1(A, B, C, D) = \Sigma m(2, 3, 4, 8, 9, 13, 14)$$

$$F_2(A, B, C, D) = \Sigma m(2, 3, 5, 8, 9, 14, 15)$$

$$F_3(A, B, C, D) = \Sigma m(2, 3, 4, 8, 9, 14, 15)$$

7.15 Comparison between PROM, PLA and PAL

Sr. No.	PROM	PLA	PAL
1.	AND array is fixed and OR array is programmable.	Both AND and OR arrays are programmable.	OR array is fixed and AND array is programmable.
2.	Cheaper and simple to use.	Costliest and complex than PAL and PROMs.	Cheaper and simpler.
3.	All minterms are decoded.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
4.	Only Boolean functions in standard SOP form can be implemented using PROM.	Any Boolean functions in SOP form can be implemented using PLA.	Any Boolean functions in SOP form can be implemented using PLA.

7.16 Complex Programmable Logic Devices (CPLDs)

- Simple PLDs (SPLDs) include PLAs, PALs and other similar types of devices.
- SPLDs have limitations of number of input product terms and outputs. For applications which requires more number of inputs or product terms or output we have to expand the capacity of PLDs by cascading them.
 - The Complex Programmable Logic Devices (CPLDs) are introduced to solve the above mentioned difficulty of SPLDs. A typical CPLD is merely a collection of multiple PLDs and an interconnection structure, all on the same chip, as shown in the Fig. 7.16.1.

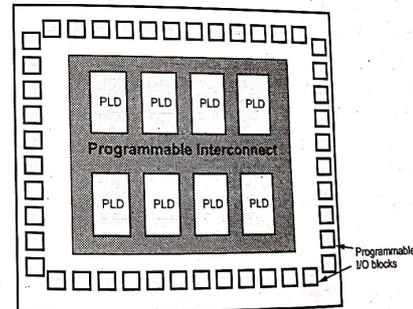


Fig. 7.16.1 General architecture of CPLD

- In CPLDs, in addition to the individual PLDs the on-chip interconnection structure is also programmable. Therefore, unlike PLDs, the CPLDs can be scaled to larger sizes by increasing the number of individual PLDs.

7.16.1 Block Diagram

- The Fig. 7.16.2 shows the block diagram of a Complex Programmable Logic Device (CPLD).

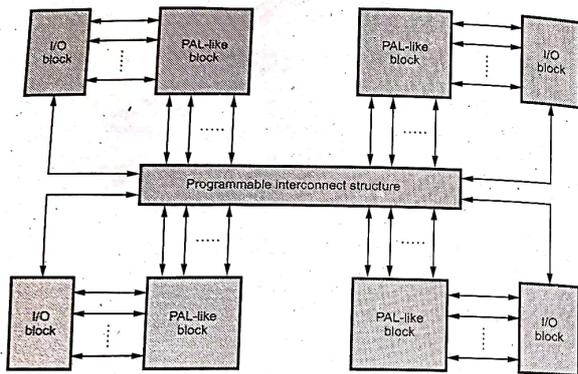


Fig. 7.16.2 Block diagram of CPLD

- It consists of collection of PAL like blocks, I/O blocks and a set of interconnection wires, called programmable interconnection structure.
- The PAL like blocks are connected to the programmable interconnect structure and to the I/O blocks. The chip input-output pins are attached to the I/O blocks.
- A PAL like block in the CPLD usually consists of about 16 macrocells. Like other macrocells, the macrocell in CPLD consists of AND-OR configuration, an EX-OR gate, a flip-flop, a multiplexer, and a tri-state buffer.
- The Fig. 7.16.3 shows the typical macrocell for CPLD. Each AND-OR configuration usually consists of 5-20 AND gates and an OR gate with 5-20 inputs.
- The EX-OR gate provides the output of OR-gate in inverted or non-inverted form as per the fuse link status.
- A D flip-flop stores the output of EX-OR gate.
- A multiplexer selects either the output of the D flip-flop or the output of the EX-OR gate depending upon its select input (either 1 or 0).
- The tri-state buffer acts as a switch which enables or disables the output.

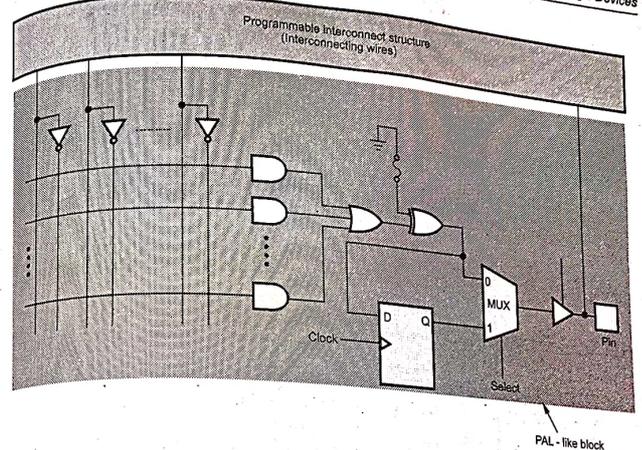


Fig. 7.16.3 A structure of typical macrocell of a CPLD

7.16.2 Architecture of XC9572 CPLD

- The XC9572 is a device from XC9500 CPLD family. It consists of 4 functional blocks (FBs), 72 macrocells, 1600 usable gates and 72 registers. The XC9572 device is available in several different packages. Different I/O packages have different number of I/O pins. For example, 44-pin PLCC has 34 I/O pins and 100-pin TQFP has 72 I/O pins.
- In XC9572, the functional blocks and I/O blocks are fully interconnected by the FastCONNECT switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capacity with 36 inputs and 18 outputs. The Fast CONNECT switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, 12 to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. This is illustrated in Fig. 7.16.4.

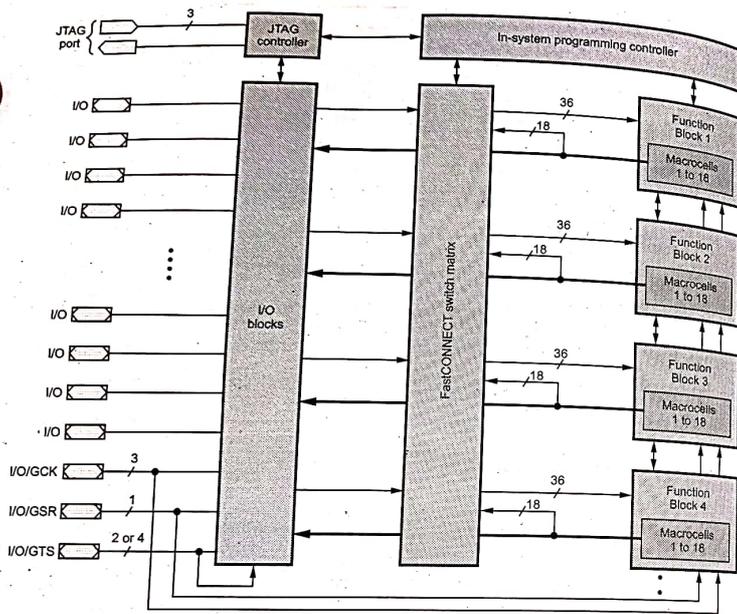


Fig. 7.16.4 XC9500 architecture

Review Questions

1. State the limitation of SPLD.
2. Draw and explain the general architecture of CPLD.
3. What it meant by CPLD ? Draw and explain the block diagram of CPLD.
4. Explain the architectural features of XC9572.
5. Draw the basic structure of CPLD. Explain its features in brief.

7.17 Field Programmable Gate Array (FPGA)

GTU : Winter-15

- Field Programmable Gate Arrays (FPGA) provide the next generation in the programmable logic devices.
- The word field in the name refers to the ability of the gate arrays to be programmed for a specific function by the user instead of by the manufacturer of the device.
- The word array is used to indicate a series of columns and rows of gates that can be programmed by the end user.
- As compared to standard gate arrays, the field programmable gate arrays are larger devices.
- The basic cell structure for FPGA is some what complicated than the basic cell structure of standard gate array.
- The programmable logic blocks of FPGAs are called logic blocks or Configurable Logic Blocks (CLBs).
- The basic architecture of FPGA consists of an array of logic blocks with programmable row and column interconnecting channels surrounded by programmable I/O blocks as shown in Fig. 7.17.1.

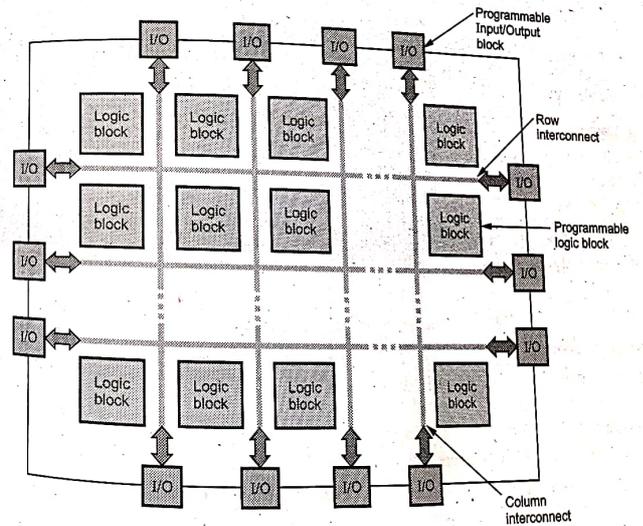


Fig. 7.17.1 Basic architecture of FPGA

- Many FPGA architectures are based on a type of memory called LUT (look-up table) rather than on (sum of product) SOP AND/OR arrays as CPLDs are.
- Another approach found on some FPGAs is the use of multiplexers to generate logic functions.

LUT :

- It is the look-up table used in FPGAs.
- It is actually a memory device that can be programmed to perform logic functions.
- The LUT essentially replaces the AND/OR array logic in a CPLD.
- Fig. 7.17.2 shows a simple diagram of an 8 bit by 1 bit (8 × 1) memory programmed to produce to SOP function $\bar{A}\bar{B}C + \bar{A}BC + ABC$.
- When any one of the three product terms appears on the LUT inputs, the corresponding memory cell storing a 1 is selected and the 1 (HIGH) appears on the output.
- For any product terms that are not part of the SOP function, the LUT output is 0 (LOW).

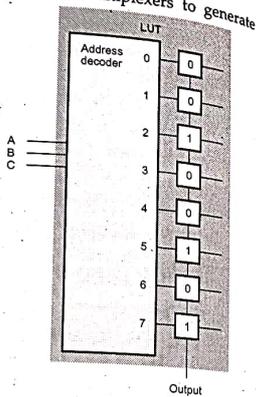


Fig. 7.17.2 An LUT programmed to produce the SOP function

The Logic Block :

- Each logic block in a generic FPGA contains several logic elements, as shown in Fig. 7.17.3.
- Generally there can be well over ten thousand logic elements in a single chip.

The Logic Element :

- A simplified diagram of a typical FPGA logic element is shown in Fig. 7.17.4. It contains an LUT, associated logic, and a flip-flop.

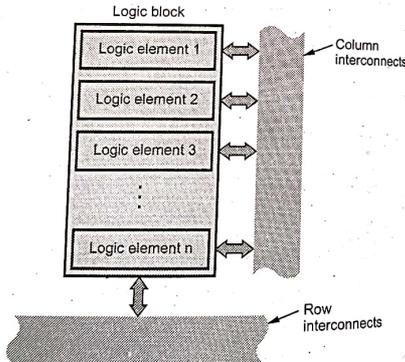


Fig. 7.17.3 Basic logic block in an FPGA

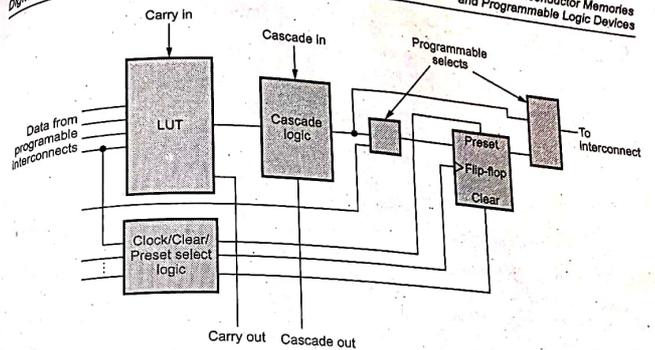


Fig. 7.17.4 A simplified typical FPGA logic element

- Each logic element contains a 4-input LUT that can be programmed as logic function generator.
- It can be used to produce SOP functions or logic functions such as adders and comparators.
- When configured as an adder, the carry in and carry out allow for adder expansion.
- Using the cascade logic, an LUT can be expanded by cascading with LUT's in other logic elements.
- The programmable selects let you choose either combinational functions from the LUT output or registered functions from the flip-flop output.

Example 7.17.1 Explain two input LUT with implementation of the function :

$$F(A, B) = \sum m(0, 3).$$

Solution : Two input LUT has $2^2 \times 1$ -bit memory, i.e. 4×1 -bit memory. We can implement the given function with 2-input LUT as shown in the Fig. 7.17.5.

The bit corresponding of the two-inputs of one bit wide memory array are available at the output of LUT. For example, if inputs AB are 00, the bit from first location is available at the output. Storing logic 1 at bit 0 and bit 3 positions, and storing logic 0 at bit 1 and bit 2 positions we can implement the given function.

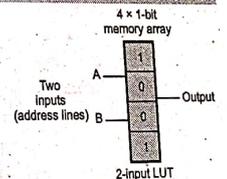


Fig. 7.17.5

Example 7.17.2 Explain the three input LUT with implementation of a full adder.

Solution : Fig. 7.17.6 shows an 8×2 LUT is programmed as a full adder. The sum and carry out expressions for a full-adder are as follows :

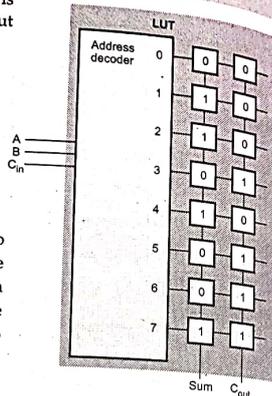
$$\begin{aligned} \text{Sum} &= (A + B) + C_{in} \\ &= \bar{A} \bar{B} C_{in} + \bar{A} B \bar{C}_{in} + A \bar{B} \bar{C}_{in} + ABC_{in} \\ C_{out} &= AB + (A + B)C_{in} \\ &= \bar{A} B C_{in} + A \bar{B} C_{in} + A B \bar{C}_{in} + ABC_{in} \end{aligned}$$

Interconnection Technology

FPGAs use either SRAM or antifuse methods to provide interconnections between logic blocks. The antifuse is normally open and is shorted to create a connection when programmed, compared to the fuse which is normally shorted and is opened to create no connection when programmed.

In SRAM method, a transistor is controlled by the state of an on-chip SRAM cell. When SRAM cell contains zero, the transistor is off and connection is open. When SRAM cell contains one, the transistor is ON and connection is shorted.

Fig. 7.17.6 An LUT programmed as full-adder



Review Questions

1. What is FPGA ? What are its salient features ?
2. Draw and explain the structural block diagram of FPGA.
3. What do you mean by FPGA ? Explain the details of internal architecture of FPGA. How will you design any digital circuit with the help of FPGA ?
4. With the help of structural block diagram explain FPGA with respect to :
1) Storage cell content in LUT 2) Three input LUT 3) Inclusion of a flip-flop in an FPGA logic.
5. What is LUT in FPGA ?
6. Write a short note on FPGA.
7. Draw and explain basic architecture of FPGA. State difference between PLA and FPGA.
8. What are registered programmable devices ?
9. Draw and explain in brief general architecture of Xilinx FPGA. **GTU : Winter-15, Marks 3**

7.18 Comparison between CPLDs and FPGAs

No.	CPLD	FPGA
1.	Fig. 7.16.1 shows basic architecture of CPLD.	Fig. 7.17.1 shows the basic architecture of FPGA.
2.	They consist of PAL like blocks, I/O blocks and programmable interconnect structures.	They consist of Configurable Logic Blocks (CLBs), I/O blocks, row interconnect and column interconnect.
3.	They use AND/OR arrays to generate logic functions.	They use memory called LUT (Look-up Table) or multiplexers to generate logic functions.
4.	They are programmed for a specific function by the manufacture of the device.	They are programmed for specific function by the user.
5.	It is more suitable in small gate count designs.	It is more suitable in high gate count designs since it has very high logic capacity.
6.	Less complex architecture.	More complex architecture.
7.	Delays are more predictable.	Delays are quite unpredictable.
8.	CPLD contains a few blocks of logic that reaches up to a few thousands.	FPGA contains upto 100 000 of tiny logic blocks.
9.	It is considered as coarse-grain device.	It is considered as a fine-grain device.
10.	CPLDs are made of larger blocks.	FPGAs are made up of tiny logic blocks.
11.	CPLD is EPROM-based digital logic chip.	FPGA is RAM based digital logic chip.
12.	It is much cheaper.	It is more expensive.
13.	Example : XC 9500 family.	Example : Xilinx 4000 family

Review Question

1. Explain difference between FPGA and CPLD.

Oral Questions and Answers

Q.1 Define a memory cell. Give an example.

Ans. : Memories are made up of registers. Each register consists of storage elements (flip-flops or capacitors in semiconductor memories and magnetic domain in magnetic storage), each of which stores one bit of data. Such a storage element is called a memory cell.

Q.2 Define a memory location.

Ans. : Memories are made up of registers. Each register in the memory is one storage location also called memory location. Each memory location is identified by an address.

Q.3 Explain 'write operation' with an example. (Refer section 7.1)

Q.4 What is a volatile memory? Give example.

Ans. : The memory which cannot hold data when power is turned off is known as volatile memory. The static RAM is a volatile memory.

Q.5 Name the types of ROM.

Ans. : There are four types of ROM : Masked ROM, PROM, EPROM and EEPROM or E²PROM.

Q.6 What is non-volatile memory ? (Refer section 7.2)

Q.7 Which memory is called volatile ? Why ? (Refer section 7.2)

Q.8 What is meant by 'static' and 'dynamic' memories ? (Section 7.3)

Q.9 Explain static memory. (Section 7.6.1)

Q.10 Define address and word.

Ans. : In a ROM, each bit combination of the input variable is called an address. Each bit combination that comes out of the output lines is called a word.

Q.11 Explain ROM.

Ans. : A Read Only Memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2^n .

Q.12 How does ROM retain information ?

Ans. : ROMs are hardwired devices. It contains memory array of programmed to retain information.

Q.13 Define PROM.

Ans. : PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

Q.14 How is individual location in a EEPROM programmed or erased ?

Ans. : Since it is electrically erasable memory, by activating particular row and column it is possible that individual can be programmed or erased.

Q.15 Mention the two types of erasable PROM. (Refer sections 7.5.2 and 7.5.3)

Q.16 Whether ROM is classified as nonvolatile storage device? Why ? (Refer section 7.5)

Q.17 Write the advantages of EPROM over PROM. (Refer section 7.5.3)

Q.18 What is EAPROM. (Refer section 7.5.4)

Q.19 Briefly explain about EEPROM. (Refer section 7.5.3)

Q.20 What is RAM ?

Ans. : Random Access Memory. Read and write operation can be carried out. It is a volatile memory. It can hold data as power is ON.

Q.21 Give the advantages of RAM.

Ans. : Advantages of RAM are :

1. RAM is a memory where we can read as well as write the data.
2. It is random access memory i.e. the particular memory location can be accessed using the address of the at memory location.
3. Higher speed.

Q.22 What is read and write operation ?

Ans. : The write operation stores data into a specified address into the memory and the read operation takes data out of a specified address in the memory.

Q.23 List the two categories of RAM. (Refer section 7.6)

Q.24 Define dynamic RAM.

Ans. : Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

Q.25 List the two types of SRAM.

Ans. : Asynchronous SRAMs and Synchronous Burst SRAMs.

Q.26 List the basic types of DRAMs.

Ans. : Fast page Mode DRAM, Extended Data Out DRAM (EDO DRAM), Burst EDO DRAM and Synchronous DRAM.

Q.27 Draw the basic dynamic memory cell. (Refer section 7.6)

Q.28 Draw the logic diagram of a memory cell. (Refer section 7.6)

Q.29 Draw the block diagram of dynamic RAM cell. (Refer section 7.6)

Q.30 Define PLD.

Ans. : Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions.

Q.31 Give the classification of PLDs.

Ans. : PLDs are classified as :

- PROM(Programmable Read Only Memory),
- Programmable Logic Array(PLA),
- Programmable Array Logic (PAL), and
- Generic Array Logic(GAL)

Q.32 What is a PLA ?

Ans. : PLA stands for Programmable Logic Array, which is a LSI component. In PLA, both AND and OR gates have fuses at the inputs, therefore in PLA both AND and OR gates are programmable. The outputs from OR gates go through fuses as inputs to output inverters so that final output can be programmed as either AND-OR or AND-OR-INVERT.

Q.33 Why was PAL developed ?

Ans. : PAL is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

Q.34 Why the input variables to a PAL are buffered ?

Ans. : The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

Q.35 Mention few applications of PLA and PAL.

Ans. : Applications of PLA and PAL are :

- They are used to implement combinational circuits.
- Registers PALs can be used to implement sequential circuits.
- They are used as a combinational logic in addressing decoding section of a microprocessor based systems.
- They can be programmed to use as code converters.

Q.36 What is FPGA ?

Ans. : FPGA stands for field programmable gate array, which is the next generation in the programmable logic devices. The word field refers to the ability of the gate arrays to be programmed for a specific function by the end user. The word array indicates a series of columns and rows of gates that can be programmed by the end user.

Q.37 List the configurable elements in the FPGA architecture.

Ans. : The FPGA architecture consists of three types of configurable elements :

1. A perimeter of Input/Output Blocks (IOBs).
2. A core array of Configurable Logic Blocks (CLBs).
3. Resources for interconnection.

Q.38 How does the architecture of a PLA differ from a PROM ?

Ans. : Refer section 7.15.

Q.39 What is PAL ? How does it differ from PLA ?

Ans. : Refer sections 7.14 and 7.15.

Notes

SOLVED MODEL QUESTION PAPER**[As per New Question Paper Pattern]**
Digital Fundamentals

Semester - III (CE/IT)

Time : 2 $\frac{1}{2}$ Hours]

[Total Marks : 70

Instructions :

- 1) Attempt all questions.
- 2) Make suitable assumptions wherever necessary.
- 3) Figures to the right indicate full marks.

- Q.1**
- a) Convert decimal number $(0.252)_{10}$ to binary with an error less than 1%. (Refer example 1.4.23) (3)
 - b) Convert the decimal number 250.5 to base 3, base 4, base 7 and base 16. (Refer example 1.4.15) (4)
 - c) Simplify : 1) $\overline{AB} + \overline{ABC} + \overline{ABCD} + \overline{ABCDE}$
2) $(P + Q + R)(\overline{P} + \overline{Q} + \overline{R})P$ (Refer example 2.2.9) (7)
- Q.2**
- a) Explain following terms w.r.t. Digital Logic Family : 1) Fan - in 2) Noise Margin 3) Power Dissipation.. (Refer section 3.2) (3)
 - b) Draw and explain the working of 2-input NAND gate. (Refer section 2.1) (4)
 - c) Attempt following : 1) Convert into sum-of -minterms : $\overline{A} + B + CA$
2) Convert into product-of-maxterms : $A(\overline{A} + B)\overline{C}$. (Refer example 4.1.13) (7)
- OR**
- c) Minimize the following logic function
 $F(A, B, C, D) = \pi M(1, 2, 3, 8, 9, 10; 11, 14) \cdot d(7, 15)$
Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only. (Refer example 4.7.27) (7)
- Q.3**
- a) State the design procedure for combinational circuits. (Refer section 4.8.2) (3)
 - b) Implement the following Boolean functions with a decoder.
 $F(w, x, y, z) = \sum (1, 3, 5, 6, 11, 14, 15)$ (Refer example 4.12.6) (4)

- c) Minimize the following function by tabular method :
 $f(w, x, y, z) = \sum m(1, 4, 8, 9, 13, 14, 15) + d(2, 3, 11, 12)$.
 (Refer example 4.9.5) (7)

OR

- Q.3** a) What is encoder ? (Refer Oral Q.18 of Chapter - 4) (3)
 b) Explain full adder in detail. (Refer section 4.14.2) (4)
 c) Implement following logic function using 8×1 MUX.
 $F = \sum m(0, 1, 3, 5, 7, 11, 13, 14, 15)$ (Refer example 4.10.19) (7)
- Q.4** a) Compare combinational and sequential circuits. (Refer section 5.1.1) (3)
 b) Describe working of look-ahead-carry adder. (Refer section 4.17) (4)
 c) Design 2-bit comparator using gates. (Refer example 4.18.1) (7)

OR

- Q.4** a) Draw gated SR latch using NAND gates only. (Refer Fig. 5.4.5 (a)) (3)
 b) Explain working of master - slave JK flip - flop with necessary logic diagram, state equation and state diagram. (Refer section 5.4.7) (4)
 c) Design a mod-12 synchronous up counter using D-flipflop. (Refer example 5.9.19) (7)
- Q.5** a) Compare three A/D conversion techniques. (Refer section 6.8.4) (3)
 b) Explain the operation of 4-bit SISO shift register using D flip-flops. (Refer section 5.8.2.1) (4)
 c) Explain R/2R ladder technique of D/A conversion. (Refer section 6.2.2.2) (7)

OR

- Q.5** a) Write a short note on FPGA. (Refer section 7.17) (3)
 b) List down the various types of ROMs and discuss any two of them. (Refer section 7.5) (4)
 c) Design a BCD to Excess-3 code converter and implement using suitable PLA. (Refer example 7.13.5) (7)

□□□